

# Pivotal Memory Technologies Enabling New Generation of AI Workloads

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**Tien Shiah**

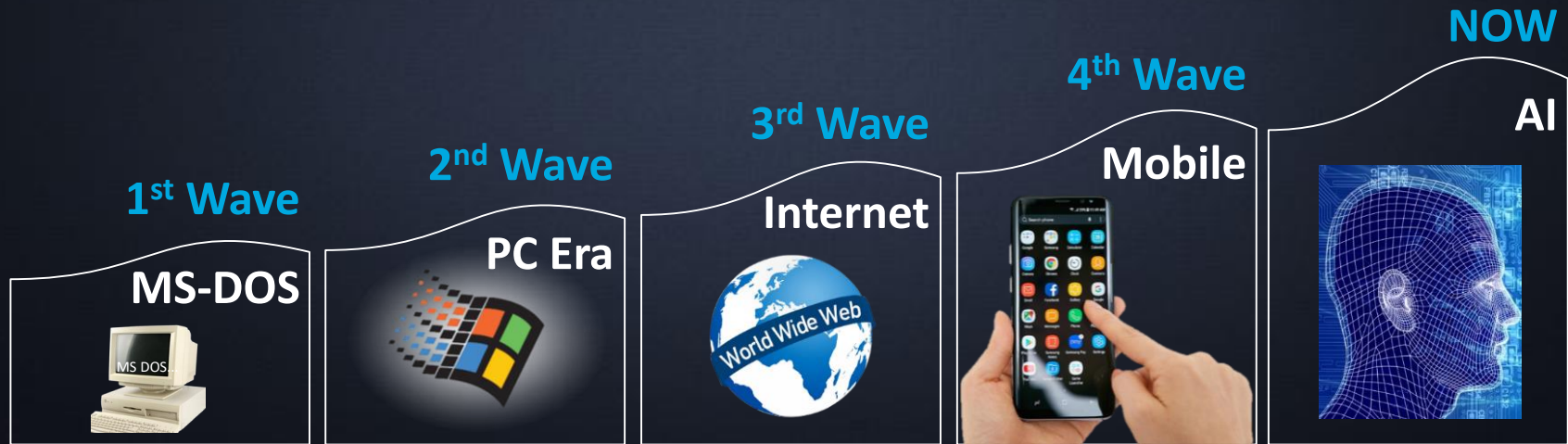
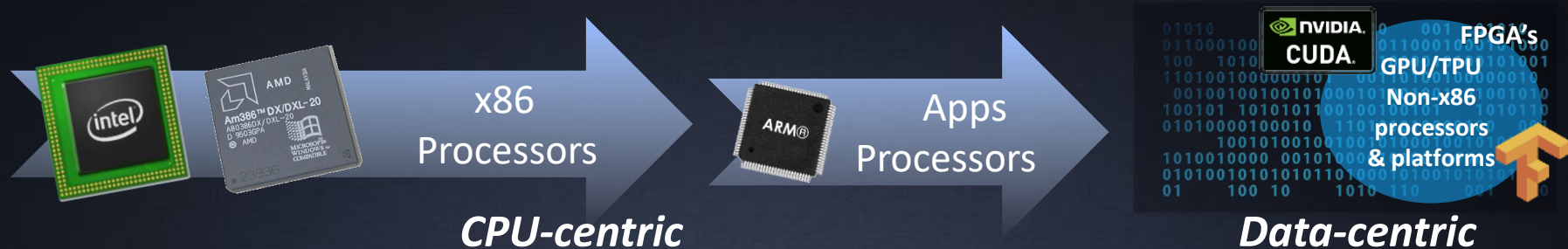
Memory Product Marketing  
Samsung Semiconductor Inc.

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# Applications drive Changes in Architectures



# Artificial Intelligence → MAINSTREAM

## Speech, Natural Language



*Amazon Echo & Alexa  
Google Smart Home Devices  
Siri & Cortana Smart Assistants*

## Deep Learning



*Screening*



*Genomics*



*Prediction*



*Game Theory*

## Image / Facial Recognition



## Autonomous Driving

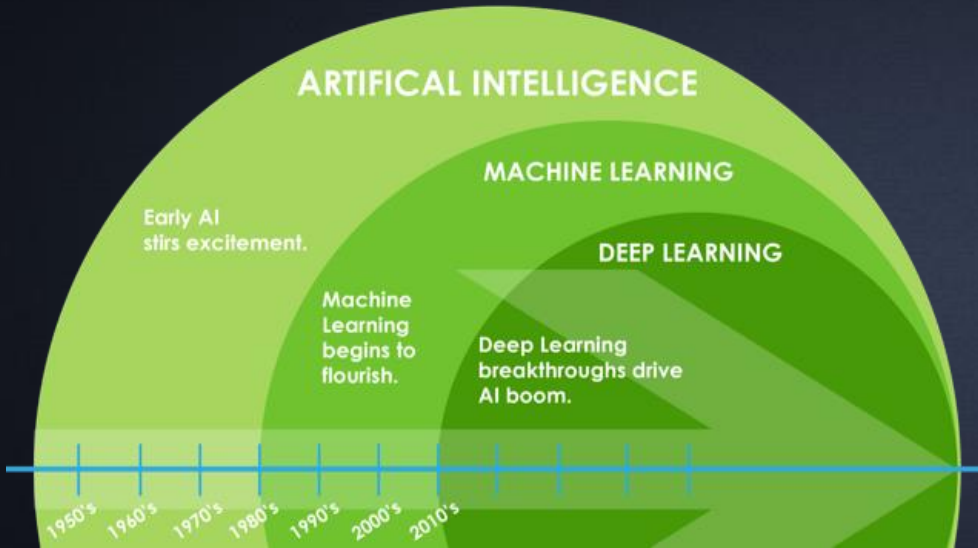


**TESLA**

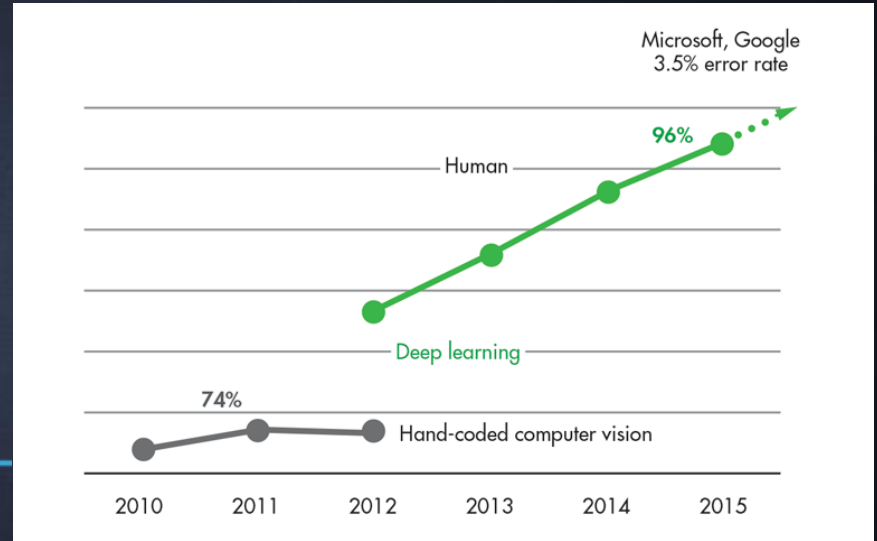


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# AI – What has Changed?



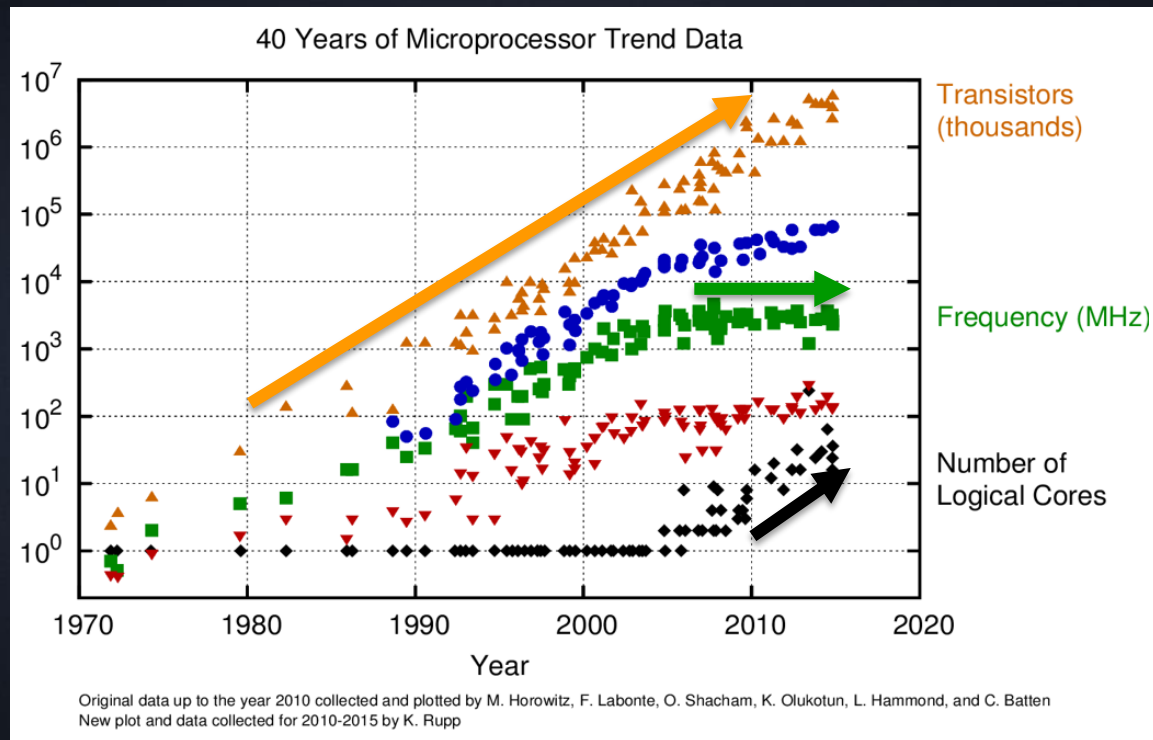
Source: Tuples Edu, buzzrobot.com



Source: Nvidia, FMS 2017

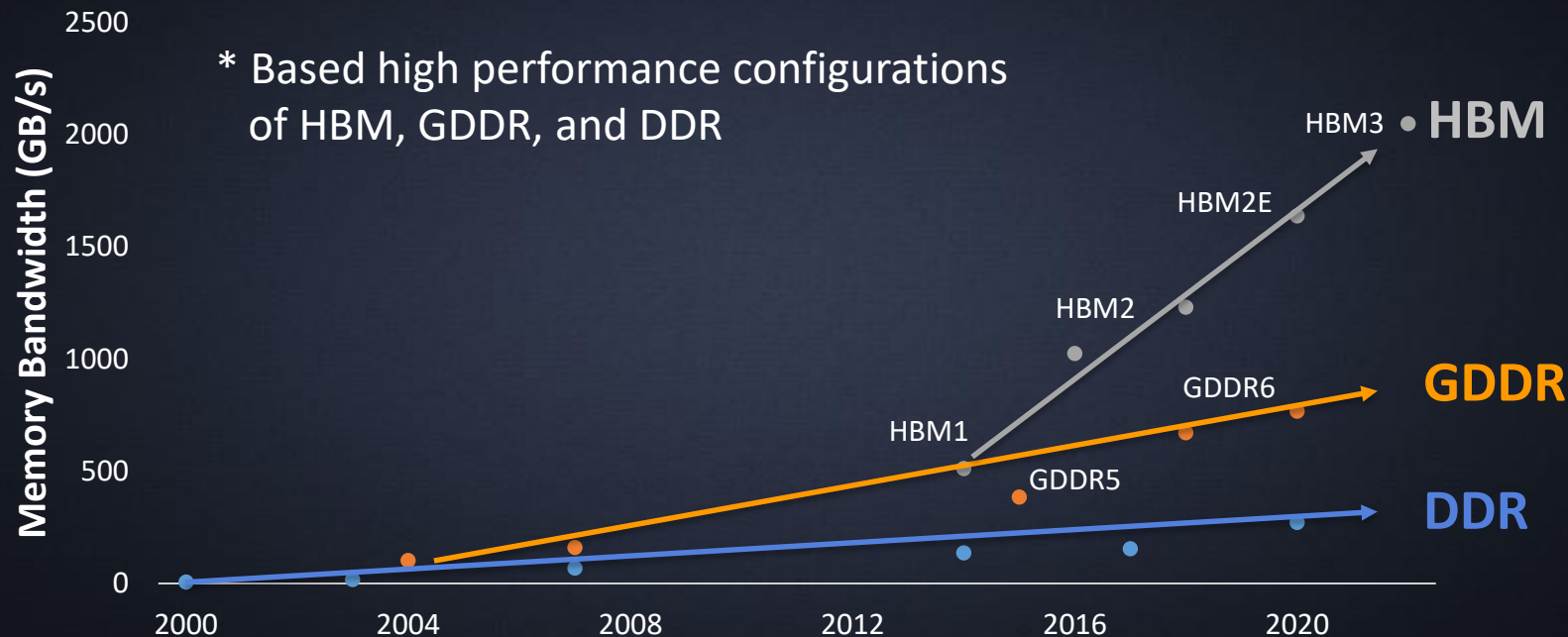
*Deep Learning algorithms require high memory bandwidth*

# Faster Computation → Multi-core



*High performance compute requires high memory bandwidth*

# Memory Bandwidth Comparison





# HBM: High Bandwidth Memory

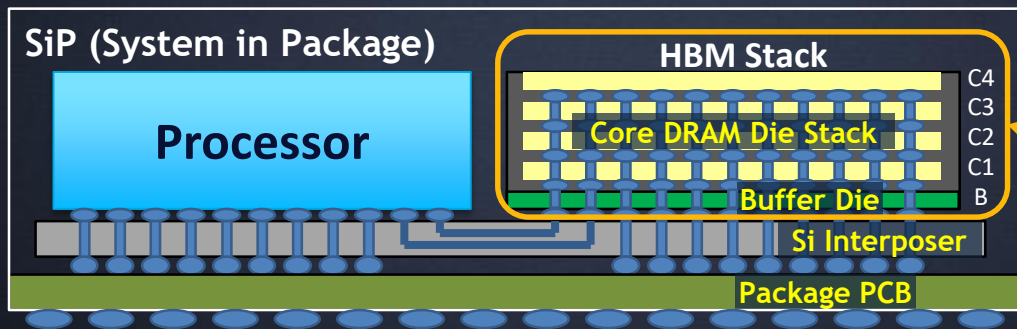
- Stacked MPGA (micro-pillar grid array) memory solution for high performance applications
- Samsung launched HBM2 in Q1 2016
- Uses DDR4 die with TSV (Through Silicon Vias)
- Available in 4H or 8H stacks
- Key Features:
  - 1024 I/O's (8 Channel, 128bits per channel)
  - Per stack: 307GB/s (current generation)
    - 77X the speed of a PCIe 3.0 x4 slot, or
    - 77 HD movies transferred per second

**\*\* Announced HBM2E: +33% throughput (410GB/s), 2X density (16GB stack) \*\***



# HBM Basics: 2.5D System In Package

- A typical HBM SiP consists of a processor (or ASIC) and 1 or more HBM stacks mounted on a Silicon Interposer
- The HBM consists of 4 or 8 DRAM die mounted on a buffer die

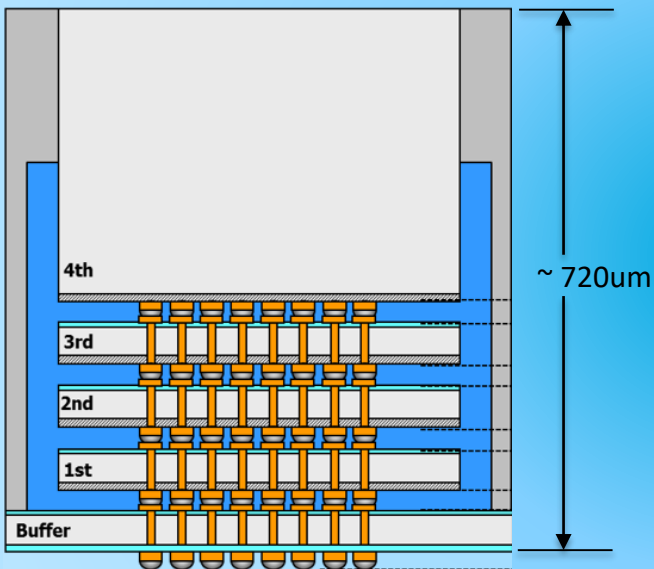


*Samsung  
manufactures  
and sells the  
HBM stack*

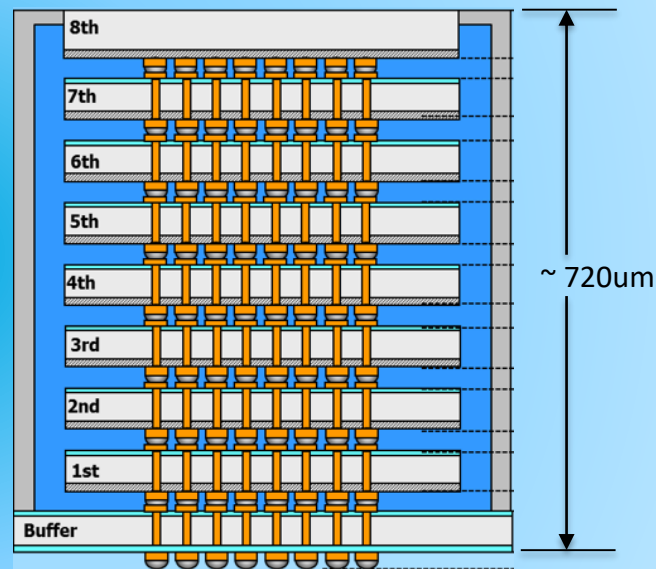
- The entire system (Processor + HBM stack + Si Interposer) is encapsulated into one larger package by the customer

# MPGA: Micro-Pillar Grid Array

## Four High Stack (4H)



## Eight High Stack (8H)



# Not just about speed: Space Efficiency

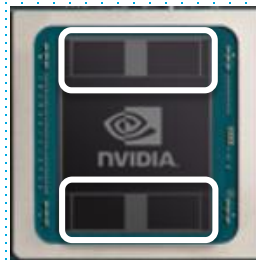
## GDDR5



Density	1 GB x 12 = 12GB
Speed/pin	1 GB/s
Pin count	384
B/W	384 GB/s

## HBM2E

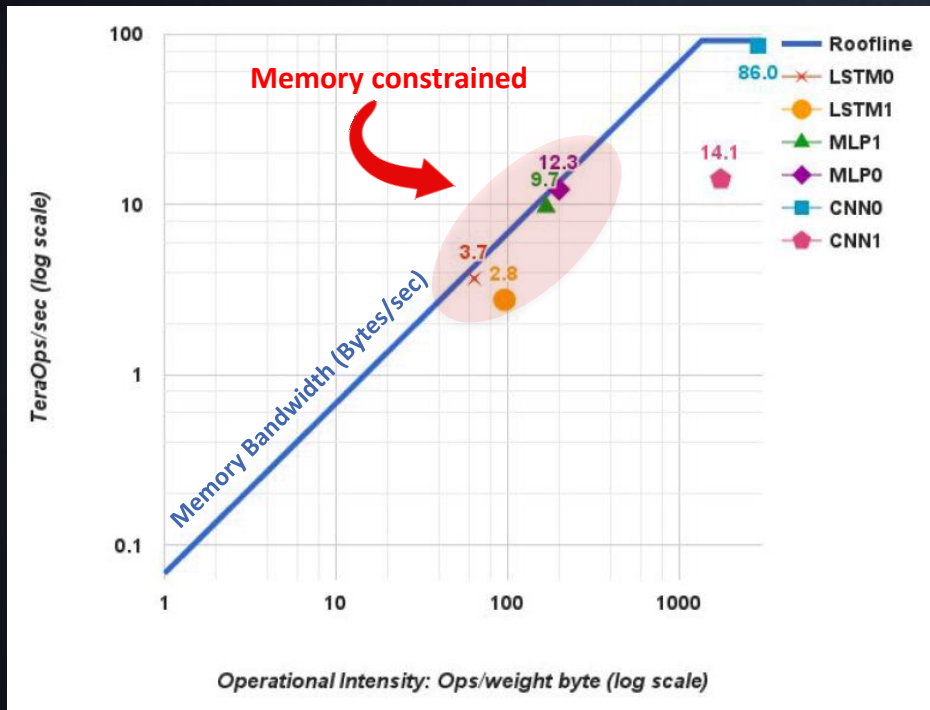
Real estate savings



Density	16 GB x 4 = 64GB
Speed/pin	0.4 GB/s
Pin count	4096
B/W	1,640 GB/s

# AI: Compute vs. Memory Constrained

## Roofline Model for TPU ASIC



Source: Google ISCA 2017

## Roofline Model

- Point below slope = memory bandwidth constrained
- Point below horizontal = compute constrained

Neural Network	Characteristic	Use Case
MLP	Structured input features	Ranking
CNN	Spatial processing	Image recognition
RNN	Sequence processing	Language translation

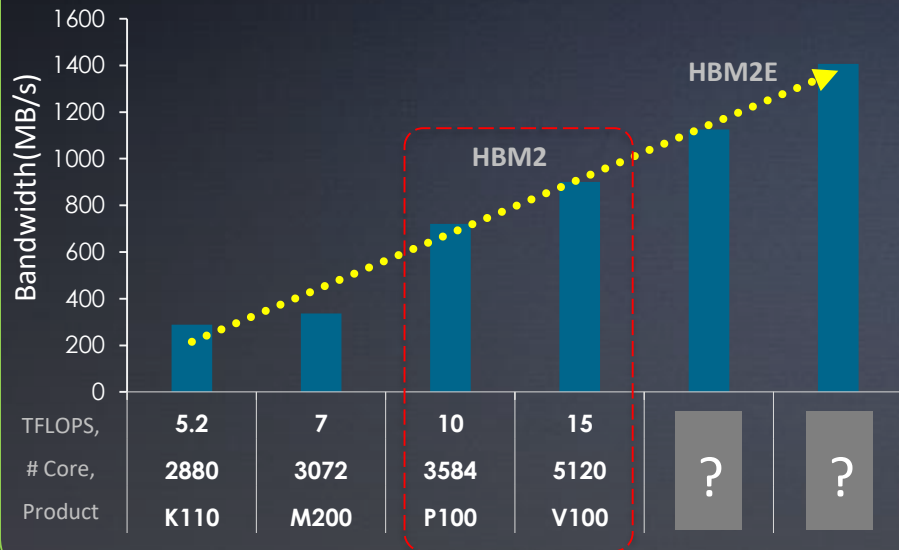
\* LSTM (Long Short-Term Memory) is subset of RNN

*Many Deep Learning applications are  
MEMORY bandwidth constrained  
→ Need High Bandwidth Memory*

# Memory Drives AI Performance

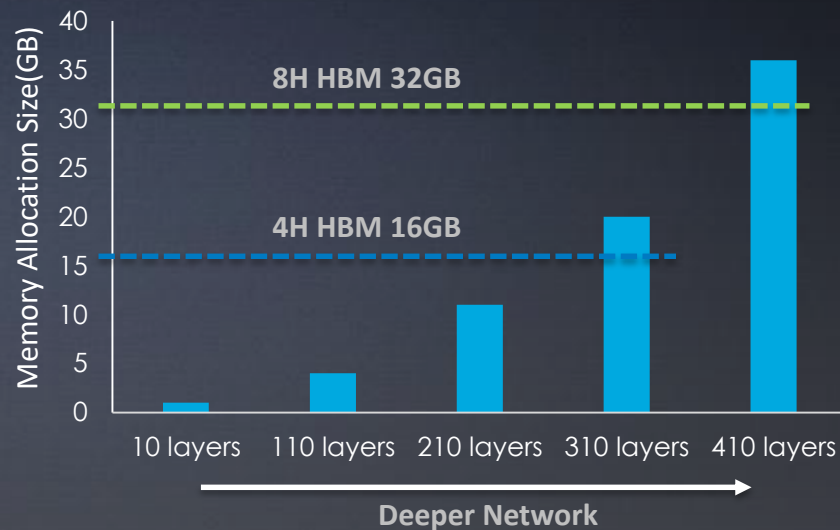
✓ **Faster Training, More Bandwidth**

## Required Memory BW (GB/s)



✓ **Better Accuracy, More Capacity**

## Memory allocation size (GB)



# HBM Presence – Some Examples



**NVIDIA**

## **Datacenter** (Acceleration, AI/ML)

- Tesla P100, V100
- DGX Station, DGX1, DGX2
- GPU Cloud
- Titan V

AI Cities  
Healthcare  
Retail  
Robotics  
Autonomous cars

## **Professional Visualization**

- Quaddro GP100, GV100

Architecture  
Engineering/Construction  
Education  
Manufacturing  
Media & Entertainment



**AMD**

## **Datacenter** (Acceleration, AI/ML)

- Radeon Instinct MI25
- Project 47

Traffic sign recognition  
Image synthesizer  
Object classifier  
Model conversion

## **Professional Visualization**

- Radeon Pro WX, SSG, Vega

VR content creation  
Graphics rendering

## **Consumer Graphics**

- Radeon Rx Vega64, Vega56

Gaming, AR/VR



## **Datacenter** (Acceleration, AI/ML)

- Nervana Neural Net Processor
- Stratix10 MX (FPGA)

ASIC

FPGA



## **Consumer Graphics**

- KabyLake-G

CPU/GPU Hybrid



H/E GFX in notebooks  
Thin/light  
Extended battery life



## **Datacenter** (Acceleration, AI/ML)

- TPU2

Cloud TPU for Training  
& Inference

TPU2: 4 ASICs, 64GB HBM2

TPU POD: 4TB HBM2

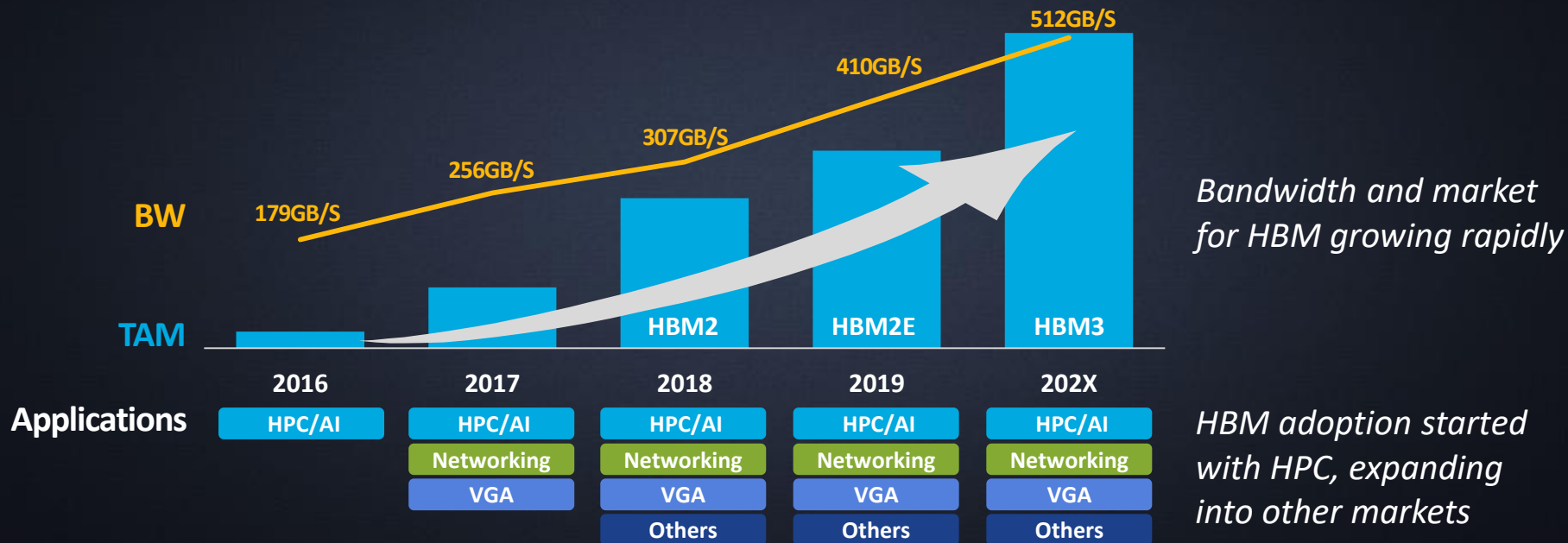


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Sources: Tom's Hardware, Anandtech, PC World, Trusted Reviews

# HBM2: Market Outlook

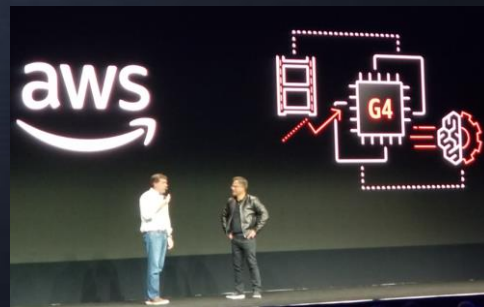
- Bandwidth needs of High-Performance Computing/AI, High-end Graphics, and new applications continue to expand





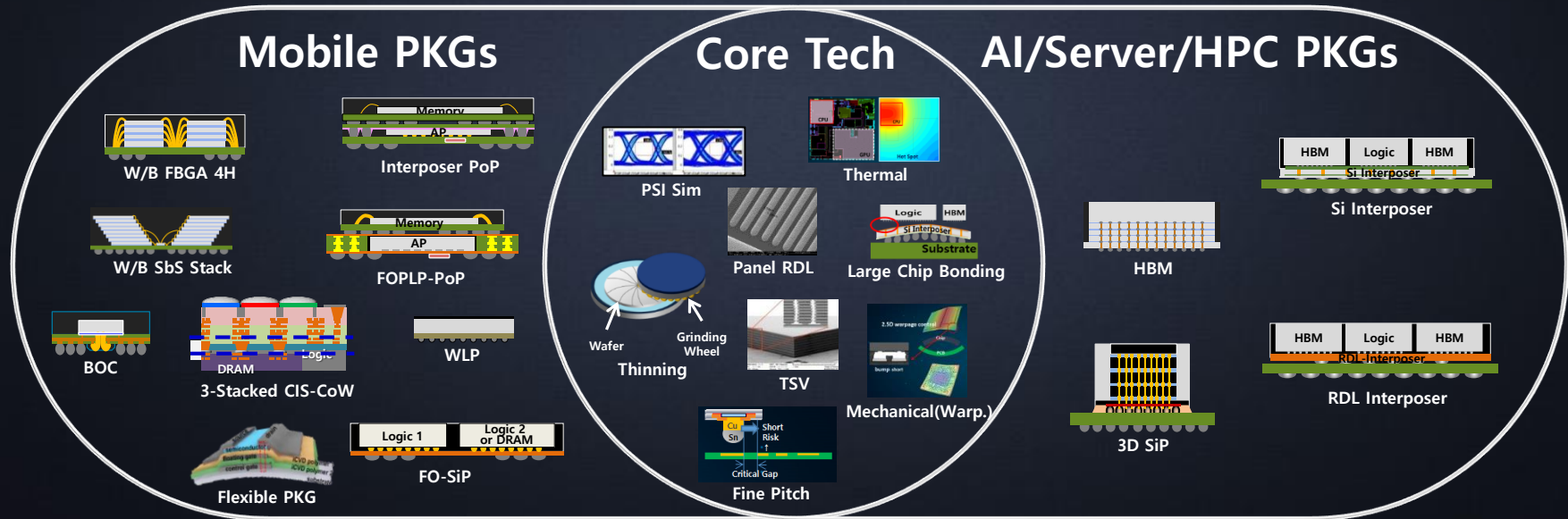
# AI Inference: GDDR6

- Inference less computationally & memory intensive than AI Training
- GDDR6 is a good option – double the bandwidth of GDDR5
  - Up to 16Gbps per pin → 64GB/s per device
- Samsung is first to market with 16Gb GDDR6
- Nvidia T4 cards
  - 16GB GDDR6
  - AWS G4 Inference



# Foundry Services

- Latest process nodes, testing, packaging, design services
- WW partners to complement solutions with IP and EDA tools



# Summary

- AI workloads rely on Deep Learning algorithms that are memory bandwidth constrained
- HBM has become the memory of choice for AI training applications in the data center
- GDDR6 provides an “off-the-shelf” alternative for AI inference workloads

**Make the smart choice: AI hardware powered by these technologies**

# Thank You...

A promotional banner for the Samsung GPU Technology Conference. The background is a dark blue server room with glowing lights and motion blur. The text is white and centered on the left side. In the top right corner, there are three links: REGISTER, SPEAKERS, and CONTACT. In the bottom right corner, there is a logo for the GPU Technology Conference.

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