

# NVIDIA Tegra K1 Embedded Platform Design Guide

### Abstract

This document contains recommendations and guidelines for engineers to follow to create a product that is optimized to achieve the best performance from the common interfaces supported by NVIDIA<sup>®</sup> Tegra<sup>®</sup> K1 series processors.

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# 1.0 Introduction

# 1.1 Abbreviations and Definitions

The following table lists abbreviations that may be used throughout this document and their definitions.

Abbreviation	Definition
BT	Bluetooth
CEC	Consumer Electronic Control
DDR3L	Double Data Rate DRAM, Third-generation
eMMC	Embedded MMC
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
HDMI	High Definition Multimedia Interface
HSIC	High Speed Inter Chip Interface
12C	Inter IC
125	Inter IC Sound Interface
КВС	Keyboard Controller
LCD	Liquid Crystal Display
LDO	Low Dropout (voltage regulator)
LVDS	Low Voltage Differential Signaling Interface
MMC	Multi-Media Card / High Speed MMC
PCIe	Peripheral Component Interconnect Express interface
PCM	Pulse Code Modulation
РНҮ	Physical Interface (i.e. USB PHY)
РМС	Power Management Controller
PMU	Power Management Unit
RF	Radio Frequency
RTC	Real Time Clock
SATA	Serial "AT" Attachment interface
SDIO	Secure Digital I/O Interface
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver-Transmitter
ULPI	UTMI+ Low Pin-count Interface
USB	Universal Serial Bus
WLAN	Wireless Local Area Network

### Table 1. Abbreviations and Definitions



### 1.2 Overview

The Jetson platform is based on the NVIDIA<sup>®</sup> Tegra<sup>®</sup> K1 application processor, which is a revolutionary step in the world of mobile computing. With Tegra K1, NVIDIA integrated its mobile version of the Kepler GPU architecture that powers the highest performing graphics cards and systems in the world. By optimizing this industry acclaimed graphics architecture for extremely low power use cases needed for mobile devices, Tegra K1 processors are first to offer features like OpenGL<sup>®</sup> 4.4, DirectX<sup>®</sup> 11.1 and CUDA/GPGPU. This high performance applications processor, coupled with the unique Tegra 4-PLUS-1<sup>™</sup> architecture, DirectTouch<sup>™</sup>, and PRISM2<sup>™</sup> technologies, is the foundation for next generation devices that enable visual computing in mobile devices.



# 1.3 Tegra K1 Block Diagram



# 2.0 Power

### Figure 1. TK1 Embedded Power Tree (Jetson TK1 Platform Example)





### 2.1.1 Supply Details

The table below shows the allocation of supplies used in the Jetson TK1 platform design & available for use in Embedded designs.

Power Rails	Usage	(V)	Power Supply or Gate	Source	Enable	Time (ms)	Notes
+VDD_MUX	Main power - Supplies PMU & various external supplies	12	na	Power Jack	na		
+5V_SYS	Main 5V supply.	5.0	TPS51220 Switcher	+VDD_MUX	PMU EN5V	0	
+3.3V_SYS	Main 3.3V supply	3.3	TPS51220 Switcher	+VDD_MUX	PMU GPIO2	0	
+3.3V_LP0	Gated 3.3V supply. On in D.Sleep.	3.3	SLG5NV-1430V Gate	+3.3V_SYS	REGEN1	7	1
+3.3V_RUN	Gated 3.3V supply. Off in D.Sleep.	3.3	SLG5NV-1430V Gate	+3.3V_SYS	REGEN3	10	2
+VDD_CORE	Tegra VDD_CORE rail	Var.	AS3728 PWR Stage (SD1, x1)	+5V_SYS	PMU GPIO	2	
+VDD_CPU	Tegra main CPU complex	Var.	AS3728 PWR Stage (SD0, x2)	+5V_SYS	PMU GPIO	Off	
+VDD_GPU	Tegra GPU	Var.	AS3728 PWR Stage (SD6, x2)	+5V_SYS	PMU GPIO	Off	
+1.35V_LP0	DDR3L rails (Tegra & DDR)	1.35	PMU Switcher SD2/3	+5V_SYS	Pwr-on Seq	8	
+1.05_RUN	HDMI & PEX/USB 1.05 rails	1.05	PMU Switcher SD4	+5V_SYS	I2C/PMU	Off	3,6
+1.8V_VDDIO	Main 1.8V supply.	1.8	PMU Switcher SD5	+5V_SYS	Pwr-on Seq	7	4
+1.05_RUN_AVDD	Tegra 1.05V PLLs & LVDS I/O rails.	1.05	PMU LDO 0	VDD_1V35	Pwr-on Seq	9	5
+1.8V_RUN_CAM	Camera 1.8V rail	1.8	PMU LDO 1	+3.3V_RUN	I2C/PMU	Off	
+1.2V_GEN_AVDD	Tegra AVDD_DSI_CSI, VDDIO_HSIC	1.2	PMU LDO 2	+1.8V_VDDIO	I2C/PMU	Off	6
+1.05V_LP0_VDD_RTC	Tegra VDD_RTC	Var.	PMU LDO 3	+1.35V_LP0, +VDD_CORE or +3.3V_SYS	Pwr-on Seq	1	
+2.8V_RUN_CAM	High voltage Camera rail(s)	2.8	PMU LDO 4	+3.3V_SYS	I2C/PMU	Off	
+1.2V_RUN_CAM_FRON T	Front Camera 1.2V rail	1.2	PMU LDO 5	+1.8V_VDDIO	I2C/PMU	Off	
+VDDIO_SDMMC3	Tegra SD Card rail	1.8/3. 3	PMU LDO 6	+3.3V_RUN	I2C/PMU	Off	
+1.05V_RUN_CAM_REA R	Rear camera 1.05V supply	1.05	PMU LDO 7	+1.8V_VDDIO	I2C/PMU	Off	
+3.3V_RUN_TOUCH	High voltage touch rail	3.3	PMU LDO 9	+5V_SYS	I2C/PMU	Off	
+2.8V_RUN_CAM_AF	Camera autofocus rail	2.8	PMU LDO 10	+5V_SYS	I2C/PMU	Off	
+1.8V_RUN_VPP_FUSE	Tegra VPP_FUSE rail	1.8	PMU LDO 11	+3.3V_RUN	I2C/PMU	Off	7
+3.3V_AVDD_HDMI_AP_GATE D	Tegra 3.3V HDMI rail	3.3	Dual FET backdrive prevention	+3.3V_RUN	+1.05_RU N	10	
+1.05V_RUN_AVDD_	Tegra AVDD_HDMI_PLL	1.05 or	Dual FETs as load	+1.05V_RUN (1.05V)	Tegra GPIO	OFF	6

### Table 2 Power Supply Allocation



Power Rails	Usage	(V)	Power Supply or Gate	Source	Enable	Time (ms)	Notes
HDMI_PLL_AP_GATE		1.2	switch	+1.2V_GEN_AVDD (1.2V)			
+VDD_1V5_MPCIE	1.5V Mini-PCIe supply	1.5	APL5910 LDO	+5V_SYS	+3.3V_LP 0	7	
+5V_USB_HS	VBUS: USB 3.0 Type A #1	5.0	TPS2065 Load SW	+5V_SYS	Tegra GPIO	Off	
+USB0_VBUS_SW	VBUS: USB 2.0 Micro AB	5.0	TPS2065 Load SW	+5V_SYS	Tegra GPIO	Off	
+5V_HDMI_CON	5V to HDMI conn.	5.0	TPS2553DRV Load SW	+5V_SYS	Tegra GPIO	Off	
+3.3V_SD_CARD	SD Card socket rail	3.3	TPS2553DRV Load SW	+3.3V_SYS	Tegra GPIO	Off	
+5V_SATA	SATA connector rail	5.0	SLG5NV-1430V Gate	+5V_SYS	Tegra GPIO	Off	

Notes: 1. Includes AVDD\_USB, VDDIO\_HV, HVDD\_PEX, HVDD\_PEX\_PLL\_E, VDDIO\_PEX\_CTL

2. Includes AVDD\_LVDS0\_PLL.

3. Includes AVDDIO\_PEX, AVDD\_PEX\_PLL, DVDDIO\_PEX (source for FETs to AVDD\_HDMI\_PLL)

4. Includes AVDD\_OSC, AVDD\_PLL\_UTMIP, VDDIO\_SYS, VDDIO\_SYS2, VDDIO\_BB, VDDIO\_SDMMC1, VDDIO\_SDMMC4, VDDIO\_AUDIO, VDDIO\_UART, VDDIO\_CAM & VDDIO\_GMI

5. Includes AVDD\_PLL\_UD2DPD, AVDD\_PLL\_C4, AVDD\_PLL\_CG, AVDD\_PLL\_X, AVDD\_PLL\_APC2C3, AVDD\_LVDSO\_IO, AVDD\_PLL\_X, AVDD\_PLL\_EREFE

6. The supply for AVDD\_HDMI\_PLL must have a discharge circuit. The PMU Switchers have this feature, but since an external load switch is used, ensure it has a discharge circuit.

7. Initial designs should include series  $0\Omega$  resistor between VPP\_FUSE supply & Tegra to allow current measurements during Fuse Audit.



# 2.2 CPU, GPU, CORE & DDR Supply Considerations

The total power solution for the CPU, GPU, CORE & DDR supplies must meet the requirements listed in the Tegra K1 Data Sheet including:

- Voltage steps required by DVFS software
- Maximum EDP current
- Minimum voltage ramp rates

In addition, in order to meet the full EDP max current, care must be taken in selecting the critical components that make up each supply circuit. These components, including the PMU switcher or external regulators must meet the current requirements and the +/- 7% maximum tolerance allowed at the Tegra power balls including supply DC tolerance, ripple & voltage transients (variations in voltage caused by changes in load).

Impedance simulations should use all the output capacitors (large capacitor[s] just beyond DC-DC inductor), as source, and all the power pins as sinks.

### 2.2.1 Power Impedance Specifications



Figure 2. Target Impedance Definitions for PCBs

DCR: DC Resistance Z<sub>BRD\_</sub>RES\_Target: Max impedance at resonance peaks below 10MHz Z<sub>BRD\_</sub>HF\_target: Max impedance at 100MHz. This specifies the inductance limit of current path to high performance ceramic capacitors

Table 3	CPU, GPU,	CORE &	DDR Power	Impedance	Specification
---------	-----------	--------	-----------	-----------	---------------

	VDD_CORE	VDD_CPU	VDD_GPU	VDD_DDR <sup>1</sup>	Comments
DCR (mΩ)	13.3	13.5	11.2	11.0	
ZBRD_RES_Target (mΩ)	12.5	7.2	7.7	11.0	Resonance Peak Impedance <10MHz
Z <sub>BRD</sub> _HF_Target (mΩ)	82.5	105.2	108.6	120.0	@ 100MHz

Note: 1. VDD\_DDR includes Tegra VDDIO\_DDR & DRAM supplies for full 64-bit memory interface.

The components shown in the tables on the following pages were selected to meet the above voltage tolerance requirements for each supply. In addition to actual part numbers, critical parameters & values for the components are listed. These should be taken into consideration if different components are used. It is important to work closely with the power supply vendor to ensure that any components selected meet the voltage/current requirements of the supply and Tegra. Impedance simulations should use all the output capacitors (large capacitor[s] just beyond DC-DC inductor), as source, and all the power pins as sinks.



### Table 4 Critical VDD\_CPU Switcher Components Recommendations (Three Power Stages)

Components	MFG	MFG Part #	Qty	Parameter	Symbol	Conditions	Value	Units
PMIC (CtrIr)	AMS	AS3722	1	Switching Frequency	f		1.35	MHz
2 phase per Pwr Stage	AMS	AS3728	3	Max Current	1		2x10	A
Inductor	TDK	SPM4015-R68M	6	Inductance	L		0.68	uH
				DC Resistance	DCR		32.7	mΩ
				Size	LxWxH		4.4x4.1x1.5	mm
				RMS Current	Irms	40C rise	4.7	А
		Saturation Current	Isat	30% drop	8	А		
Output Ta	Taiyo	JMK212BJ476MG-T	4 per Power Stage)	Data Sheet Capacitance	С		47	uF
Capacitor	ruden			Size	LxW		0805	mm
				Dielectric			X5R	Code
				Rated Voltage	V		6.3	V
Input	Taiyo	TMK316BJ106KD-TD	4 per Power	Data Sheet Capacitance	С		10	uF
Capacitor	ruden		stage)	Size	LxW		3.5	mm
				Dielectric			X5R	Code
				Rated Voltage	V		25	V
PCB Routing							TBD	mΩ

### Table 5 Critical VDD\_GPU Switcher Components Recommendations (Two Power Stages)

Components	MFG	MFG Part #	Qty	Parameter	Symbol	Conditions	Value	Units
PMIC (Ctrlr)	AMS	AS3722	1	Switching Frequency	f		1.35	MHz
2 phase per Pwr Stage	AMS	AS3728	2	Max Current	I		10	A
Inductor	TDK	SPM4015-R68M	4	Inductance	L		0.68	uH
				DC Resistance	DCR		32.7	mΩ
				Size	LxWxH		4.4x4.1x1.5	mm
			RMS Current	Irms	40C rise	4.7	А	
			Saturation Current	Isat	30% drop	8	А	
Output	Output Taiyo JMK212BJ476MG-T	3 per Power	Data Sheet Capacitance	С		47	uF	
Capacitor	ruuen		Staye)	Size	LxW		0805	mm
				Dielectric			X5R	Code
				Rated Voltage	V		6.3	V
Input	Taiyo	TMK316BJ106KD-TD	4 per Power	Data Sheet Capacitance	С		10	uF
Сарасної	ruden		stage)	Size	LxW		1206	mm
				Dielectric			X5R	Code
				Rated Voltage	V		25	V
PCB Routing							TBD	mΩ



### Table 6 Critical VDD\_CORE Switcher Components Recommendations (One Power Stage)

Components	MFG	MFG Part #	Qty	Parameter	Symbol	Conditions	Value	Units
PMIC (CtrIr)	AMS	AS3722	1	Switching Frequency	f		1.35	MHz
2 phase per Pwr Stage	AMS	AS3728	1	Max Current	I		10	A
Inductor	TDK	SPM4015-R68M	2	Inductance	L		0.68	uH
				DC Resistance	DCR		32.7	mΩ
				Size	LxWxH		4.4x4.1x1.5	mm
				RMS Current	Irms	40C rise	4.7	А
			Saturation Current	Isat	30% drop	8	А	
Output Capacitor	Taiyo Yuden	JMK212BJ476MG-T	3	Data Sheet Capacitance	С		47	uF
				Size	LxW		0805	mm
				Dielectric			X5R	Code
				Rated Voltage	v		6.3	v
Input	Taiyo	TMK316BJ106KD-TD	4	Data Sheet Capacitance	С		10	uF
Сарасної	ruuen			Size	LxW		1206	mm
				Dielectric			X5R	Code
				Rated Voltage	V		25	v
PCB Routing							TBD	mΩ

### Table 7. Basic Tegra Power Control Connections

Ball Name	Туре	Termination (typical)	Description
CLK_32K_IN	I		<b>32.768kHz Clock</b> : input for 32kHz clock used by RTC & PMC blocks
SYS_RESET_N	Ι		System Reset: Reset input for Tegra
PWR_I2C_SCL/SDA	O/B	1K $\Omega$ pull-up resistor to VDDIO_SYS.	Power I2C: Connect to PMU.
CORE_PWR_REQ	0		Core Power Request: Connect to CORE_PWRREQ on PMU
CPU_PWR_REQ	0		CPU Power Request: Connect to CPU_PWRREQ on PMU
PWR_INT	I		Power Interrupt: Connect to XINT pin on PMU



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Table 8. Recommended States for Tegra Power Rails (Typical grouping shown)

Power Rail	Voltage (V)	Early Power-on	For Boot	Deep Sleep	Notes
VDD_CORE	Variable	ON	ON	OFF	
VDD_CPU & VDD_GPU	Variable	OFF	OFF	OFF	
VDD_RTC	Variable	ON	ON	ON	
AVDD_OSC/PLL_UTMIP, VDDIO_SYS/SYS2/AUDIO/UART/SDMMC1/SDMMC4, VDDIO_CAM/BB/GMI	1.8	ON	ON	ON	1, 2
VDDIO_DDR	1.2/1.35	OFF	ON	ON	3
AVDD_PLL_x, VDDIO_DDR_HS	1.05	ON	ON	OFF	
AVDD_HDMI_PLL, DVDDIO_PEX, AVDDIO_PEX, AVDD_PEX_PLL, VDDIO_SATA, AVDD_SATA_PLL	1.05	OFF	OFF	OFF	4, 5
AVDD_CSI_DSI, VDDIO_HSIC	1.2	OFF	OFF	On	6
AVDD_HDMI	3.3	OFF	OFF	OFF	7
AVDD_USB, HVDD_PEX, HVDD_PEX_PLL_E, VDDIO_HV, VDDIO_PEX_CTL	3.3	See Notes	See Notes	See Notes	4, 5
VDDIO_SDMMC3	1.8/2.8- 3.3	OFF	OFF	OFF	
VPP_FUSE	1.8	OFF	OFF	OFF	3, 8

Note: 1. Rail must be on in Deep Sleep if any of the Wake capable pins on these blocks are used for wake

- VDDIO\_AUDIO/UART/SDMMC1/SDMMC4/BB are typically combined with other 1.8V rails, such as AVDD\_OSC & VDDIO\_SYS/SYS2, so would be ON in all three modes shown. If they come from a separate supply, they are not required to be on unless any pins are used for wake or pulled/driven high in Deep Sleep mode.
   Do not negative supply they are not required to be on unless any pins are used for wake or pulled/driven high in Deep Sleep mode.
- 3. Do not power until SYS\_RESET\_N is asserted & VDD\_RTC / VDD\_CORE have reached their nominal level. Violating this constraint may permanently damage Tegra.
- 4. **AVDD\_USB** Required for "Boot" for Force Recovery Mode.
- If USB 2.0 Wake (Using USB mechanisms) is required, AVDD\_USB must be powered. If USB 3.0 Wake on USB3\_TXx/RXx (Using USB mechanisms) is required for connected USB 3.0 devices, HVDD\_PEX must be powered in Deep Sleep. AVDDIO\_PEX & AVDD\_PEX\_PLL do not need to be powered & are recommended to be off in Deep Sleep
- 6. VDDIO\_HSIC must be on in Deep Sleep if used for Modem or possibly WiFi & connection must be maintained
- 7. AVDD\_HDMI must be off in Deep Sleep to pass Voff compliance. Do not combine with 3.3V rails that need to be on.
- 8. VPP\_FUSE must be off in Deep Sleep or damage can occur. This rail should be off at all times unless actively being used to burn fuses.



### 2.2.2 Power Sequencing

### Figure 3. Power-up Sequence



- Notes: +1.8V\_VDDIO Includes: AVDD\_OSC/PLL\_UTMIP/LVDS0\_PLL & VDDIO\_SYS/SYS2/BB/SDMMC1/SDMMC4/AUDIO/UART/GMI - 1.05V\_RUN\_AVDD Includes: AVDD\_PLL\_UD2DPD/PLL\_C4/PLL\_CG/PLL\_X/PLL\_APC2C3/LVDS0\_IO/PLL\_X/PLL\_EREFE.
  - Critical relationships:
    - Tegra VDD\_RTC (+1.05V\_LP0\_VDD\_RTC) & VDD\_CORE (+VDD\_CORE) must be valid before other Tegra rails
    - Tegra VDDIO\_SYS/SYS2 (+1.8V\_VDDIO) must be valid before other Tegra I/O rails.
    - All rails required for boot, 32KHz clock & OSC (System Clock) must be valid before SYS\_RESET\_N goes high.
    - See Tegra K1 Series Data Sheet for more details on power sequencing.

# 2.3 Power Decoupling Guidelines

See Checklist table at end of document for Decoupling requirements.

# 2.4 Decoupling Capacitor Placement

For VDD\_CPU/GPU/CORE, VDDIO\_DDR & DRAM power rails, use areas on multiple layers to reduce the routing resistance from supply to power balls. See the figures in this section for examples.

General Power Routing Guidelines

- Route power using thick areas, duplicated on multiple layers where possible.
- Minimize distance from supply to destination.
- Connect overlapping areas on different layers with multiple vias to reduce resistance/impedance.

### 2.4.1 CPU, GPU, CORE & DRAM Routing & Decoupling Placement

Tegra decoupling capacitors should be placed on the bottom, just below the power ball arrays. For DRAM decoupling, they can be below the power balls, or next to the power balls on the same side of the PCB. Use 35-40 mil width traces from the balls to the decoupling capacitors. Make sure that the 35-40 mils shape has a GND references on the adjacent layer.



Figure 4. CPU, CORE, GPU & DRAM Inner Layer Main Power Routing



Figure 5. CPU, GPU, CORE & DRAM Decoupling Capacitor Placement



Note: Decoupling capacitors located on the bottom of the PCB, just below the power balls they are associated with.

### Figure 6. DRAM Decoupling Capacitor Placement



# 2.5 Remote Power Sense Guidelines

Tegra processors support remote power sense functionality for the VDD\_CPU, VDD\_CORE & VDD\_GPU rails. For each of the rails there is a positive (SENSE+) & negative (SENSE-) line.

- VDD\_CPU\_SENSE & GND\_CPU\_SENSE
- VDD\_CORE\_SENSE & GND\_CORE\_SENSE
- VDD\_GPU\_SENSE & GND\_GPU\_SENSE



The SENSE+ balls are routed on the Tegra package/die to power rail locations near each load & to provide feedback to the PMU/Regulators so they can adjust to any voltage variances. The SENSE- balls are routed on the Tegra package/die to GND locations near each load.

General Guidelines:

- Keep Sense lines away from noisy components (such as power inductors) and noisy signal traces
- Do not route Sense lines directly under or over noisy power rails.
- Route Sense lines with GND reference plane. If possible, route GND traces on either side of the Sense pairs

Tahlo 0	General	Power	Sonco	Pouting	Guidalinas
Table 9.	General	Power	Sense	Routing	Guidennes

Parameter	Requirement	Notes
Topology	Point to Point	
Number of loads	1 load	
Reference plane	GND where possible	
Trace Routing	Route as pseudo differential pair with min 4/4/4 trace widths/spacing	
Max Trace Delay	As short as possible	
Trace Spacing (to other nets)	3x dielectric	

Note: - Strongly recommend review of sense line routing & other critical items related to VDD\_CPU/GPU/CORE supplies by PMU/Regulator vendor

### 2.5.1 Thermal throttling (SOC\_THERM)

Tegra has external over-current (OC) detection mechanisms to monitor devices outside Tegra, (such as PMIC, battery, on-board power sensors) and provide OC alarms signals to Tegra. These are routed to SOC\_THERM to throttle the system in these events and are available on the following pins, which are followed by typical usage.

SOC_THERM Pin		Typical Usage
KB_ROW15	Single-Cell Designs Dual-Cell Designs	Battery Voltage (VDD_SYS) Monitor GPU Power/Thermal Events
GPIO_PK0		Modem Power Report
GPIO_PJ2		Power Monitor Output
CLK_32K_OUT		CPU Power/Thermal Events (may be covered by Power Monitor instead, or in addition to this SOC_THERM)

# 2.6 5V Input Considerations

For designs that choose to use 5V input instead of 12V a power & voltage monitor are highly recommended to monitor and alert the system software of potential issues that could cause the supply to drop below acceptable levels.



### 2.6.1 Power Monitor

A Power Monitor, such as shown below, is highly recommended where Tegra is used in a 5V design.





Note: In order to support short and long-term average power limiting thru the Power Monitor, the CRIT & WARN pins should be tied together and routed to the SOC\_THERM input, GPIO\_PJ2

### 2.6.2 Voltage Monitor

For 5V input design, a voltage monitor should be connected to the VSYS rail that supplies the system PMIC and other components requiring the VSYS level input. This device will generate an alert quickly, if the rail "droops" below an acceptable level. The voltage monitor circuit is implemented with a fast voltage comparator supplied by VDD\_SYS (Battery/Charger level) with a 1.8V (VDD\_1V8) reference common with the Tegra IO domain that receives the output signal. The particular part selected is an OnSemi NCS2202SQST2G. This device has an open drain active low output which is pulled low when the VDD\_SYS voltage drops below the selected threshold. The open drain output is pulled up by an internal pull-up resistor on the Tegra KB\_ROW15 pin.

### Figure 8. Voltage Monitor Connections



### **Threshold Selection**

The exact threshold target for the circuit is dependent on the specific system characteristics. There are a number of contributors to the ESR (resistance) of the system from the battery to the input of the system PMU. A higher system ESR will result in a higher IR drop for a specific current level for a specific total amount of power being consumed from the battery.

The voltage threshold should be set based on the minimum system voltage plus a voltage delta. This voltage delta represents the maximum droop below the voltage comparator threshold that is expected for high transient workloads, possibly concurrent with modem transmit cycles.



# 2.7 Deep Sleep Wake Considerations

Certain events are required to generate a wake condition. This can vary depending on Operation System. Check to see which of the signals in the table below are required as wake events. The wake pins used in the Jetson TK1 reference design are indicated.

### Table 10. Signal Wake Events

Potential Wake Event	Tegra Ball Assigned
Touch Screen Interrupt	GPIO_W3_AUD
Modem to AP Wake	GPIO_PV0
Battery Charger Interrupt	GPIO_PJ0
System Overcurrent Alert	GPIO_PJ2
Skin Temperature Alert	GPIO_PI6
PCIe Wake	PEX_WAKE_N
Power Button	KB_COLO
GPU Overcurrent Interrupt	KB_ROW15
Headphone Insertion Detection	KB_ROW7 / Audio Codec pin
SD Card Card Detect	SDMMC3_CD_N
PMIC Interrupt to AP	PWR_INT_N
Low Battery Alert	KB_COL5
Wi-Fi Interrupt	GPIO_PU5
Available Bluetooth Interrupt	GPIO_PU6
HDMI Hot Plug Detect	HDMI_INT
HDMI Consumer Electronic Control	HDMI_CEC

# 2.8 General Power Routing Guideline

Avoid routing critical signals near power components or noisy power traces/areas, whether on the same layer, or above/below the components or power traces/areas.



# 3.0 Interface Routing Guidelines

### 3.1 Overview

This chapter contains the PCB routing and other guidelines for the following Tegra interfaces

Clocks	DSI	SDMMC	Strapping Pins
DRAM	LVDS	125	Thermal Diode
USB	eDP	12C	
PCIe	HDMI	SPI	
SATA	CSI	UART	
HSIC	DTV	JTAG	

Note: - Unless otherwise noted, all resistor values are ±5% & trace impedance values are ±15%

### Signal Name Conventions

The following conventions are used in describing the signals for Tegra:

- Signal names use a mnemonic to represent the function of the signal (i.e. Secure Digital Interface #3 CMD signal is SDMMC3\_CMD), written in bold to distinguish it from other text. Active low signals usually have an underscore followed by capital N (\_N) after the name (i.e. SYS\_RESET\_N). Differential signals are identified as a pair with the same names that end with \_P and \_N or just P and N (for positive and negative, respectively). For example, USB1\_DP and USB1\_DN indicate a differential signal pair.
- I/O Type The signal I/O type is represented as a code to indicate the operational characteristics of the signal. The table below lists the I/O codes used in the signal description tables.

Code	Definition
A	Analog
DIFF I/O	Bidirectional Differential Input/Output
DIFF IN	Differential Input
DIFF OUT	Differential Output
1/0	Bidirectional Input/Output
I	Input
0	Output
OD	Open Drain Output
I/OD	Bidirectional Input / Open Drain Output
Р	Power

### Table 11. Signal Type Codes

General SFIO (Special Function IO) & GPIO (General Purpose IO) selection.

 The SFIO and GPIO usage should match those used on Jetson TK1, or alternative "Use-case" options shown in the Jetson TK1 Pinmux spreadsheet.

### **Routing Guideline Format**

The routing guidelines have the following format to specify how a signal should be routed.

- Breakout traces are traces routed from BGA ball either to a point beyond the ball array, or to another layer where full normal spacing guidelines can be met. Breakout trace delay limited to 500 mils unless otherwise specified.
- After breakout, signal should be routed according to specified impedance for differential, single-ended, or both (for example: HDMI). Trace spacing to other signals also specified.



- Follow max & min trace delays where specified. Trace delays are typically shown in mm or in terms of signal delay in pico-seconds (ps) or both.
  - For differential signals, trace spacing to other signals must be larger of specified × dielectric height or inter-pair spacing
  - Spacing to other signals/pairs cannot be smaller than spacing between complementary signals (intrapair).
  - Total trace delay depends on signal velocity which is different between outer (microstrip) & inner (stripline) layers of a PCB.

### Signal Routing Conventions

Throughout this document, the following signal routing conventions are used:

SE Impedance (/ Diff Impedance) at x Dielectric Height Spacing

- Single-ended (SE) impedance of trace (along with differential impedance for diff pairs) is achieved by spacing requirement. Spacing is multiple of dielectric height. Dielectric height is typically different for microstrip & stripline. Note: 1 mil = 1/1000th of an inch.
- Note: Trace spacing requirement applies to SE traces or differential pairs to other SE traces or differential pairs. It does not apply to traces making up a differential pair. For this case, spacing/trace widths are chosen to meet differential impedance requirement.

### General Routing Guidelines

Pay close attention when routing high speed interfaces, such as DDR3L/LPDDR3, HDMI, USB/HSIC or DSI/CSI. Each of these interfaces has strict routing rules for the trace impedance, width, spacing, total delay, and delay/flight time matching. The following guidelines provide an overview of the routing guidelines and notations used in this document.

### Controlled Impedance

Each interface has different trace impedance requirements & spacing to other traces. It is up to designer to calculate trace width & spacing required to achieve specified single-ended (SE) & differential (Diff) impedances.

Max Trace Lengths/Delays

Trace lengths/delays should include main PCB routing (where Tegra resides) and any additional routing on a Flex/ secondary PCB segment connected to main PCB. The max length/delay should be from Tegra to the actual connector (i.e. USB, HDMI, SD Card, etc.) or device (i.e. onboard USB device, Display driver IC, camera imager IC, etc.)

### Trace Delay/Flight Time Matching

Signal flight time is the time it takes for a signal to propagate from one end (driver) to other end (receiver). One way to get same flight time for signal within signal group is to match trace lengths within specified delay in the signal group.

- Except for DRAM or if otherwise stated, always include Tegra substrate trace delay or propagation delay in all trace delay or flight-time matching calculations.
- Total trace delay = substrate trace delay + board trace delay. Do not exceed maximum trace delay specified.
- For six layers or more, it is recommended to match trace delays based on flight time of signals. For example, outer-layer signal velocity could be 150psi (ps/inch) & inner-layer 180psi. If one signal is routed 10 inches on outer layer & second signal is routed 10 inches in inner layer, difference in flight time between two signals will be 300ps! That is a big difference if required matching is 15ps (trace delay matching). To fix this, inner trace needs to be 1.7 inches shorter or outer trace needs to be 2 inches longer.
- In this design guide, terms such as intra-pair & inter-pair are used when describing differential pair delay. Intra-pair refers to matching traces within differential pair (for example, true to complement trace matching). Inter-pair matching refers to matching differential pairs average delays to other differential pairs average delays.



### **General PCB Routing Guidelines**

For GSSG stackup to minimize crosstalk, signal should be routed in such a way that they are not on top of each other in two routing layers (see diagram to right)	G S G G
Do not route other signals or power traces/areas directly under or over critical high-speed interface signals.	

# 3.2 Clocks

Туре	Clock	Description / Typical Use	Source	Tegra Pin	Power Rail
Input	32kHz	32.768kHz clock. Used by PMC	PMU	CLK_32K_IN	VDDIO_SYS/SYS2
Internal	OSC	Oscillator. Main Tegra clock source	XTAL or External	XTAL_IN/OUT XTAL_OUT only	AVDD_OSC /VDDIO_SYS/SYS2
Internal	PLLA, PLLP, PLLC2, PLLC3	PLLA Used for Audio. PLLP used for a variety of peripheral blocks. PLLC2/C3 are multi-purpose PLLs	OSC		AVDD_PLL_APC2C3
Internal	PLLC, PLLG	PLLG used for Graphics Engine. PLLC is a multi- purpose PLL	OSC		AVDD_PLL_CG
Internal	PLLU, PLLD, PLLD2, PLLDP	PLLU used for USB 2.0. PLLD/D2 used for Display & MIPI (DSI & CSI). PLLDP used for eDP.	OSC		AVDD_PLL_UD2DPD
Internal	PLLM	Typically used for DRAM controller	OSC		AVDD_PLLM
Internal	PLLC4		OSC		AVDD_PLL_C4
Internal	PLLX	Used for CPU	OSC		AVDD_PLLX
Internal	PLLE, PLL_REFE	Used for USB3, PCIe & SATA blocks	OSC		AVDD_PLL_EREFE
Internal	PEX_PLL	Used for USB3/PCIe PHYs	OSC		AVDD_PEX_PLL
Internal	SATA_PLL	Used for SATA PHY	OSC		AVDD_SATA_PLL
Output	VIMCLK	Used for Camera 1 master reference clock.	Various	CAM_MCLK	VDDIO_CAM
Output	VIMCLK2	Used for Camera 2 master reference clock.	Various	GPIO_PBB0	VDDIO_CAM
Output	EXTPERIPH1_CLK	Used for Audio MCLK, etc.	Various	DAP_MCLK1	VDDIO_AUDIO
Output	EXTPERIPH2_CLK	Used for Touchscreen Clock, etc.	Various	CLK2_OUT	VDDIO_SDMMC1
Output	EXTPERIPH3_CLK	General purpose clock output	Various	CLK3_OUT	VDDIO_UART

### Table 12. Tegra Clock Input & General Output Tree

Figure 9. Tegra External Clocking Block Diagram



# 3.2.1 Oscillator & PLL Power Routing

The routing requirements in the table below apply to the following critical clock power rails:

- AVDD\_OSC, AVDD\_HDMI\_PLL
- AVDD\_PLL\_APC2C3, AVDD\_PLL\_X, AVDD\_PLL\_M, AVDD\_PLL\_UTMIP, AVDD\_PLL\_C4, AVDD\_PLL\_CG, AVDD\_PLL\_EREFE, AVDD\_PLL\_UD2DPD



Table 13. Clock Power Routing Requirements

Parameter	Requirement	Units	Notes
Reference plane	GND if possible		See note 1
Trace Spacing	3х	Dielectric	
Max Trace Delay	Minimum		See note 3

- Note: If GND reference is not feasible, as may be the case with GSSG stack-up, keep the routing distance very short and have GND areas/traces next to the rails.
  - Use reference platform layout as a guideline for routing & location of bypass capacitors & filters.
  - Avoid routing signal traces or other power traces/areas directly above/below or in parallel with these critical rails.

### 3.2.2 Additional PLL Power Noise Coupling Reduction Guidelines

Table 14.	PLL Power	& I/O Power	Via Coupling	Requirements

PLL PWR Via Victim	PLL Power Rail Via Aggressor	Minimum Distance (Via center to via center)	PCB Height	Other Requirements
PLLM PWR, Pin K16	+1.35V_LP0_VDDIO_DDR_AP	1.3 mm	<= 40mil	
PLLM PWR, Pin K16	+1.35V_LP0_VDDIO_DDR_AP	1.5 mm	>= 40mil	
PLLA, PLLP, PLLC2, PLLC3 PWR, Pin B17	+1.05V_DDR_AVDD, Pin A17	1.1 mm	ALL (PWR pins on edge of die to less constraints)	GND via must be placed in between two Power VIAS

Table 15. PLL Power Trace to Power Plane Broadside Coupling Requirements

PLL PWR Via Victim	PLL Power Rail Trace Aggressor	Routing Restriction	
PLLM & PLLAPC2C3 PWR Trace	+1.8V (I/O Power) & 1.35V (I/O Power)	PLL power trace not allowed directly below or above the I/O power plane to avoid broadside coupling.	

### 3.2.3 32.768kHz Clock

The 32.768kHz clock is provided by the PMU. This clock is input on the CLK\_32K\_IN pin which is referenced to the VDDIO\_SYS rail. See the Tegra K1 Data Sheet for details on the requirements for this clock.

### 3.2.4 Oscillator Clock

A crystal is connected to XTAL\_OUT and XTAL\_IN to generate the reference clock internally. A reference circuit is shown in Figure 10. The table contains the requirements for the crystal used, the value of the parallel bias resistor and information to calculate the values of the two external load capacitors ( $C_{L1}$  and  $C_{L2}$ ) shown in the circuit.



Figure 10. Crystal Connection



Table 16 Crystal and Circuit Requirements

Symbol	Parameter	Min	Тур	Мах	Unit	Notes
F <sub>P</sub>	Parallel resonance crystal Frequency		12		MHz	1
F <sub>TOL</sub>	Frequency Tolerance		±50		ppm	1
CL	Load Capacitance for crystal parallel resonance Typical values used for $C_{L1}/C_{L2}$	5	12		pF	1, 3, 5
DL	Crystal Drive Level			300	uW	1, 6
ESR	Equivalent Series Resistance			100	Ω	2,4
T <sub>START</sub>	Start Time (From AVDD_OSC on or SYS_CLK_REQ active coming out of Deep Sleep)		< 6	10	mS	
T <sub>BUF_DRV</sub>	Tegra Oscillator Buffer drive strength register value		TBD			7
R <sub>BIAS</sub>	Bias resistor value		2		MΩ	

Note: 1. F<sub>P</sub>, F<sub>TOL</sub>, C<sub>L</sub> and DL are found in the Crystal Data Sheet

- 2. ESR = RM \* (1 + CO/CL)^2 where: RM = Motional Resistance; C0 =Shunt Capacitance from Crystal Data Sheet; Data Sheets may specify ESR directly consult manufacturer if unclear whether ESR or RM are specified.
- 3. C<sub>L</sub> = Load capacitance (Crystal Data Sheet). CPCB is PCB capacitance (trace, via, pad, etc.)
- 4. Crystals with lower ESR and C<sub>L</sub> requirements are recommended
- 5. Load capacitor values (CLx) can be found with formula:  $C_L = [(CL1xCL2)/(CL1+CL2)]+CPCB$ . Or, since CL1 and CL2 are typically of equal value, CL = (CLx/2)+CPCB.  $CLx = (CL CPCB) \times 2$
- 6.  $DL = 0.5 \text{*}ESR^{*}(2\pi \times F_{P} \times CL \times V)^{2}$ .  $V = AVDD_{OSC} = 1.8V$
- 7. If other drive strength settings are used, XTAL\_OUT swing should reach below 200mV & above 1.3V over all conditions

Parameter		Requirement	Units	Notes
Topology		Point to Point		
Number of loads		1	load	
Reference plane		GND		Including Crystal itself
Breakout Region Max Delay		Min width/spacing		
Trace Impedance	Differential Single-ended	90 55	Ω	±20% (See Note 1)
Trace Spacing (to other nets)	Microstrip	3х	dielectric	Include keep out area around

 Table 17. Crystal Interface Signal Routing Requirements





Parameter	Requirement	Units	Notes
Stripline	2x		crystal itself.
Max Trace Delay	400	ps	
Max Trace Intra-pair (XTAL_OUT to XTAL_IN) Skew	6 (microstrip) 7 (stripline)	ps	

- Note: Keep XTAL\_IN/OUT traces away from other signal traces or unrelated power traces/areas or power supply components. Use proper GND isolation around and above/below these sensitive signals.
  - Max Trace Delay & Max Trace Delay Skew matching must include substrate pin delays unless otherwise specified
  - Routing as differential pair provides better noise immunity

### Table 18. XTAL\_IN/OUT Signal Connections

Ball Name	Туре	Termination	Description
XTAL_IN XTAL_OUT	A	Load capacitors from XTAL_IN & XTAL_OUT to GND. Typically 12pF, but depends on PCB loading & Crystal Specs.	Crystal Input and Output: Connect to a 12MHz Crystal

### Table 19. Crystal Interface Package Delays

Signal Name	Ball #	Package Delay (ps)		
XTAL_IN	E3	72		
XTAL_OUT	E4	70		

### 3.3 DRAM

Tegra supports DDR3L or LPDDR3 up to 8GB total, up to 1866 (933MHz).

### DDR Pin Configuration/Remapping

Tegra supports the remapping of the Address/Command/Control pins in order to make routing easier/cleaner. A table is provided for each DRAM configuration option supported that shows how the Address/Control/Command/Data pins should be routed to the DRAM devices. This table must be followed exactly.

Note: The pin multiplexing tables use the "default" DDR pin names/numbers as in the Tegra K1 Data Sheet. However, the reference schematics may use modified Tegra schematic symbols to make them more readable. For these, pin swapping will have been done, at least in part, by renaming the DRAM pins & routing these directly to their counterparts on the DRAM. Check which symbol type is used before using the pin multiplexing tables.



### Figure 11. DDR3L Connections



Note: - See the "Power Decoupling Guidelines" section for power rail decoupling and filter requirements for Tegra.



Figure 12. Configuration Option #14 (DDR3L, 4x16, 2 Top/2 Bottom Vertical) Placement Example



Figure 13. Configuration Option #10 (DDR3L, 4x16, 1x4 Top, Inline) Placement Example



The following tables show the connections from TK1 out to the four DDR3L DRAM devices. The symbol used in the reference schematics is a modified version of the default pin out shown in the Data Sheet. The tables include columns that contain the default pin out, Jetson TK1 symbol ball number, the net name used to connect to the DRAM, which device the net is going to, the DDR ball number and finally the ball name. All of these should be duplicated on a design. The same symbol ball out, same net names associated with each ball, etc. should be used to ensure the connections match and can be easily verified against the table and/or reference design.



### Table 20 DRAM Pin Multiplexing Option #14 (DDR3L, , 4x16, 2 Top/2 Bottom Vertical)

Tegra Ball #	Tegra Default Ball Name	Jetson Symbol Ball Name	DDR3L Net Name	DDR Device	DDR Ball #	DDR Ball Name	Teg Bal	gra [    # [	Tegra Default Ball Name	Jetson Symbol Ball Name	DDR3L Net Name	DDR Device	DDR Ball #	DDR Ball Name
G14	DDR_CLK	DDR_CLK	DDR0_CLKP	1 & 2	J7	CLK	A	.8 [	DDR_DQ16	DDR_DQ18	DDR_DQ[26]	2	F2	DQ2
H14	DDR_CLK_N	DDR_CLK_N	DDR0_CLKN	1 & 2	K7	CLK_N	В	8 [	DDR_DQ17	DDR_DQ16	DDR_DQ[24]	2	E3	DQ0
H18	DDR_CLKB	DDR_CLKB	DDR1_CLKP	3&4	J7	CLK	C	6 [	DDR_DQ18	DDR_DQ17	DDR_DQ[25]	2	H7	DQ7
G18	DDR_CLKB_N	DDR_CLKB_N	DDR1_CLKN	3 & 4	K7	CLK_N	E	6 [	DDR_DQ19	DDR_DQ23	DDR_DQ[31]	2	F8	DQ3
E14	DDR_A0	DDR_A2	DDR_A[2]	All	P3	A2	A	.7 E	DDR_DQ20	DDR_DQ22	DDR_DQ[30]	2	G2	DQ6
D14	DDR_A1	DDR_A5	DDR_A0[5]	1&2	P2	A5	A	6 L	DDR_DQ21	DDR_DQ19	DDR_DQ[27]	2	H8	DQ5
E15	DDR_A2	DDR_WE_N	DDR_WE_L	All	L3	WE_L	D	6 L	DDR_DQ22	DDR_DQ21	DDR_DQ[29]	2	H3	DQ4
E12	DDR_A3	DDR_A4	DDR_AU[4]		P0	A4	r C	0 L 0 r		DDR_DQ20	DDR_DQ[20]	2	F7 F2	
F12	DDR 45				P3	Δο	D	8 1	DDR_DQ32P	DDR_DOS2N	DDR_DOS3N	2	63	
C12	DDR_A6	DDR A8			T8	A8	B	6 [	DDR_DM2	DDR_DM2	DDR_DM[3]	2	F7	
F14	DDR A7	DDR A7	DDR A[7]	All	R2	A7	G	12	DDR DO24	DDR DO29	DDR DO[13]	2	C2	DO11
D15	DDR_A8	DDR_RAS_N	DDR_RAS_L	All	J3	RAS_L	H1	12 [	DDR_DQ25	DDR_DQ31	DDR_DQ[15]	2	C3	DQ9
B12	DDR_A9	DDR_A6	DDR_A[6]	All	R8	A6	A1	11 [	DDR_DQ26	DDR_DQ25	DDR_DQ[9]	2	A3	DQ15
D18	DDR_A10	DDR_A13	DDR_A[13]	All	T3	A13	E1	11 [	DDR_DQ27	DDR_DQ26	DDR_DQ[10]	2	A7	DQ12
G17	DDR_A11	DDR_A_B3	DDR_A1[3]	3&4	N2	A3	A1	10 E	DDR_DQ28	DDR_DQ30	DDR_DQ[14]	2	B8	DQ14
A16	DDR_A12	DDR_A15	DDR_A[15]	All	M7	A15	B1	11 [	DDR_DQ29	DDR_DQ27	DDR_DQ[11]	2	A2	DQ13
C20	DDR_A13	DDR_A14	DDR_A[14]	All	T7	A14	F1	11 [	DDR_DQ30	DDR_DQ28	DDR_DQ[12]	2	C8	DQ10
E17	DDR_A14	DDR_BA0	DDR_BA[0]	All	M2	BA0	D1		DDR_DQ31	DDR_DQ24	DDR_DQ[8]	2	D7	DQ8
E18	DDR_A15	DDB A BE	DDR A1[1]	All	N8 CD	DA I	H		DDR_DQS3P	DDR_DQS3P	DDR_DQSTP	2	U/	
E20				30/4	P2 DQ	Δ/	C1	11 L		DDR DM2	DDR DM[1]	2	D7	UDU3_L
E20	DDR A B5	DDR BA2	DDR BA[2]	ΔII	M3	BA2	G	21 I	DDR DO32	DDR DO34	DDR DO[50]	2	D7	DO8
F18	DDR BA0	DDR A12	DDR $A[12]$	All	N7	A12	A2	21 [	DDR DO33	DDR_DO35	DDR_D0[51]	3	C2	D011
D20	DDR BA1	DDR A11	DDR A[11]	All	R7	A11	E2	21 [	DDR DQ34	DDR DQ32	DDR DQ[48]	3	C8	DQ10
H15	DDR_BA2	DDR_A10	DDR_A[10]	All	L7	A10	F2	20 [	DDR_DQ35	DDR_DQ38	DDR_DQ[54]	3	B8	DQ14
C14	DDR_CAS_N	DDR_A0	DDR_A[0]	All	N3	A0	G2	20 E	DDR_DQ36	DDR_DQ36	DDR_DQ[52]	3	A7	DQ12
G15	DDR_RAS_N	DDR_A3	DDR_A0[3]	1&2	N2	A3	D2	21 E	DDR_DQ37	DDR_DQ37	DDR_DQ[53]	3	A2	DQ13
C15	DDR_WE_N	DDR_CAS_N	DDR_CAS_L	All	K3	CAS_L	B2	21 [	DDR_DQ38	DDR_DQ33	DDR_DQ[49]	3	C3	DQ9
F15	DDR_RESET_N	DDR_RESET_N	DDR_RESET_L	All	T2	RESET_L	C2	21 [	DDR_DQ39	DDR_DQ39	DDR_DQ[55]	3	A3	DQ15
B14	DDR_CSO_N	DDR_CS1_N	DDR0_CS1_L	1&2	L1	CS1_L	H2	21 [	DDR_DQS4P	DDR_DQS4P	DDR_DQS6P	3	F3	UDQS
AIZ D10	DDR_CSI_N	DDR_CSU_N	DDRU_CSU_L	1&2	L2	CSU_L	H <sub>2</sub>	20 L	DDR_DQS4N	DDR_DQS4N	DDR_DQS6N	3	63	UDQS_L
A10	DDR_CS_BU_N			3 & 4	12		P2	21 1				3	Е/ ЦQ	DOS
A13	DDR_CKE0	DDR_CKE0	DDR0_CKE0	1&2	K9	CKE0	C2	24 [	DDR_DO41	DDR_DQ43	DDR_D0[33]	3	F7	D01
A14	DDR_CKE1	DDR CKE1	DDR0_CKE1	1&2	J9	CKE1	E2	27 [	DDR DQ42	DDR DQ46	DDR_DQ[38]	3	G2	DQ6
A20	DDR CKE BO	DDR CKE BO	DDR1 CKE0	3 & 4	K9	CKE0	A2	24 [	DDR DQ43	DDR DQ43	DDR DQ[35]	3	F8	DQ3
B20	DDR_CKE_B1	DDR_CKE_B1	DDR1_CKE1	3&4	J9	CKE1	E2	26 E	DDR_DQ44	DDR_DQ44	DDR_DQ[36]	3	H3	DQ4
A15	DDR_ODT0	DDR_ODT0	DDR0_ODT0	1&2	K1	ODT0	B2	26 E	DDR_DQ45	DDR_DQ40	DDR_DQ[32]	3	F2	DQ2
B15	DDR_ODT1	DDR_ODT1	DDR0_ODT1	1 & 2	J1	ODT1	A2	25 E	DDR_DQ46	DDR_DQ47	DDR_DQ[39]	3	H7	DQ7
C18	DDR_ODT_B0	DDR_ODT_B0	DDR1_ODT0	3 & 4	K1	ODT0	A2	26 [	DDR_DQ47	DDR_DQ42	DDR_DQ[34]	3	E3	DQ0
A18	DDR_OD1_B1	DDR_CS_B1_N	DDR1_CS1_L	3&4	L1	CS1_L	C2	26 L	DDR_DQS5P	DDR_DQS5P	DDR_DQS4P	3	C7	LDQS
							D2	26 L	DDR_DQS5N	DDR_DQS5N	DDR_DQS4N	3	B/	LDQS_L
٨2				1	EQ	DO2	B2	24 L 22 L			DDR_DO[4]	3	03	
Δ <i>1</i>		DDR_DQ7		1	F0 H8	DQ3	E2	22 L 24 F		DDR_DQ54	DDR_D0[62]	4	B8	DQ9
B5	DDR DO2	DDR DO0	DDR DO[16]	1	E3	DQ0	A	23 Г	DDR DQ50	DDR DO50	DDR D0[58]	4	D7	DQ8
C2	DDR_DQ3	DDR_DQ3	DDR_DQ[19]	1	H3	DQ4	C2	23 [	DDR_DQ51	DDR_DQ52	DDR_DQ[60]	4	C2	DQ11
B3	DDR_DQ4	DDR_DQ4	DDR_DQ[20]	1	G2	DQ6	B2	23 [	DDR_DQ52	DDR_DQ48	DDR_DQ[56]	4	A7	DQ12
B2	DDR_DQ5	DDR_DQ1	DDR_DQ[17]	1	F7	DQ1	G2	23 E	DDR_DQ53	DDR_DQ49	DDR_DQ[57]	4	A3	DQ15
C3	DDR_DQ6	DDR_DQ5	DDR_DQ[21]	1	F2	DQ2	F2	24 E	DDR_DQ54	DDR_DQ53	DDR_DQ[61]	4	C8	DQ10
A5	DDR_DQ7	DDR_DQ2	DDR_DQ[18]	1	H7	DQ7	H2	23 E	DDR_DQ55	DDR_DQ51	DDR_DQ[59]	4	A2	DQ13
C5	DDR_DQS0P	DDR_DQS0P	DDR_DQS2P	1	F3	LDQS	E2	23 E	DDR_DQS6P	DDR_DQS6P	DDR_DQS7P	4	F3	UDQS
D5	DDR_DQSON	DDR_DQSON	DDR_DQS2N	1	G3	LDQS_L	D2	23 L	DDR_DQS6N	DDR_DQS6N	DDR_DQS7N	4	G3	UDQS_L
	DDR_DM0	DDR_DMU	DDR_DM[2]	1	E/	LDM DO12	F2	23 L	DDR_DM6	DDR_DM6	DDR_DM[7]	4	E/	UDM DO1
E0				1	A/	DQ12	02	2/ L				4	Г/ Цо	DOS
68	DDR DO10	DDR DO10	DDR DO[2]	1	A3	DO15	C2	27 L	DDR D058	DDR_D057	DDR DO[41]	4	F2	DO2
F8	DDR DO11	DDR_D014	DDR DO[6]	1	A2	D013	A2	29 1	DDR D059	DDR_DO62	DDR DO[46]	4	H7	D07
E9	DDR DQ12	DDR DQ8	DDR DQ[0]	1	C8	DQ10	C.3	31 [	DDR DQ60	DDR DQ56	DDR DQ[40]	4	H3	DQ4
A9	DDR_DQ13	DDR_DQ9	DDR_DQ[1]	1	B8	DQ14	A2	27 [	DDR_DQ61	DDR_DQ59	DDR_DQ[43]	4	E3	DQ0
D9	DDR_DQ14	DDR_DQ15	DDR_DQ[7]	1	D7	DQ8	C3	30 E	DDR_DQ62	DDR_DQ58	DDR_DQ[42]	4	G2	DQ6
E8	DDR_DQ15	DDR_DQ12	DDR_DQ[4]	1	C3	DQ9	A2	28 E	DDR_DQ63	DDR_DQ63	DDR_DQ[47]	4	F8	DQ3
G9	DDR_DQS1P	DDR_DQS1P	DDR_DQSOP	1	C7	UDQS	B3	30 E	DDR_DQS7P	DDR_DQS7P	DDR_DQS5P	4	C7	LDQS
H9	DDR_DQS1N	DDR_DQS1N	DDR_DQSON	1	B7	UDQS_L	B2	29 [	DDR_DQS7N	DDR_DQS7N	DDR_DQS5N	4	B7	LDQS_L
B9	DDR_DM1	DDR_DM1	DDR_DM[0]	1	D3	UDM	B2	27 [	UUR_DM7	DDR_DM7	DDR_DM[5]	4	D3	LDM

Notes: -

The DDR pin remapping must be followed exactly as shown above.

- The DDR Devices 1/2/3/4 in the table above correspond to DDR U7B1/U4B1/U4C1/U7C1 respectively on the Jetson TK1 platform.



### Table 21 DRAM Pin Multiplexing Option #10 (23x23mm, DDR3L, 4x16, 1x4 Top, Inline)

Tegra Ball #	Tegra Default Ball Name	Jetson Symbol Ball Name	DDR3L Net Name	DDR Device	DDR Ball #	DDR Ball Name	Tegra Ball #	Tegra Default Ball Name	Jetson Symbol Ball Name	DDR3L Net Name	DDR Device	DDR Ball #	DDR Ball Name
G14	DDR_CLK	DDR_CLK	DDR0_CLKP	1 & 2	J7	CLK	A8	DDR_DQ16	DDR_DQ18	DDR_DQ[10]	2	F2	DQ2
H14	DDR_CLK_N	DDR_CLK_N	DDR0_CLKN	1 & 2	K7	CLK_N	B8	DDR_DQ17	DDR_DQ16	DDR_DQ[8]	2	E3	DQ0
H18	DDR_CLKB	DDR_CLKB	DDR1_CLKP	3 & 4	J7	CLK	C6	DDR_DQ18	DDR_DQ17	DDR_DQ[9]	2	F7	DQ1
G18	DDR_CLKB_N	DDR_CLKB_N	DDR1_CLKN	3 & 4	K7	CLK_N	E6	DDR_DQ19	DDR_DQ23	DDR_DQ[15]	2	H7	DQ7
E14	DDR_A0	DDR_A2	DDR_A[2]	All	P3	A2	A7	DDR_DQ20	DDR_DQ22	DDR_DQ[14]	2	G2	DQ6
D14	DDR_A1	DDR_A5	DDR_A0[5]	1 & 2	P2	A5	A6	DDR_DQ21	DDR_DQ19	DDR_DQ[11]	2	F8	DQ3
E15	DDR_A2	DDR_WE_N	DDR_WE_L	All	L3	WE_L	D6	DDR_DQ22	DDR_DQ21	DDR_DQ[13]	2	H8	DQ5
E12	DDR_A3	DDR_A4	DDR_A0[4]	1&2	P8	A4	F6	DDR_DQ23	DDR_DQ20	DDR_DQ[12]	2	H3	DQ4
D12	DDR_A4	DDR_A1	DDR_A[1]	All	P7	A1	C8	DDR_DQS2P	DDR_DQS2P	DDR_DQS1P	2	F3	LDQS
F12	DDR_A5	DDR_A9	DDR_A[9]	All	R3	A9	D8	DDR_DQS2N	DDR_DQS2N	DDR_DQS1N	2	G3	LDQS_L
C12	DDR_A6	DDR_A8	DDR_A[8]	All	18	A8	B6	DDR_DM2	DDR_DM2	DDR_DM[1]	2	E7	LDM
F14	DDR_A7	DDR_A/	DDR_A[7]	All	R2	A/	G12	DDR_DQ24	DDR_DQ29	DDR_DQ[29]	2	A2	DQ13
D15	DDR_A8	DDR_RAS_N	DDR_RAS_L	All	J3	RAS_L	H12	DDR_DQ25	DDR_DQ31	DDR_DQ[31]	2	A3	DQ15
BI2	DDR_A9	DDR_A6	DDR_A[6]	All	R8 T0	A6	AII	DDR_DQ26	DDR_DQ25	DDR_DQ[25]	2	63	DQ9
D18	DDR_ATO	DDR_AI3	DDR_A[13]	All	13	A13	EII	DDR_DQ27	DDR_DQ26	DDR_DQ[26]	2	60	DQ10
GI/	DDR_ATT	DDR_A_B3	DDR_AI[3]	3 & 4	NZ	A3	A10	DDR_DQ28	DDR_DQ30	DDR_DQ[30]	2	88	DQ14
A16	DDR_A12	DDR_A15	DDR_A[15]	All	M/ T7	A15	BII E11	DDR_DQ29	DDR_DQ27	DDR_DQ[27]	2	62	DUTT
C20	DDR_AI3	DDR_AI4	DDR_A[14]	All	17	A14	FII D11	DDR_DQ30	DDR_DQ28	DDR_DQ[28]	2	A/	DQ12
E17	DDR_A14	DDR_BAU	DDR_BA[U]	AII	IVIZ NO	BAU DA1		DDR_DQ31	DDR_DQ24	DDR_DQ[24]	2	07	
E18 U17				AII 3.8.4	NQ CD	DA I 45	611	DDR_DQ33P	DDR_DQ53P	DDR DOS3N	2	C/ 87	
E20				364	PZ D0	но Лл	G11 C11	DDR_DQ33N	DDR_DQS3N		2	D/	UDUS_L
E20				λII	го Mo	RA2	621				2	03	
F17 E10	DDR_A_DO	DDR_DAZ	DDR_DA[2]		N7	DA2	G21 A21	DDR_DQ32			2	C0	DQ10
F 10	DDR_DAU	DDR_AI2	DDR_A[12]		N/ D7	A12	A21	DDR_DQ33	DDR_DQ35		2	02	
U20					17	A10	E21				2	B8	DQ8
C14	DDR_DAZ				L7 N3	A10	F20				2	Δ0	DQ14
G15	DDR_CAS_N	DDR_A3		1 & 2	N2	Δ3	D21	DDR_DQ30			3	Δ2	DQ12 D013
C15	DDR_WE_N	DDR_AS			K3		B21	DDR_DQ37			3	C3	
E15	DDR_WE_N	DDR RESET N	DDR RESET I		T2	RESET I	C21				3	Δ3	DQ15
B14	DDR_RESET_N	DDR_CS1_N	DDR0_CS1_L	1 & 2	11	CS1 I	H21	DDR_DOS4P	DDR_DOS4P	DDR DOS4P	3	F3	
A12	DDR_CS1_N	DDR_CS0_N	DDR0_CS0_L	1&2	12		H20	DDR_DOS4N	DDR_DOS4N	DDR_DOS4N	3	G3	
B18	DDR_CS_B0_N	DDR_00T_B1	DDR1_0DT1	3 & 4	J1	ODT1	F21	DDR_DM4	DDR_DM4	DDR_DM[4]	3	F7	
A19	DDR_CS_B1_N	DDR_CS_B0_N	DDR1_CS0_L	3 & 4	12	CS0_L	D24	DDR DO40	DDR DO45	DDR_DO[53]	3	H8	D05
A13	DDR CKE0	DDR CKE0	DDR0 CKE0	1 & 2	K9	CKE0	C24	DDR DQ41	DDR DQ41	DDR DQ[49]	3	F7	DQ1
A14	DDR CKE1	DDR CKE1	DDR0 CKE1	1&2	J9	CKE1	E27	DDR DQ42	DDR DQ46	DDR DQ[54]	3	G2	DQ6
A20	DDR CKE BO	DDR CKE BO	DDR1 CKE0	3 & 4	К9	CKE0	A24	DDR DQ43	DDR DQ43	DDR DQ[51]	3	F8	DQ3
B20	DDR CKE B1	DDR CKE B1	DDR1 CKE1	3 & 4	J9	CKE1	E26	DDR DQ44	DDR DQ44	DDR DQ[52]	3	H3	DQ4
A15	DDR ODTO	DDR ODTO	DDR0 ODT0	1 & 2	K1	ODT0	B26	DDR DQ45	DDR DQ40	DDR DQ[48]	3	E3	DQ0
B15	DDR_ODT1	DDR_ODT1	DDR0_ODT1	1 & 2	J1	ODT1	A25	DDR_DQ46	DDR_DQ47	DDR_DQ[55]	3	H7	DQ7
C18	DDR_ODT_B0	DDR_ODT_B0	DDR1_ODT0	3 & 4	K1	ODT0	A26	DDR_DQ47	DDR_DQ42	DDR_DQ[50]	3	F2	DQ2
A18	DDR_ODT_B1	DDR_CS_B1_N	DDR1_CS1_L	3&4	L1	CS1_L	C26	DDR_DQS5P	DDR_DQS5P	DDR_DQS6P	3	C7	LDQS
							D26	DDR_DQS5N	DDR_DQS5N	DDR_DQS6N	3	B7	LDQS_L
							B24	DDR_DM5	DDR_DM5	DDR_DM[6]	3	D3	LDM
A3	DDR_DQ0	DDR_DQ7	DDR_DQ7	1	H7	DQ7	A22	DDR_DQ48	DDR_DQ54	DDR_DQ[46]	4	B8	DQ14
A4	DDR_DQ1	DDR_DQ6	DDR_DQ6	1	G2	DQ6	E24	DDR_DQ49	DDR_DQ55	DDR_DQ[47]	4	A3	DQ15
B5	DDR_DQ2	DDR_DQ0	DDR_DQ0	1	E3	DQ0	A23	DDR_DQ50	DDR_DQ50	DDR_DQ[42]	4	C8	DQ10
C2	DDR_DQ3	DDR_DQ3	DDR_DQ3	1	F8	DQ3	C23	DDR_DQ51	DDR_DQ52	DDR_DQ[44]	4	A2	DQ12
B3	DDR_DQ4	DDR_DQ4	DDR_DQ4	1	H3	DQ4	B23	DDR_DQ52	DDR_DQ48	DDR_DQ[40]	4	D7	DQ8
B2	DDR_DQ5	DDR_DQ1	DDR_DQ1	1	F7	DQ1	G23	DDR_DQ53	DDR_DQ49	DDR_DQ[41]	4	C3	DQ9
C3	DDR_DQ6	DDR_DQ5	DDR_DQ5	1	H8	DQ5	F24	DDR_DQ54	DDR_DQ53	DDR_DQ[45]	4	A2	DQ13
A5	DDR_DQ7	DDR_DQ2	DDR_DQ2	1	F2	DQ2	H23	DDR_DQ55	DDR_DQ51	DDR_DQ[43]	4	C2	DQ11
C5	DDR_DQS0P	DDR_DQS0P	DDR_DQS0P	1	F3	LDQS	E23	DDR_DQS6P	DDR_DQS6P	DDR_DQS5P	4	F3	UDQS
D5	DDR_DQSON	DDR_DQSON	DDR_DQSON	1	G3	LDQS_L	D23	DDR_DQS6N	DDR_DQS6N	DDR_DQS5N	4	G3	UDQS_L
C1	DDR_DM0	DDR_DM0	DDR_DM[0]	1	E7	LDM	F23	DDR_DM6	DDR_DM6	DDR_DM[5]	4	E7	UDM
C9	DDR_DQ8	DDR_DQ11	DDR_DQ[19]	1	C2	DQ11	D27	DDR_DQ56	DDR_DQ61	DDR_DQ[61]	4	H8	DQ5
F9	DDR_DQ9	DDR_DQ13	DDR_DQ[21]	1	A2	DQ13	029	DDR_DQ57	DDR_DQ60	DDR_DQ[60]	4	H3	DQ4
G8	DDR_DQ10	DDR_DQ10	DDR_DQ[18]	1	08	DQ10	027	DDR_DQ58	DDR_DQ57	DDR_DQ[57]	4	F7	DQ1
F8	DDR_DQ11	DDR_DQ14	DDR_DQ[22]	1	88	DQ14	A29	DDR_DQ59	DDR_DQ62		4	G2	DQ6
E9	DDR_DQ12	DDR_DQ8	DDR_DQ[16]	1	07	DQ8	031	DDR_DQ60	DDR_DQ56		4	E3	DQU
A9	DDR_DQ13			1	03	DQ9	A27	DDR_DQ61	DDR_DQ59		4	FÖ	DQ3
09	DDR_DQ14	DDR_DQ15	DDR_DQ[23]	1	A3	DQ15	030	DDR_DQ62			4	F2	DQ2
Eð	DDR_DQ15	DDR_DQ12	DDR_DQ[20]	1	A/		A28	DDR_DQ63	DDR_DQ63		4	H/	
69	DDR_DQSTP	DDR_DUSTP	DDR_DQ52P	1	D7		D30	DDR_DQS/P	DDR_DQS/P	DDR_DQS/P	4	07	
H9 D0	DDR_DQSTN	DDR_DUSIN	DDR_DQ52N	1	B/	UDUS_L	B29	DDR_DQS/N	DDR_DQS/N	DDR_DQS/N	4	B/	LDUS_L
BA	DDK_DMI	DDR_DMI	DDR_DM[2]		D3	UDM	B27	DDK_DM/	DDR_DMI/	DDK_DM[/]	4	D3	LDIVI

Note: The DDR pin remapping must be followed exactly as shown above.



### **DDR3L Design Guidelines**

- Notes: The topology for each signal must be followed exactly as shown in the figures included for each signal group. The Requirements are 32-bit channel except the DDR0\_CLKP/DDR0\_CLKN to DDR1\_CLKP/DDR1\_CLKN requirement.
  - New Skew requirement term definitions:
    - "Center, +/-" mean the skew is measured from the clock/strobe (center signal) to the related signals, either before or after the strobe/clock and must meet the required max value.
    - "Absolute" mean the maximum skew between any of the signals listed is within the required max value.
    - "Load to Load" means that the skew is the total of the path from Tegra out to the destination (load) for each signal involved in the requirement. This allows for asymmetric routing of the different branches in T-topologies, as long as the total lengths/delays are within the requirement value.

Figure 14. Single Rank, 16-bit DDR3L DQ, DQS, DQM (Point-Point Topology - Used w/2-T Address Topology)



### Table 22. DDR3L, 4x16 Data Signal Group Routing Requirements

Parameter		Requirement	Units	Notes
Max Frequency / Data Rate		933 / 1866	MHz/Mbps	See note 1
Switching Period (T)		0.5	Т	
Тороlоду		Direct		
Configuration / Device Organization		1	load	
Termination (VTT & ODT)		None		
Reference plane		GND		
Max PCB breakout length		6.35	mm	
Via proximity (Signal to reference)		< 3.8 (24)	mm (ps)	See note 2
Capacitance				
Min Input/Output Capacitance (DQ/DM/DQS)		1.4	pF	
Max Input/Output Capacitance (DQ/DM/DQS)		2.1	pF	
Input Capacitance Delta (DQSP & DQSN)	Min / Max	0 / 0.15	pF	
Input Capacitance Delta(DQ, DM, DQSP, DQSN)	Min / Max	-0.5 / 0.3	pF	
Impedance/Spacing				
Trace Impedance	DQ / DM DQS Single Ended DQS Differential	40/50 (option) 45/50 (option) 80/90 (option)	Ω	$\pm$ 15%. Options are for 40Ω/45Ω/80Ω or 50Ω/50Ω/90Ω
Trace Spacing	Microstrip / Stripline	3x / 2x	dielectric	
Max Via Count				
Max Number of Vias (Tx to Rx (Per device) / T	x to all loads):	2		
Trace Lengths/Delays				
Max Trace Length/Delay (PCB Main Trunk)		33.34 (210)	mm (ps)	
Skew Matching				
Max Trace Length/Delay Skew from DQS to DC	Ω / DM	1.575 (Center +/- 10)	mm (ps)	



Parameter	Requirement	Units	Notes
Max Trace Length/Delay Skew from DQSP & DQSN	0.32 (2)	mm (ps)	
Max Trace Length/Delay Skew from CLK to DQS (load to load) PCB Main Trunk + Branch (CLK) compared withPCB Main Trunk (DQS)	25.40 (160)	mm (ps)	
Max Trace Length/Delay Skew from DQ to DQ (within byte)	3.18 (Absolute 20)	mm (ps)	
Max Trace Length/Delay Skew from DQ to DQ (within same 32-bit partition)	12.70 (80)	mm (ps)	
Max Trace Length/Delay Skew from DQ (Lower 32-bit partition) to DQ (Upper 32-bit partition)	12.70 (80)	mm (ps)	
General DQ/DM/DQS Routing Considerations			
DQ/DM/DQS in each byte should be kept on same layer			

Note: 1. Max frequency is target. Actual frequency may depend on characterization results, and achievable PLL frequency used to clock the EMC block

2. Up to 4 signal vias can share a single GND return via

Table 23.	DDR3L,	4x16 Da	ta Signal	Group	Connections
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Signal Name	Туре	Termination	Description						
DDR_DQ[63:0] DDR_DM[7:0] DDR_DQS[7:0]P/N	I/O O DIFF I/O	No VTT or ODT (On-Die Termination) Required	Data:Connect to DQ pins of all DRAMs (see table below)Data Mask:Connect to DM pins on DRAMs (see table below)Data Strobes:Connect to DQSxP/DQSxN pins of all DRAM (table below)Byte Lanes (Groupings) per channelDataDataData MaskDataDataDataStrobe						
			DQ[7:0] DQ[15:8] DQ[23:16] DQ[31:24]	DMO DM1 DM2 DM3	DQS0P/N DQS1P/N DQS2P/N DQS3P/N	DQ[39:32] DQ[47:40] DQ[55:48] DQ[63:56]	DM4 DM5 DM6 DM7	DQS4P/N DQS5P/N DQS6P/N DQS7P/N	

Note: The Tegra DRAM ball names may not correspond to the signal brought out on that ball. Use the DRAM Pin Multiplexing table to select the correct Tegra ball to connect to each DDR3L ball.

Figure 15. DDR3L, 4x16 Address (A[15:6,2:0), Command (RAS\_N, CAS\_N, WE\_N & RESET\_N) 2-T Topology



### Table 24. DDR3L, 4x16 Address/Command Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency / Data Rate	466.5 / 466.5	MHz/Mbps	Note 1
Switching Period (T)	2	Т	
Topology	Т-Т		
Configuration / Device Organization	4	load	
Reference Pplane	GND		



Parameter	Requirement	Units	Notes
Max PCB breakout length	6.35	mm	
Via proximity (Signal to Reference)	< 3.8 (24)	mm (ps)	See Note 2
Capacitance			
Input Capacitance Min /	Max 0.75 / 1.2	pF	
Input Capacitance Delta (All Add/Cmd) Min /	Max -0.4 / 0.4	pF	
Impedance/Spacing			
Trace Impedance	50	Ω	±15%
Trace Spacing Microstrip / Strip	line 3x / 2x	dielectric	
Max Via Count			
Max Number of Vias (Tx to Rx (Per device) / Tx to all loads):	4 / 8		
Trace Lengths/Delays			
Max Trace Length/Delay (PCB Main Trunk)	41.28 (260)	mm (ps)	
Max Trace Length/Delay: Branch 1	14.29 (90)	mm (ps)	
Max Trace Length/Delay: Branch 2	14.29 (90)	mm (ps)	
Max Trace Length/Delay Asymmetry for Branch 1	7.17 (45)	mm (ps)	
Max Trace Length/Delay Asymmetry for Branch 2	7.17 (45)	mm (ps)	
Skew Matching			
Max Trace Length/Delay Skew between Addr/Cmd & PCB Main Trunk +Branch 1 + Branch 2	Clk 25.4 (160)	mm (ps)	
Max Trace Length/Delay Skew between any Add/Cmd any other Add/Cmd.	to 25.4 (160)	mm (ps)	

Note: 1. Max frequency is target. Actual frequency may depend on characterization results, and achievable PLL frequency used to clock the EMC block

- 2. Up to 4 signal vias can share a single GND return via
- Address: DDR\_A[15:6,2:0], DDRO\_A[5:3], DDR1\_A[5:3], DDR\_BA[2:0]. Command: DDR\_RAS, DDR\_CAS & DDR\_WE

Table 25. DDR3L, 4x16 Address/Command Signal Group Connections

Signal Name	Туре	Termination	Description
DDR_A[15:6,2:0]	0		Address 15:6, 2:0: Connect to matching Ax pins of all DRAM
DDR_BA[2:0]	0		Bank Address: Connect to BAx pins of all DRAMs
DDR_CAS	0		Column Add. Strobe: Connect to CAS pins of all DRAMs
DDR_RAS	0		Row Address Strobe: Connect to RAS pin of all DRAMs
DDR_WE	0		Write Enable: Connect to WE pin of all DRAMs
DDR_RESET_N	0		Reset: Connect to RESET pin of all DRAMs

**Note:** The Tegra DRAM ball names may not correspond to the signal brought out on that ball. Use the DRAM Pin Multiplexing table to select the correct Tegra ball to connect to each DDR3L ball.



Figure 16. DDR3L, 4x16 Address (A[5:3] for 32-bit partitions [1:0]) 1-T Topology



Table 26. DDR3L, 4x16 Address (A[5:3] for 32-bit partitions [1:0]) Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency / Data Rate	466.5 / 466.5	MHz/Mbps	Note 1
Switching Period (T)	2	Т	
Topology	T-Branch		
Configuration / Device Organization	2	load	
Reference Pplane	GND		
Max PCB breakout length	6.35	mm	
Via proximity (Signal to Reference)	< 3.8 (24)	mm (ps)	See Note 2
Capacitance			
Input Capacitance Min / Max	0.75 / 1.2	pF	
Input Capacitance Delta (All Add/Cmd) Min / Max	-0.4 / 0.4	pF	
Impedance/Spacing			
Trace Impedance	50	Ω	±15%
Trace Spacing Microstrip / Stripline	3x / 2x	dielectric	
Max Via Count			
Max Number of Vias (Tx to Rx (Per device) / Tx to all loads):	4 / 8		
Trace Lengths/Delays			
Max Trace Length/Delay (PCB Main Trunk)	42.86 (270)	mm (ps)	
Max Trace Length/Delay: Branch	14.29 (90)	mm (ps)	
Max Trace Length/Delay Asymmetry for Branch	7.17 (45)	mm (ps)	Absolute
Skew Matching			
Max Trace Length/Delay Skew, Addr & Clk (PCB Main Trunk +Branch A/B)	12.7 (80)	mm (ps)	Center (CIk) +/-
Max Trace Length/Delay Skew: Any Add to any other Add (for A[5:3] & A_B[5:3], this requirement is within each group, not between the groups).	25.4 (160)	mm (ps)	Absolute

Note: 1. Max frequency is target. Actual frequency may depend on achievable PLL frequency used to clock the EMC block

- 2. Up to 4 signal vias can share a single GND return via
- 3. Address: DDR\_A[15:0], DDR\_A\_B[5:3], DDR\_BA[2:0]. Command: DDR\_RAS, DDR\_CAS & DDR\_WE



### Table 27. DDR3L, 4x16 Address (A[5:3] for 32-bit partitions [1:0]) Signal Group Connections

Signal Name	Туре	Termination	Description
DDR_A[5:3]	0		Address 5:3: Connect to matching Ax pins of DRAM in lower 32-bit data
DDR_A_B[5:3]	0		Address B 5:3: Connect to matching Ax pins of DRAM in upper 32-bit data

Note: The Tegra DRAM ball names may not correspond to the signal brought out on that ball. Use the appropriate DRAM Pin Multiplexing tables included after each placement diagram to select the correct connections.

### Figure 17. DDR3L, 4x16 Control 1-T Topology



Note: There are two sets of control signals. Primary set routes to DDR3L devices #1 & #2. Secondary set routes to #3 & #4.

### Table 28. DDR3L, 4x16 Control Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency / Data Rate	933 / 933	MHz/Mbps	Note 1
Switching Period (T)	1	Т	
Тороlоду	T-Branch		
Configuration / Device Organization	2	load	
Reference Pplane	GND		
Max PCB breakout length	6.35	mm	
Via proximity (Signal to Reference)	< 3.8 (24)	mm (ps)	See Note 2
Capacitance			
Input Capacitance Min / Max	0.75 / 1.2	pF	
Input Capacitance Delta (All Ctrl) Min / Max	-0.4 / 0.2	pF	
Impedance/Spacing			
Trace Impedance	50	Ω	±15%
Trace Spacing Microstrip / Stripline	3x / 2x	dielectric	
Max Via Count			
Max Number of Vias (Tx to Rx (Per device) / Tx to all loads):	4 / 8		
Trace Lengths/Delays (T Topology)			
Max Trace Length/Delay (PCB Main Trunk)	42.86 (270)	mm (ps)	
Max Trace Length/Delay: Branch	14.29 (90)	mm (ps)	
Max Trace Length/Delay Asymmetry for Branches	7.14 (45)	mm (ps)	Absolute
Skew Matching			



Parameter	Requirement	Units	Notes
Max Trace Length/Delay Skew: Ctrl & Clk (PCB Main Trunk +Branch A/B)	12.7 (80)	mm (ps)	Center (Clk) +/-
Max Trace Length/Delay Skew in Branch A/B	7.14 (45)	mm (ps)	Absolute
Max Trace Length/Delay Skew: Any Ctrl to any other Ctrl within 32- bit half.	25.4 (160)	mm (ps)	Absolute

- Note: 1. Max frequency is target. Actual frequency may depend on achievable PLL frequency used to clock the EMC block
  - 2. Up to 4 signal vias can share a single GND return via
  - 3. Control: DDR[1:0]\_CS[1:0], DDR[1:0]\_CKE[1:0] & DDR[1:0]\_ODT[1:0].

Table 29.	DDR3L,	4x16 Cc	ntrol Sian	al Group	Connections

Signal Name	Туре	Termination	Description
DDR0_CS[1:0] DDR1_CS[1:0]	0		Chip Select: Connect to CSx pins of all DRAM in lower 32-bit data Chip Select: Connect to CSx pins of all DRAM in upper 32-bit data
DDR0_CKE[1:0] DDR1_CKE[1:0]	0		Clock Enable: Connect to CKEx pin of all DRAM in lower 32-bit data Clock Enable: Connect to CKEx pin of all DRAM in upper 32-bit data
DDR0_ODT[1:0] DDR1_ODT[1:0]	0		<b>On-Die Termination Control</b> : Connect to <b>ODTx</b> pin of all DRAM in lower 32- bit data <b>On-Die Termination Control</b> : Connect to <b>ODTx</b> pin of all DRAM in upper 32- bit data

**Note:** The Tegra DRAM ball names may not correspond to the signal brought out on that ball. Use the appropriate DRAM Pin Multiplexing tables included after each placement diagram to select the correct connections.

### Figure 18. DDR3L, 4x16 Clock 1-T Topology



Note: There are two sets of differential clock signals. The primary set routes to DDR3L devices #1 & #2 while the secondary set routes to #3 & #4.

Table 30.	DDR3L,	4x16	Clock	Routing	Requirements

Parameter	Requirement	Units	Notes
Max Frequency	933	MHz	Note 1
Switching Period (T)	0.5	Т	
Тороlоду	T-Branch		
Configuration / Device Organization	2	load	
Reference plane	GND		



Parameter	Requirement	Units	Notes
Max PCB breakout length	6.35	mm	
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 2
DDR_CLK/CLK_N AC Source Termination. Max Length/Delay from Capacitor to Tegra	2.54 (16ps)	mm (ps)	2.2pF capacitor between CLK & CLK_N
Capacitance			
Input Capacitance Min / Max	0.75 / 1.2	pF	
Input Capacitance Delta (CLK_P/CLK_N) Min / Max	0 / 0.15	pF	
Impedance/Spacing			
Trace Impedance Single Ended / Differential	50 / 90	Ω	±15%
Trace Spacing Microstrip / Stripline	3x / 2x	dielectric	
Max Via Count			
Max Number of Vias (Tx to Rx (Per device) / Tx to all loads):	4 / 8		
Trace Lengths/Delays			
Max Trace Length/Delay: PCB Main Trunk	30.16 (190)	mm (ps)	Note 5
Max Trace Length/Delay: Branch	14.29 (90)	mm (ps)	Note 5
Max Trace Length/Delay Asymmetry for Branches	7.14 (45)	mm (ps)	Absolute
Max Trace Length/Delay: Term_A	12.7 (80)	mm (ps)	Absolute
Max Trace Length/Delay: Term_B	3.18 (20)	mm (ps)	Absolute
Max Trace Length/Delay: Term_C	3.18 (20)	mm (ps)	Absolute
Skew Matching			
Max Trace Length/Delay Skew CLK/CLK_N (Main Trunk + T-Branch A/B)	0.79 (5)	mm (ps)	Absolute
Max Trace Length/Delay Skew from DDR_CLK/DDR_CLK_N (lower 32-bit clock pair) to DDR_CLKB/DDR_CLKB_N (upper 32-it clock pair)	4.76 (30)	mm (ps)	Absolute

Note: 1. Max frequency is target. Actual frequency may depend on characterization results, and achievable PLL frequency used to clock the EMC block.

- 2. Up to 4 signal vias can share a single GND return via
- 3.  $45\Omega$  AC load termination resistors should be on top layer without any vias. 0.01uF capacitor from resistors should be on top layer with single via to GND
- 4. Max Trace Length/Delay for PCB Main Trunk + Branch & the Max Trace Length/Delay: Branch requirements must be met. The Max Trace Length/Delay: PCB Main Trunk can be exceeded as long as the Branch is adjusted to meet the Max Trace Length/Delay for PCB Main Trunk + Branch requirement.

Signal Name	Туре	Termination	Description
DDRO_CLKP DDRO_CLKN	DIFF OUT	90 $\Omega$ between CLKP & CLKN & 0.01uF cap center- tapped to GND. 2 x 45 $\Omega$ (closest 1% value). 2.2pF cap between the CLKP & CLKN lines near Tegra	Differential Clock for Lower 32-bit Channel: Connect CLK_P/CLK_N pins of DRAM for Channel 0.
DDR1_CLKP DDR1_CLKN	DIFF OUT	Same as for CLKP/CLKN above	Differential Clock for Upper 32-bit Channel: Connect to CLK_P/CLK_N pins of DRAM for Channel 1.

	Table 31.	DDR3L,	4x16 Clock	Connections
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Note: The Tegra DRAM ball names may not correspond to the signal brought out on that ball. Use the appropriate DRAM Pin Multiplexing tables included after each placement diagram to select the correct connections.

Miscellaneous DDR3L Guidelines

### Table 32. DDR\_COMP\_PU/PD Routing Requirements

Parameter	Requirement	Units	Notes
Reference plane	GND if possible		See note 1
Trace Impedance	50	Ω	±20%
Max Trace Delay	19 (120)	mm (ps)	See note 3

Note: 1. If GND reference is not feasible, as may be the case with GSSG stack-up, keep the routing distance very short and have GND areas/traces surrounding the DDR\_COMP\_PU/PD traces.

- 2. Use reference platform layout as a guideline for routing & location of the DDR\_COMP\_PU/PD resistors.
- 3. Avoid routing signal traces directly below and in parallel with this critical rail.

### Table 33. DRAM VREF\_DQ/CA & ZQ Routing Requirements

Parameter	Requirement	Units	Notes
Reference Plane	GND if possible		See note 1
Max Capacitance	5	pF	VREF & ZQ only - See note 2
Trace Spacing	3х	Dielectric	To other signals
Max Trace Delay	Minimum		See note 3

Note: 1. If GND reference not feasible, keep routing distance very short & have GND areas/traces next to rails.

2. Maximum external load capacitance on ZQ pin, including package, PCB, resistor & DRAM device(s).

- 3. Use reference platform layout as a guideline for routing & location of bypass caps & resistors (ZQ & VREF).
- 4. Avoid routing signal traces directly below and in parallel with this critical rail.
- 5. Locate capacitors & resistors related to VREF & ZQ very near associated DRAM balls.

Ball Name	Туре	Termination	Description
DDR_COMP_PU	А	34Ω, 1% to VDDIO_DDR	DRAM Compensation Pull-up. See termination requirement
DDR_COMP_PD	А	34Ω, 1% to GND	DRAM Compensation Pull-down: See termination requirement
VDDIO_DDR	Ρ		DRAM Interface I/O Power Rail: Connect to 1.35V supply for DDR3L
VDDIO_DDR_MCLK	Р		DRAM Clock I/O Power Rail: Connect to 1.35V supply for DDR3L
VDDIO_DDR_HS	Р		DRAM Interface High Speed Power Rail: Connect to 1.05V supply

### Table 34. Miscellaneous Tegra DDR Connections

Table 35. Miscellaneous DDR3L Connections

DDR3L Ball Name	Туре	Termination	Description
VREF_DQ VREF_CA	A	Resistor Divider with one end to 1.35V & other end to GND - Recommend one per DRAM. See note under Connection diagram.	DRAM Voltage Reference Data & Command/Address: Connect both VREF(CA) and VREF(DQ) pins of DRAM each to center of voltage divider described in Termination column.
ZQ0, ZQ1	А	240Ω, 1% to GND	DRAM Zero Compensation pins: Connect each ZQ[1:0] pin to a



# DDR3L Ball Name Type Termination Description UDD, VDDQ P Image: Separate resistor and then to GND as described in Termination column VDD, VDDQ P DRAM Power Rails: Connect to same source as VDDIO\_DDR VSS, VSSQ P DRAM Ground pins: Connect to GND

### 3.3.2 LPDDR3

Figure 19. LPDDR3, 2 x 32, 178-pin Connections



Note: See the Power Decoupling Guidelines" section for power rail decoupling and filter requirements for Tegra .






The following table shows the connections from TK1 out to the two LPDDR3 DRAM devices. The symbol used in the reference schematics is a modified version of the default pin out shown in the Data Sheet. The tables include columns that contain the default pin out, Jetson TK1 symbol ball number, the net name used to connect to the DRAM, which device the net is going to, the DDR ball number and finally the ball name. All of these should be duplicated on a design. The same symbol ball out, same net names associated with each ball, etc. should be used to ensure the connections match and can be easily verified against the table and/or reference design

Tegra	Tegra Default	Jetson Symbol	LPDDR3	DDR	DDR	DDR	Tegra	Tegra Default	Jetson Symbol	LPDDR3	DDR	DDR	DDR
Ball #	Ball Name	Ball Name	Net Name	Device	Ball #	Ball Name	Ball #	Ball Name	Ball Name	Net Name	Device	Ball #	Ball Name
G14	DDR CLK	DDR CLK	DDR0 CLKP	1	.J3	СК Р	A8	DDR DO16	DDR DO18	DDR DO[22]	1	E9	DO14
H14	DDR CLK N	DDR CLK N	DDR0_CLKN	1	12	CK N	B8	DDR DO17	DDR DO16		1	D9	D015
H18	DDR_CLKB	DDR_CLKB	DDR1_CLKP	2	13	CK P	C6	DDR DO18	DDR DO17	DDR DO[17]	1	F10	D09
G18	DDR CLKB N	DDR CLKB N	DDR1_CLKN	2	12	CK N	E6				1	FQ	DQ10
E14				1	52		A7				1	E11	DQ10
E14	DDR_AU	DDR_AZ	DDRU_A[7]	1	EZ E2	CAF	A/	DDR_DQ20	DDR_DQ22	DDR_DQ[20]	1		DQ12
D14	DDR_AT	DDR_A5	DDRU_A[5]	I	F3	CA5	AO	DDR_DQ21	DDR_DQ19	DDR_DQ[19]	1	F8	DUTT
E15	DDR_A2	DDR_WE_N	NC	-	-	-	D6	DDR_DQ22	DDR_DQ21	DDR_DQ[16]	1	FII	DQ8
E12	DDR_A3	DDR_A4	NC	-	-	-	F6	DDR_DQ23	DDR_DQ20	DDR_DQ[21]	1	E10	DQ13
D12	DDR_A4	DDR_A1	DDR0_A[4]	1	M3	CA4	C8	DDR_DQS2P	DDR_DQS2P	DDR_DQS2P	1	G10	DQS1_P
F12	DDR_A5	DDR_A9	DDR0_A[2]	1	N2	CA2	D8	DDR_DQS2N	DDR_DQS2N	DDR_DQS2N	1	G11	DQS1_N
C12	DDR_A6	DDR_A8	DDR0_A[3]	1	N3	CA3	B6	DDR_DM2	DDR_DM2	DDR_DM[2]	1	G8	DM1
F14	DDR_A7	DDR_A7	DDR0_A[0]	1	R2	CA0	G12	DDR_DQ24	DDR_DQ29	DDR_DQ[31]	1	B8	DQ31
D15	DDR_A8	DDR_RAS_N	DDR0_A[1]	1	P2	CA1	H12	DDR_DQ25	DDR_DQ31	DDR_DQ[30]	1	B9	DQ30
B12	DDR A9	DDR A6	NC	-	-	-	A11	DDR DQ26	DDR DQ25	DDR DQ[24]	1	C11	DQ24
D18	DDR A10	DDR A13	DDR1 A[0]	2	R2	CA0	E11	DDR DQ27	DDR DQ26	DDR DQ[26]	1	C9	DQ26
G17	DDR A11	DDR A B3	DDR1_A[7]	2	F2	CA7	A10	DDR DO28	DDR DO30		1	C8	D027
A16	DDR A12	DDR A15	DDR1 A[4]	2	M3	CA4	B11	DDR DO29	DDR DO27		1	B11	DO28
C20	DDR A13	DDR A14		2	D2	CAS	F11	DDR DO30			1	B10	DQ20
E17				2	E2	CA6	D11				1	C10	DQ27
E10				2	D2	CA1					1	D10	DOS 20
EIG	DDR_AID			2	PZ	CAI		DDR_DQ33P	DDR_DQ33P	DDR_DQ33P	1	DIU	
H17	DDR_A_B3	DDR_A_B5	DDK1_A[9]	2	C2	CA9	GTT	DDR_DQS3N	DDR_DQS3N	DDR_DQS3N		DIT	DUS_3N
E20	DDR_A_B4	DDR_A_B4	NC	-	-	-	C11	DDR_DM3	DDR_DM3	DDR_DM[3]	1	D8	DM3
F17	DDR_A_B5	DDR_BA2	NC	-	-	-	G21	DDR_DQ32	DDR_DQ34	DDR_DQ[45]	2	E10	DQ13
F18	DDR_BA0	DDR_A12	DDR1_A[2]	2	N2	CA2	A21	DDR_DQ33	DDR_DQ35	DDR_DQ[43]	2	F8	DQ11
D20	DDR_BA1	DDR_A11	DDR1_A[5]	2	F3	CA5	E21	DDR_DQ34	DDR_DQ32	DDR_DQ[44]	2	E11	DQ12
H15	DDR_BA2	DDR_A10	DDR1_A[3]	2	N3	CA3	F20	DDR_DQ35	DDR_DQ38	DDR_DQ[40]	2	F11	DQ8
C14	DDR_CAS_N	DDR_A0	DDR0_A[8]	1	D2	CA8	G20	DDR_DQ36	DDR_DQ36	DDR_DQ[41]	2	F10	DQ9
G15	DDR_RAS_N	DDR_A3	DDR0_A[9]	1	C2	CA9	D21	DDR_DQ37	DDR_DQ37	DDR_DQ[47]	2	D9	DQ15
C15	DDR WE N	DDR CAS N	DDR0 A[6]	1	E3	CA6	B21	DDR DQ38	DDR DQ33	DDR DQ[42]	2	F9	DQ10
F15	DDR RESET N	DDR RESET N	NC	-	-	-	C21	DDR DQ39	DDR DQ39	DDR DQ[46]	2	E9	DQ14
B14	DDR CSO N	DDR CS1 N	DDR0_CS1_L	1	14	CS1 N	H21	DDR_DOS4P	DDR DOS4P	DDR DOS6P	2	G10	DOS 1P
A12	DDR_CS1_N	DDR_CS0_N	DDR0_0DT0	1	18	ODTO	H20	DDR_DOS4N	DDR_DOS4N	DDR_DOS6N	2	G11	DOS 1N
B18	DDR CS BO N	DDR ODT B1	DDR1_CS0_L	2	13	CSO_N	F21	DDR DM4	DDR DM4	DDR_DM[6]	2	G8	DM1
A19	DDR CS B1 N	DDR CS BO N	NC	-	-	-	D24	DDR DO40	DDR DO45	DDR DO[53]	2	R9	DO21
Δ13	DDR_CKE0	DDR_CKE0	DDR0_CKE1	1	КЛ	CKE1	C24				2	то	D017
Δ1/	DDR_CKE1	DDR_CKE1	DDR0_CKE0	1	K3	CKEO	E27				2	R11	DO23
A14	DDD CKE BO	DDR_CKE BO	DDR0_CKE0	2	KA	CKE1	A24				2	TR	DQ25
R20	DDD CKE D1	DDD CKE D1	DDR1_CKEN	2	K4 V2	CKED	F24				2	T10	DQ10
D20	DDR_CKE_DT	DDR_CRE_DT	DDR1_CKEU	2 1	K3 1.2	CKEU	E20				2		DQ18
AID D1F	DDR_ODT1	DDR_ODT1	DDRU_C3U_L	1	L3	C30_N	D20	DDR_DQ45	DDR_DQ40		2	КО T11	DQ20
B15	DDR_ODTI	DDR_ODTI	NC	-	-	-	A25	DDR_DQ46	DDR_DQ47	DDR_DQ[51]	2	111	DQ19
C18	DDR_OD1_B0	DDR_OD1_B0	DDR1_OD10	2	78	ODTO	A26	DDR_DQ47	DDR_DQ42	DDR_DQ[54]	2	110	DQ22
A18	DDK_OD1_B1	DDR_CS_B1_N	DDR1_CS1_L	2	L4	CS1_N	C26	DDR_DQS5P	DDR_DQS5P	DDR_DQS4P	2	P10	DQS_2P
							D26	DDR_DQS5N	DDR_DQS5N	DDR_DQS4N	2	P11	DQS_2N
							B24	DDR_DM5	DDR_DM5	DDR_DM[4]	2	P8	DM2
A3	DDR_DQ0	DDR_DQ7	DDR_DQ[3]	1	T11	DQ19	A22	DDR_DQ48	DDR_DQ54	DDR_DQ[35]	2	N11	DQ3
A4	DDR_DQ1	DDR_DQ6	DDR_DQ[7]	1	R11	DQ23	E24	DDR_DQ49	DDR_DQ55	DDR_DQ[38]	2	M10	DQ6
B5	DDR_DQ2	DDR_DQ0	DDR_DQ[6]	1	R10	DQ22	A23	DDR_DQ50	DDR_DQ50	DDR_DQ[32]	2	P9	DQ0
C2	DDR_DQ3	DDR_DQ3	DDR_DQ[0]	1	T8	DQ16	C23	DDR_DQ51	DDR_DQ52	DDR_DQ[33]	2	N9	DQ1
B3	DDR_DQ4	DDR_DQ4	DDR_DQ[2]	1	T10	DQ18	B23	DDR_DQ52	DDR_DQ48	DDR_DQ[34]	2	N10	DQ2
B2	DDR_DQ5	DDR_DQ1	DDR_DQ[4]	1	R8	DQ20	G23	DDR_DQ53	DDR_DQ49	DDR_DQ[37]	2	M9	DQ5
C3	DDR DQ6	DDR DQ5	DDR DQ[1]	1	T9	DQ17	F24	DDR DQ54	DDR DQ53	DDR DQ[39]	2	M11	DQ7
A5	DDR DO7	DDR DO2	DDR DO[5]	1	R9	D021	H23	DDR DO55	DDR DO51	DDR DO[36]	2	M8	DO4
C5	DDR DOSOP	DDR DOSOP	DDR DOSOP	1	P10	DOS 2P	F23	DDR DOS6P	DDR DOS6P	DDR DOS5P	2	110	DOS OP
D5	DDR DOSON	DDR DOSON	DDR DOSON	1	P11	DOS 2N	D23	DDR DOSAN	DDR DOSAN	DDR DOS5N	2	111	DOS ON
C1	DDR DMO	DDR DMO		1	D8	DM2	E23	DDR DM6			2	18	DM0
0				1	N10		D27				2	R11	0028
C9 E0				1	M10	DQ2	027				2	CO	DQ20
F9	DDR_DQ9	DDR_DQ13		1	WITU DO	DQb	029	DDR_DQ57			2	011	DQ20
68	DDR_DQ10	DDR_DQ10		1	P9	000	027	DDR_DQ58	DDR_DQ57		2		0024
F8	DDR_DQ11	DDR_DQ14	DDR_DQ[9]		119	DQI	A29	DDR_DQ59	DDR_DQ62	DDR_DQ[61]	2	RIO	0029
E9	DDR_DQ12	DDR_DQ8	DDR_DQ[12]	1	M8	DQ4	C31	DDR_DQ60	DDR_DQ56	DDR_DQ[63]	2	B8	DQ31
A9	DDR_DQ13	DDR_DQ9	DDR_DQ[11]	1	N11	DQ3	A27	DDR_DQ61	DDR_DQ59	DDR_DQ[59]	2	C8	DQ27
D9	DDR_DQ14	DDR_DQ15	DDR_DQ[15]	1	M11	DQ7	C30	DDR_DQ62	DDR_DQ58	DDR_DQ[62]	2	B9	DQ30
E8	DDR_DQ15	DDR_DQ12	DDR_DQ[13]	1	M9	DQ5	A28	DDR_DQ63	DDR_DQ63	DDR_DQ[57]	2	C10	DQ25

Table 36 DRAM Pin Multiplexing Option (LPDDR3, 2 x 32, 178-pin)



	Tegra Ball #	Tegra Default Ball Name	Jetson Symbol Ball Name	LPDDR3 Net Name	DDR Device	DDR Ball #	DDR Ball Name	Tegra Ball #	Tegra Default Ball Name	Jetson Symbol Ball Name	LPDDR3 Net Name	DDR Device	DDR Ball #	DDR Ball Name
Γ	G9	DDR_DQS1P	DDR_DQS1P	DDR_DQS1P	1	L10	DQS_0P	B30	DDR_DQS7P	DDR_DQS7P	DDR_DQS7P	2	D10	DQS_3P
Γ	H9	DDR_DQS1N	DDR_DQS1N	DDR_DQS1N	1	L11	DQS_0N	B29	DDR_DQS7N	DDR_DQS7N	DDR_DQS7N	2	D11	DQS_3N
Γ	B9	DDR_DM1	DDR_DM1	DDR_DM[1]	1	L8	DM0	B27	DDR_DM7	DDR_DM7	DDR_DM[7]	2	D8	DM3

Note: The DDR pin remapping must be followed exactly as shown above.

#### LPDDR3, x32 Design Guidelines

Note: The topology for each signal must be followed exactly as shown in the figures included for each signal group. The Requirements are 32-bit channel except the DDR\_CLK/DDR\_CLK\_N to DDR\_CLKB/DDR\_CLKB\_N requirement.

Figure 21. LPDDR3, x32/x64 DQ, DQS, DQM Topology



#### Table 37. LPDDR3, x32 Data Signal Group Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency / Data Rate	933 / 1866	MHz/Mbps	See note 1
Switching Period (T)	0.5	Т	
Тороlоду	Direct		
Configuration / Device Organization	1 - 2	load(s)	1 to 2 die per package per channel
Termination (VTT & ODT)	None		
Reference Plane	GND		
Max PCB breakout length	6.35	mm	
Via GND/Signal Return - Max Separation (Signal to Reference)	< 3.8 (24)	mm (ps)	See Note 2
Capacitance			
Min Input Capacitance Min / Max	1 / 1.8	pF	per load
Input Capacitance Delta (DQS_P/N) Min / Max (DQ/DM) Min / Max	0 / 0.2 -0.25 / 0.25	pF	per load
Impedance/Spacing			
Trace Impedance: DQ/DQM DQS Single Ended / Differential	40 45 / 80	Ω	±15%
Trace Spacing Microstrip / Stripline	3x / 2x	dielectric	
Max Trace Lengths/Delays			
Max Trace Length/Delay (PCB Main Trunk) Long Channel Short Channel	46.04 (290) 33.34 (210)	mm (ps)	Absolute
Skew Matching			
Max Trace Length/Delay Skew between DQ/DM & DQS	1.575 (10)	mm (ps)	Reference to DQS with DQ (+/-) tolerance



Parameter	Requirement	Units	Notes
Max Trace Length/Delay Skew between DQSP & DQSN	0.32 (2)	mm (ps)	Absolute
Max Trace Length/Delay Skew between DQS & CLK PCB Main Trunk (DQS) vs + PCB Main Trunk (CLK)	6.35 (30)	mm (ps)	Reference to CLK with DQS (+/-) tolerance
Max Trace Length/Delay Skew from any DQ to any other DQ (within byte)	3.18 (20)	mm (ps)	Absolute. See Note 3
Max Trace Length/Delay Skew from any DQ/DM/DQS byte to byte within 32-bit channel	9.53 (60)	mm (ps)	Absolute. See Note 3
Max Via Count			
Max Number of Vias	2		See Note 4
General DQ/DM/DQS Routing Considerations			
DQ/DM/DQS in each byte should be kept on same layer			

Note: 1. Max frequency is target. Actual frequency may depend on characterization results, and achievable PLL frequency used to clock the EMC block.

- 2. Up to 4 signal vias can share a single GND return via
- 3. If the DQ:DQS skew requirement is violated, the DQ:DQ requirement must still be maintained.

Table 38.	LPDDR3,	x32 Data	Signal	Group	Connections
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Signal Name	Туре	Termination	Description	1				
DDR_DQ[63:0] DDR_DM[7:0] DDR_DQS[7:0]P/N	I/O O DIFF I/O	No VTT or ODT (On-Die Termination) Required	<ul> <li>bata: Connect to DQ pins of all DRAMs (see table below)</li> <li>bata Mask: Connect to DM pins on DRAMs (see table below)</li> <li>bata Strobes: Connect to DQSxP/DQSxN pins of all DRAM (table be Byte Lanes (Groupings) per channel</li> <li>bata</li> <li></li></ul>				table below) Data Strobe	
			DQ[7:0] DQ[15:8] DQ[23:16] DQ[31:24]	DM0 DM1 DM2 DM3	DQS0P/N DQS1P/N DQS2P/N DQS3P/N	DQ[39:32] DQ[47:40] DQ[55:48] DQ[63:56]	DM4 DM5 DM6 DM7	DQS4P/N DQS5P/N DQS6P/N DQS7P/N

Note: The Tegra DRAM ball names may not correspond to the signal brought out on that ball. Use the DRAM Pin Multiplexing table to select the correct Tegra ball to connect to each DRAM ball.

#### Figure 22. LPDDR3, x32 Address, Command & Control Topology [Direct Connect]

Single Die/Load LPD	DR3 Device	D	ual Die/Load LPD	DR3 Device
Tegra Main trunk	LPDDR3 Die (1)	Т	egra Main trunk	LPDDR3 Die #1 Die #2

#### Table 39. LPDDR3, x32 Address/Command/Control Signal Routing Requirements

Parameter		Requirement	Units	Notes
Max Frequency / Data Rate	Add/Cmd Ctrl	933 / 1866 933 / 933	MHz/Mbps	Note 1
Switching Period (T)	Add/Cmd / Ctrl	0.5 / 1	Т	
Тороlоду		Direct		

Parameter	Requirement	Units	Notes
Configuration / Device Organization Add/Cmd Ctrl	1 - 2 1	load(s)	1 to 2 die per package per channel
Reference Plane	GND		
Max PCB breakout length	6.35	mm	
Via GND/Signal Return - Max Separation (Signal to Reference)	< 3.8 (24)	mm (ps)	See Note 2
Capacitance			
Input Capacitance Min / Max	0.7 / 1.3	pF	
Input Capacitance Delta Min / Max	-0.2 / 0.2	pF	
Impedance/Spacing			
Trace Impedance	40	Ω	±15%
Trace Spacing Microstrip / Stripline	3x / 2x	dielectric	
Max Trace Lengths/Delays			
Max Trace Length/Delay (PCB Main Trunk) Long Channel Short Channel	46.04 (290) 33.34 (210)	mm (ps)	Absolute
Skew Matching			
Max Trace Length/Delay Skew between Addr/Cmd/Ctl & Clk	6.35 (40)	mm (ps)	Reference to CLK with Add/Cmd/CtI (+/-) tolerance
Max Trace Length/Delay Skew from any Add/Cmd/Ctl to any other Add/Cmd/Ctl (within channel)	3.18 (20)	mm (ps)	Absolute
Max Via Count			
Max Number of Vias	2		See Note 3

Note: 1. Max frequency is target. Actual frequency may depend on achievable PLL frequency used to clock the EMC block.

- 2. Up to 4 signal vias can share a single GND return via
- Cmd/Add includes DDR[1:0]\_A[9:0]. DDR\_A\_B[5:3], DDR\_A[15:10], DDR\_RAS/CAS/WE/RESET are not used.
- 4. Ctl includes DDR[1:0]\_CS[1:0], DDR[1:0]\_CKE[1:0], DDR[1:0]\_ODT[1:0].

Table 40. LPDDR3, x32 Command/Address & Control Group Connections

Signal Name	Туре	Termination	Description
DDR0_A[9:0] DDR1_A[9:0]	0		Address 9:0: Connect to CA 9:0 pins of lower 32-bit DRAM
DDR_A[15:10], DDR_A_B[5:3], DDR_BA[2:0], DDR_RAS, DDR_CAS, DDR_WE, DDR_RESET	0		Unused DRAM pins for LPDDR3: Leave NC
DDR0_CS[1:0] DDR1_CS[1:0]	0		Chip Select: Connect to CSx pins of all DRAM in Channel 0 Chip Select: Connect to CSx pins of all DRAM in Channel 1
DDR0_CKE[1:0] DDR1_CKE[1:0]	0		Clock Enable: Connect to CKEx pin of all DRAM in Channel 0 Clock Enable: Connect to CKEx pin of all DRAM in Channel 1
DDR0_ODT[1:0] DDR1_ODT[1:0]	0		On-Die Termination Ctrl: Connect to ODTx pin of all DRAM in Channel 0. On-Die Termination Ctrl: Connect to ODTx pin of all DRAM in Channel 1.



Note: The Tegra DRAM ball names may not correspond to the signal brought out on that ball. Use the DRAM Pin Multiplexing table to select the correct Tegra ball to connect to each DRAM ball.

#### Figure 23. LPDDR3, x32/x64 LPDDR3, Clock Topology



#### Table 41. LPDDR3, x32/x64 Clock Routing Requirements

Parameter	Requirement	Units	Notes		
Max Frequency	933	MHz	See Note 1		
Switching Period (T)	0.5	Т			
Тороlоду	Direct				
Configuration / Device Organization	1 - 2	load(s)	1 to 2 die per package per channel		
Reference Plane	GND				
Max PCB breakout length	6.35	mm			
Via GND/Signal Return - Max Separation (Signal to Reference)	< 3.8 (24)	mm (ps)	See Note 2		
Capacitance					
Input Capacitance	0.7 / 1.4	pF			
Input Capacitance Delta Min / Max	0 / 0.15	pF			
Impedance/Spacing					
Trace Impedance Single Ended / Differential	45 / 80 50 / 90	Ω	±15%		
Trace Spacing Microstrip / Stripline	3x / 2x	dielectric			
Max Trace Lengths/Delays					
Max Trace Length/Delay (PCB Main Trunk) Long Channel Short Channel	39.69 (250) 26.99 (170)	mm (ps)	Absolute		
Skew Matching					
Max Trace Length/Delay Skew CLK/CLK_N	0.32 (2)	mm (ps)	Absolute		
Max Trace Length/Delay Skew from DDR_CLK/DDR_CLK_N (Channel 0 or 1) to DDR_CLKB/DDR_CLKB_N (Channel 1 or 0)	4.76 (30)	mm (ps)	Absolute		
Max Via Count					
Max Number of Vias	2		See Note 3		

Note: 1. Max frequency is target. Actual frequency may depend on achievable PLL frequency used to clock the EMC block.

2. Up to 4 signal vias can share a single GND return via



#### Table 42. LPDDR3, x32 Clock Connections

Signal Name	Туре	Termination	Description
DDR_CLK_P/N	DIFF OUT		<b>Differential Clock:</b> Connect <b>CLK_P/CLK_N</b> pins of DRAM for Channel 0.
DDR_CLKB_P/N	DIFF OUT		Differential Clock B: Connect to CLK_P/CLK_N pins of DRAM for Channel 1.

# Note: DDR\_COMP\_PU/PD, VDDIO\_DDR\_HS,DRAM VREF\_DQ/CA & ZQ routing requirements can be found at the end of the DDR3L section

#### Table 43. Miscellaneous Tegra LPDDR3 Connections

Ball Name	Туре	Termination	Description
DDR_COMP_PU	А	40.2Ω, 1% to <b>VDDIO_DDR</b>	DRAM Compensation Pull-up. See termination requirement
DDR_COMP_PD	А	40.2Ω, 1% to GND	DRAM Compensation Pull-down: See termination requirement
VDDIO_DDR	Р		DRAM Interface I/O Power Rail: Connect to 1.2V supply
VDDIO_DDR_HS	Р		DRAM Interface High Speed Power Rail: Connect to 1.05V supply

#### Table 44. Miscellaneous LPDDR3 Connections

Ball Name	Туре	Termination	Description
VREF(CA) VREF(DQ)	A	Resistor divider. One end to 1.2V & other to GND. See note under Connection diagram.	LPDDR3 Command/Address & Data Voltage References: Connect both VREF(CA) and VREF(DQ) pins of module each to center of voltage divider described in Termination column.
VDD1	Р		LPDDR3 Core 1: Connect VDD1 pins of module to 1.8V supply
VDD2, VDDCA, VDDQ	Ρ		DRAM Core 2, Command/Address/Data IO rails: Connect to 1.2V supply
ZQ0, ZQ1	A	240Ω, 1% to GND	LPDDR3 Zero Compensation pins: Connect each ZQ[1:0] pin to a separate resistor and then to GND as described in Termination column
VSS, VSSQ. VSSCA	Р		LPDDR3 Core, Cmd/Add & Data GND pins: Connect to GND.

# 3.3.3 Common DRAM Routing Guidelines

Guideline	Description / Illustration			
Avoid routing over voids in the GND reference in the ball-out area. The figure to the right shows a "GOOD" example, where the GND continues between the BGA balls with the DDR CLK routing staying over the GND. Avoid the "BAD" example, where the GND has a break and the signal passes over this break (or Void). This guideline should be used for DDR Clock, and if possible Data/DQS/DM.	GOOD			
Separate critical DDR traces (CLK, DQ/DQS/DM, VREF, COMP, etc.) from other signal traces or unrelated power areas or power supply components				



Table 45. DRAM Interface Package Delays

Signal Name	Ball	Pkg									
	#	Delay									
		(ps)			(ps)			(ps)			(ps)
DDR_A_B3	H17	53	DDR_CS_B0_N	B18	78	DDR_DQ28	A10	82	DDR_DQ58	C27	73
DDR_A_B4	E20	80	DDR_CS_B1_N	A19	77	DDR_DQ29	B11	70	DDR_DQ59	A29	86
DDR_A_B5	F17	55	DDR_CS0_N	B14	76	DDR_DQ3	C2	77	DDR_DQ6	C3	91
DDR_A0	E14	63	DDR_CS1_N	A12	84	DDR_DQ30	F11	53	DDR_DQ60	C31	97
DDR_A1	D14	65	DDR_DM0	C1	79	DDR_DQ31	D11	71	DDR_DQ61	A27	82
DDR_A10	D18	56	DDR_DM1	B9	85	DDR_DQ32	G21	58	DDR_DQ62	C30	86
DDR_A11	G17	51	DDR_DM2	B6	76	DDR_DQ33	A21	85	DDR_DQ63	A28	88
DDR_A12	A16	81	DDR_DM3	C11	76	DDR_DQ34	E21	55	DDR_DQ7	A5	84
DDR_A13	C20	64	DDR_DM4	F21	69	DDR_DQ35	F20	63	DDR_DQ8	C9	71
DDR_A14	E17	64	DDR_DM5	B24	79	DDR_DQ36	G20	56	DDR_DQ9	F9	55
DDR_A15	E18	55	DDR_DM6	F23	67	DDR_DQ37	D21	70	DDR_DQSON	D5	79
DDR_A2	E15	63	DDR_DM7	B27	76	DDR_DQ38	B21	73	DDR_DQS0P	C5	77
DDR_A3	E12	57	DDR_DQ0	A3	87	DDR_DQ39	C21	70	DDR_DQS1N	H9	63
DDR_A4	D12	66	DDR_DQ1	A4	77	DDR_DQ4	B3	78	DDR_DQS1P	G9	60
DDR_A5	F12	59	DDR_DQ10	G8	84	DDR_DQ40	D24	77	DDR_DQS2N	D8	71
DDR_A6	C12	62	DDR_DQ11	F8	71	DDR_DQ41	C24	71	DDR_DQS2P	C8	69
DDR_A7	F14	57	DDR_DQ12	E9	65	DDR_DQ42	E27	71	DDR_DQS3N	G11	64
DDR_A8	D15	67	DDR_DQ13	A9	84	DDR_DQ43	A24	93	DDR_DQS3P	H11	66
DDR_A9	B12	76	DDR_DQ14	D9	59	DDR_DQ44	E26	62	DDR_DQS4N	H20	62
DDR_BA0	F18	51	DDR_DQ15	E8	70	DDR_DQ45	B26	79	DDR_DQS4P	H21	59
DDR_BA1	D20	65	DDR_DQ16	A8	84	DDR_DQ46	A25	85	DDR_DQS5N	D26	76
DDR_BA2	H15	55	DDR_DQ17	B8	71	DDR_DQ47	A26	92	DDR_DQS5P	C26	75
DDR_CAS_N	C14	61	DDR_DQ18	C6	79	DDR_DQ48	A22	83	DDR_DQS6N	D23	63
DDR_CKE_B0	A20	78	DDR_DQ19	E6	73	DDR_DQ49	E24	63	DDR_DQS6P	E23	65
DDR_CKE_B1	B20	78	DDR_DQ2	B5	75	DDR_DQ5	B2	83	DDR_DQS7N	B29	87
DDR_CKE0	A13	82	DDR_DQ20	A7	89	DDR_DQ50	A23	78	DDR_DQS7P	B30	85
DDR_CKE1	A14	81	DDR_DQ21	A6	86	DDR_DQ51	C23	78	DDR_ODT_B0	C18	74
DDR_CLK	G14	57	DDR_DQ22	D6	67	DDR_DQ52	B23	70	DDR_ODT_B1	A18	77
DDR_CLK_N	H14	59	DDR_DQ23	F6	88	DDR_DQ53	G23	52	DDR_ODT0	A15	79
DDR_CLKB	H18	78	DDR_DQ24	G12	57	DDR_DQ54	F24	67	DDR_ODT1	B15	71
DDR_CLKB_N	G18	80	DDR_DQ25	H12	61	DDR_DQ55	H23	83	DDR_RAS_N	G15	46
DDR_COMP_PD	D17	67	DDR_DQ26	A11	70	DDR_DQ56	D27	74	DDR_RESET_N	F15	52
DDR_COMP_PU	C17	73	DDR_DQ27	E11	57	DDR_DQ57	C29	77	DDR_WE_N	C15	65

# 3.3.4 Component Vias (also called or Rat-T Vias)

Component vias are used to replace T-points which are unstable & tend to move around on the board layout. The designer must keep relocating the T-points back to the correct location. Component vias stay in the location they are placed & are easier to manage when routing or creating topologies.

Creating Component Vias

A component via is simply a single-pin IC symbol. For Allegro, a component via is created for each via in the library including test points & via pad-stack data is used for the IC pin. For Concept schematic capture, create one component via symbol & add a different component-via JEDEC type in Parts table. Once the schematic has been loaded, the designer will be able to select which component via is best for the design.

When to use component vias

A component via is used wherever a T-point is needed, or when trying to control trace delays mid-route. The net topology is controlled by dividing it up into multiple segments. Each section has a maximum delay associated. In addition, after each T, branches also have relative delay (skew) requirements. To control these items, component vias are added to divide the nets into main trunk & the two branches as shown below:



The above example indicates the location of the component vias (CV1). Each via must be added to the schematic before loading it into the layout file. The final outcome is shown below.

#### Table 46. Example Segment Measurements using Component Vias

Max Delays	Measurement (mm)	Max Skews	Measurement (mm)
Tegra to CV1	45		
CV1 to DRAM 1	12	CV1 to DRAM1 verses CV1 to DRAM2	6
CV1 to DRAM 2	12		

The cost of using component vias is the time required to add each via to the schematic and place them on the layout. The benefits are many though:

- Flowing T-point issue is eliminated
- Easier to see the how topology is to be routed & to perform routing checks& to see topology in Constraint manager
- Easier to move component vias to maximize routing strategy
- Easier to relocate components & busses to different areas of board

# 3.4 USB/PCIe/SATA Interfaces

Tegra has three USB 2.0 controllers.

- USB2 Controller #1 can drive a USB 2.0 PHY, required at a minimum to support Device mode for USB Recovery mode. Host mode can also be supported.
- USB2 Controller #2 can be configured to drive either a second USB 2.0 PHY or an HSIC interface. Only
  Host mode is supported for the PHY.
- USB2 Controller #3 can also be configured to drive either a PHY or HSIC interface. Only Host mode is supported for the PHY.

The XUSB3 controller supports up to two USB 3.0 interfaces and can also be configured to drive the USB 2.0 PHYs.

Two PCIe controllers supporting up to 5 PCI lanes (two interfaces) and a single SATA controller/interface is provided. See the table below for possible USB 3.0, PCIe & SATA lane mappings.

Use Case	USB 3.0	PCIe	SATA	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	SATA
Jetson TK1				USB_SS#0	Unused	PCIe#1_0		PCIe#0_0	SATA
1	2	1 x1 & 1 x2	1	USB_SS#0	USB_SS#1	PCIe#1_0	PCIe#0_1	PCIe#0_0	SATA
2	1	1 x4	1	USB_SS#0	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0	SATA
3	0	1 x1 & 1 x4	1	PCIe#1_0	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0	SATA
4	1	1 x1 & 1 x4	0	PCIe#1_0	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0	USB_SS#1

Table 47. USB 3.0, PCIe & SATA Lane Mapping Use Cases



## Figure 24 TK1 USB Connections



Note:

1. Ensure bulk capacitance meets USB 3.0 requirements for Type A connector.

- 2. Any ESD solution must also maintain signal quality & meet USB requirements.
- 3. See Reference design for details on ID connections.
- 4. If USB Wake w/USB DP/DN mechanisms is required for connected devices, AVDD\_USB must be powered in Deep Sleep. If USB 3.0 Wake on USB3\_TXx/RXx (Using USB mechanisms) is required, HVDD\_PEX must be powered in Deep Sleep. AVDDIO\_PEX & DVDDIO\_PEX do not need to be powered & are recommended to be off in Deep Sleep.
- 5. See the "Power Decoupling Guidelines" section for power rail decoupling and filter requirements.
- 6. Connector used must be USB-IF certified.



#### Table 48. USB 2.0 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency (High Speed) Bit Rate/UI period/Frequency	480/2.083/240	Mbps/ns/MHz	
Max Loading High Speed / Full Speed / Low Speed	10 / 150 / 600	pF	
Reference plane	GND		
Breakout Region Impedance	Min width/spacing		
Trace Impedance Diff pair / Single Ended	90 / 50	Ω	±15%
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Max Trace Delay Microstrip / Stripline	1280 (~8) / 1150 (~7)	ps (in)	See Note 2
Max Intra-Pair Skew between USBx_DP & USBx_DN	7.5	ps	See Note 2

Note: 1. Up to 4 signal vias can share a single GND return via.

- 2. Max Trace Delay & Max Trace Delay Skew matching must include substrate pin delays unless otherwise specified
- 3. Default USB drive strength, slew rate, termination values are fused at the factory for each Tegra device. Default fused settings will meet USB Electrical specification using max trace delays listed in table above. If adjustments to the settings are required, they MUST be done as an offset to default values instead of overwriting those values. Consult AE & CE team for assistance

#### **USB 3.0 Design Guidelines**

The requirements following apply to the USB 3.0 controller PHY interface (USB3\_RX0N/P & USB3\_TX0N/P)

Table 49.	USB 3.0 Interface	Signal Routing	Requirements
10010 171	000 0.0 111011000	orginal noathig	noquin onnonito

Parameter	Requirement	Units	Notes
Data Rate / UI period	5.0 / 200	Gbps / ps	
Max Number of Loads	1	load	
Termination	90 differential	Ω	On-die termination at TX & RX
Reference plane	GND		
Breakout Region Max length	7.62	mm	4x dielectric spacing preferred
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See note 1
Trace Spacing Microstrip / Stripline To Ref plane & capacitor pad To unrelated high-speed signals	4x / 3x 5x / 3x 5x / 4x	dielectric	
Max Trace Length	152	mm	See Note 2
Max PCB Via distance from BGA ball	7.62	mm	
Max Intra-Pair Skew (RX/TXN to RX/TXP)	0.15 (1)	mm (ps)	See Note 2
Intra-pair matching between subsequent discontinuities	0.15 (1)	mm (ps)	See note 3
Via placement (GND Via distance)	< 1x	Diff via pitch	See note 3
Max Number of Vias	4		
Via stub length	< 0.4	mm	



Parameter	Requirement	Units	Notes
AC coupling capacitor	0.1	uF	Discrete 0402
AC coupling capacitor Location	< 8 (53)	mm (ps)	From adjacent discontinuities (ex, connector, AC cap)
SMT Connector GND Voiding			GND plane under signal pad should be voided. Size of void should be the same size as the pad.

Note: 1.

- Up to 4 signal vias can share a single GND return via Include Package & PCB routing delays for Max trace delays and max trace delay skew parameters. 2.
- Recommend trace length matching to <1ps before Vias or any discontinuity to minimize common mode 3. conversion.
- 4. Place GND Vias as symmetrically as possible to data pair Vias.

#### Table 50. Additional USB 3.0 Routing Guidelines

TX & RX routing to minimize Xtalk.	<ol> <li>Ideal solution is to breakout TX &amp; RX breakout on different layers.</li> <li>If in same layer, recommend not interleaving TX &amp; RX traces</li> </ol>					
	Inter-pair spacing for minimizing FEX	I (TInter-S.	Inter-p for min	air spacing imizing FEXT		
	TX 🛋 🛋 🛋				RX RX	
	Inter-S <sub>FEX</sub>	σ Inter-pair s for minimizir	pacing ng NEXT			
	If routing on the same layer, increase in a) Use the recommended trace dimen below.	iter-pair spacing	g using the meth ut & main route	nods below. & length limita	ation from the table	
	PCB	Н	DI	Stan	ndard	
	Line Type	Stripline-St	ackup=GSSG	Micro-strip		
	Section	breakout	main trace	breakout	main trace	
	Trace Widths	1x	1.32x	1.32x	1.32x	
	Inter-S (Within Pair)	1.167x	1.68x	1.32x	1.32x	
	Inter-S <sub>NEXT</sub> (Between TX/RX)	4.85x	>3x	1.32x	>4x	
	Inter-S <sub>FEXT</sub> (Between TX/TX or RX/RX)	>1x	>1x	1x	>1x	
	Length	<11mm	<170mm-L <sub>brk</sub>	<4mm	<170mm-L <sub>brk</sub>	
	<ul> <li>all Nx values in the table are for trace spacing, in terms of the minimum dielectric height         * L<sub>brk</sub> is the breakout trace length         Notes:         If the TX/RX sequence cannot be non-inerleaved in the breakout, all the inter-pair spacing should follow the rule of inter-SNEXT. Having different trace dimensions for breakout &amp; main route provides optimal near-end Xtalk suppression. Strongly suggest to have non-interleaved sequence in the main     </li> </ul>					
	<ul> <li>Since breakout route is much shorter than main route, min trace width should be selected for breakout trace to increase inter-pair spacing.</li> <li>Having different trace dimensions for breakout &amp; main route provide optimal near-end Xtalk</li> </ul>					
	breakout region.	norm serpentin	ie i outing for in	па-рап экем С		



Y-Pattern Via If TX & RX vias are near each other, place the pairs orthogonally as shown in figure to the right.	Recommended Placement	TX & RX vias placed in alighment increases Xtalk
Serpentine Guideline	a) Use more serpentine runs to minimize the intra-pair spacing variation & provide more spacing to other adjacent traces.	<ul> <li>b) Do not compensate for inter-pair skew to avoid increasing trace length</li> </ul>
Connector	Connector used must be USB-IF certified	

## Table 51. USB\_REXT Routing Requirements

Parameter	Requirement	Units	Notes
Reference plane	GND if possible		See note 1
Trace Impedance	50	Ω	±15%
Max Trace Delay	75	ps	Include only PCB routing delay

Note: 1. If GND reference is not feasible, as may be the case with GSSG stack-up, keep the routing distance as short as possible & have GND areas/traces next to the USB\_REXT trace.

2. Use reference platform layout as a guideline for routing & location of USB\_REXT resistor.

3. Avoid routing signal traces directly below and in parallel with these critical rails.

#### Table 52. PEX\_TERMP Routing Requirements (required for USB3 or PCIe)

Parameter	Requirement	Units	Notes
Reference plane	GND if possible		See note 1
Trace Impedance	50	Ω	±15%
Max Trace Delay	75	ps	Include only PCB routing delay

Note: 1. If GND reference is not feasible, keep the routing distance as short as possible & have GND areas/traces next to the PEX\_TERMP traces.

- 2. Use reference platform layout as a guideline for routing & location of PEX\_TERMP resistor.
- 3. Avoid routing signal traces directly below and in parallel with these critical rails.



# Common USB Routing Guidelines

#### Guideline

If routing to USB device or USB connector includes a flex or 2<sup>nd</sup> PCB, the total routing including all PCBs/flexes must be used for the max trace & skew calculations.

Keep critical USB related traces such as USB3\_TX/RX, USB\_REXT & PEX\_TERMP etc. away from other signal traces or unrelated power traces/areas or power supply components

#### Table 53. USB 2.0 Signal Connections

Ball Name	Туре	Termination	Description
USB[2:0]_DP USB[2:0]_DN	DIFF I/O	$90\Omega$ common-mode chokes close to connector. ESD Protection between choke & connector on each line to GND	<b>USB Differential Data Pair:</b> Connect to USB Micro AB connector D+/D- pins.
USBO_VBUS	A		USB Bus 5V Supply: Connect to +USB2_VBUS_SW (VBUS supply for Micro AB connector) through load switch.
USBO_ID	A	100 $\Omega$ series resistor. 100k $\Omega$ pull-up to +5V_SYS & ESD Protection near connector	<b>USB Identification</b> : Connect to USB Micro AB ID pin. Also connect ID pin from connector to PMU PWM_CLK2 pin through FETs. See reference design for details.
USB_REXT	А	1K $\Omega$ , 1% to GND (see Note)	External Reference: Connect through resistor to GND
AVDD_USB	Р		USB PHY Power Rail: Connect to +3.3V_LP0 supply
AVDD_PLL_UTMIP	Ρ	$30\Omega$ @100MHz ferrite bead to 1.8V	USB PHY PLL Power Rail: Connect to +1.8V_VDDIO_LPO_OFF supply through filter

#### Table 54. USB 2.0 Interface Package Delays

Signal Name	Ball #	Pkg Delay (ps)	Signal Name	Ball #	Pkg Delay (ps)
USBO_DN	AH20	80	USB2_DN	AE20	64
USB0_DP	AJ20	80	USB2_DP	AD20	63
USB1_DN	AF20	74	USB_REXT	AL19	76
USB1_DP	AG20	74			

Table 55. US	B 3.0 Signal	Connections
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Ball Name	Туре	Termination	Description
USB3_TXON/P	DIFF I/O	Series 0.1uF caps close to connector. ESD Protection between cap & conn. to GND	USB 3.0 Differential Transmit Data Pair: Connect to USB 3.0 connector.
USB3_RXON/P	DIFF I/O	ESD Protection between cap & conn. to GND	USB 3.0 Differential Receive Data Pairs: Connect to USB 3.0 connector.
PEX_TERMP	А	2.49KΩ, 1% to GND	PCIe/USB3 Calibration: Connect through resistor to GND
DVDDIO_PEX	Ρ		PCIe /USB PHY Digital Power Rail: Connect to 1.05V supply
AVDDIO_PEX	Ρ		PCIe/USB PHY Analog Power Rail: Connect to 1.05V supply
AVDD_PEX_PLL	Ρ		PCIe/USB PHY PLL Power Rail: Connect to 1.05V supply
HVDD_PEX	Ρ		PCIe/USB 3.0 High Voltage Power Rail: Connect to 3.3V supply
HVDD_PEX_PLL_ E	Ρ		PCIe/USB 3.0 PLL High Voltage Power Rail: Connect to 3.3V supply
VDDIO_PEX_CTL	Р		PCIe/USB Control Block Rail: Connect to 3.3V supply.



#### Table 56. USB 3.0 ESD Protection Device Requirements

Parameter	Requirement	Units	Notes
Recommended ESD protection device	SEMTECH RClamp0524p		
Max Reverse Stand-Off Voltage ( $V_{RWM}$ )	5	V	Any I/O pin to GND
Min Reverse Breakdown Voltage (V <sub>BR</sub> )	6	V	It=1mA - Any I/O pin to GND
Max Reverse Leakage Current (I <sub>R</sub> )	1	uA	$V_{\text{RWM}}{=}5V,~T{=}25C$ – Any I/O pin to GND
Max Clamping Voltage (V <sub>c</sub> )	15	V	$I_{\mbox{\scriptsize PP}}\mbox{-}1A,\mbox{ tp}\mbox{=}8/20\mbox{us}$ - Any I/O pin to GND
Typ/Max Junction Capacitance (C <sub>j</sub> )	0.3/0.4	pF	$V_R$ =0V, f=1MHz - Between I/O pins
Max Junction Capacitance (C <sub>j</sub> )	0.8	pF	$V_R=0V$ , f=1MHz - Any I/O pin to GND

Note: The junction capacitance of ESD devices has an effect on signal integrity. Choose components with low capacitance with package optimized for high speed links. SEMTECH Rclamp0524p has been well verified with its 0.3pF capacitance. See detailed characteristics above.

## Table 57. USB 3.0 Common Mode Choke Requirements (Optional - Only used if rare EMI issue is seen)

Parameter		Requirement	Units	Notes
Common mode impedance (at 100MHz) Mi Ma	in ix	65 90	Ω	
Rdc (Max)		0.3	Ω	
Differential mode impedance Z0 at 2.5GHz		90	Ω	+/- 15%
Differential insertion loss ( Sdd21  at 2.5GHz)		<2.22	dB	
Common-to-Common insertion loss ( Scc21  at 2.5GHz)		>19.2	dB	

#### Table 58. USB 3.0 Interface Package Delays

Signal Name	Ball #	Pkg Delay (ps)	Signal Name	Ball #	Pkg Delay (ps)
USB3_RX0N	AL21	43	PEX_USB3_RX1N	AL23	46
USB3_RX0P	AK21	43	PEX_USB3_RX1P	AK23	46
USB3_TX0N	AJ21	36	PEX_USB3_TX1N	AG21	26
USB3_TX0P	AH21	35	PEX_USB3_TX1P	AF21	26
PEX_TERMP	AL22	54			

Note: If the USB 3.0 interface is coming from the SATA balls, get the package delays from the table at the end of the SATA section.



Tegra contains two PCIe controllers that support up to 5 lanes, and 2 separate interfaces. These narrow, highspeed interfaces can be used to connect to a variety of high bandwidth devices. The example below is from the Jetson TK1 design. See the table "USB 3.0, PCIe & SATA Lane Mapping Use Cases" at the beginning of the "USB/PCIe/SATA Interfaces" section for other PCIe options.



# Figure 25. Jetson PCIe Connections

- Notes: If PCIe is routed to a connector, only AC caps on Tegra TX lines are required & should be near the connector. Device TX AC caps are assumed to be located on the device side of the connector. If routed directly to a peripheral on the board, AC caps are needed for both the Tegra TX lines (connected to device RX) & Device TX lines (connected to Tegra RX). The AC caps should be located near each TX device (Tegra TX or device TX).
  - See the "Power Decoupling Guidelines" section for power rail decoupling and filter requirements



Table 59.	PCIe Interface	Signal Routing	Requirements

Parameter	Requirement	Units	Notes
Max Frequency / UI Period	5.0 / 200	Gbps / ps	2.5GHz, half-rate architecture
Тороlоду	Point-point		Unidirectional, differential
Configuration / Device Organization	1	Load	
Max Load (per pin)	N/A	pF	See return loss spec in PCIe 2.0 spec
Termination	50	Ω	To GND Single Ended for P & N
Reference plane	GND		
Breakout Region Width/line spacing pair spacing	4 10	Mils	Maximum pair spacing of 500 mils
Trace Impedance differential / Single Ended	90 45 - 60	Ω	±15%
Pair to Pair Trace Spacing Stripline / Microstrip	3x / 4x	Dielectric	
Tx to Rx spacing			Recommend Tx & Rx signals routed on separate layers w/GND between for isolation. See note 1
Spacing to planes/cap. pads Stripline / Microstrip	3x / 4x	Dielectric	
Max Trace Length/Delay	10″ (1700)	in (ps)	For trace with loss <=0.4dB/in @ 2.5GHz. See note 2 & 3
Max Within Pair Trace Delay Skew	1	ps	See note 3 & 4
Max Pair to Pair Trace Delay Skew (RX to RX or TX to TX - Within Link)	600	ps	See note 3 & 4
Trace Width Options	4/5/6	Mils	See note 2

Note: 1. If routing in the same layer is necessary, route group TX & RX separately wo/mixing RX/TX routes & keep distance between nearest TX/RX trace & RX to other signals 3x RX-RX separation

2. For with trace loss >= 0.7dB/in @ 2.5GHz, the max trace length should be 7.5 inches. To reduce trace loss, ensure the loss tangent of the dielectric material & roughness of the metal are tightly controlled.

3. Include Package & PCB routing delays for Max trace delays and max trace delay skew parameters.

4. Do trace length matching before the vias to transition to different layers or any discontinuity to minimize common mode conversion

Table 60. Additional PCIe Interface Signal Routing Guidelines

Maximum # of Vias	Maximum of 4 vias per TX traces and 2 vias per RX trace.
Routing signals over the antipad	Not allowed
Routing over voids	When signal pair approaches vias, the maximal trace length across the void on the plane is 50mil;
Serpentine line rule	For microstrip line, minimal spacing between each turn is 4x dielectric; For stripline, it is 3x dielectric height (3x of thinner of above & below)
PTH (Plated Through-hole) Vias	Keep GND via as close as possible
Ground sliver between BGA pads	Remove ground slivers between BGA pads & feedthrus to via to reduce the capacitive loading of BGA pad
DC Blocking capacitor location	Place DC blocking capacitors within 0.3" of the connector if one exists, or near the receiver.
Ground plane under AC cap pads	Remove GND plane under AC blocking capacitor pads. If board has ICT pads, remove plane under



	those as well. Void is size of pad + ring equal to dielectric thickness.
Serpentine line rule	<ul> <li>Avoid tight bends</li> <li>No 90deg bends; impact to loss and jitter budgets</li> <li>Keep angles &gt;= 135deg (a)</li> <li>maintain adequate air gap</li> <li>A &gt;= 4x trace width</li> <li>Lengths of B, C &gt;= 1.5x trace width</li> <li>Serpetines length is at least 3w for jog</li> </ul>
Keep critical PCIe/SATA relate power traces/areas or power	ed traces such as PCIe/SATA_TX/RX, PCIe/SATA_TERMP etc. away from other signal traces or unrelated supply components

**PEX\_TERMP** is shared by PCIe & USB3 blocks. See routing requirements in USB section.

Table 61. PCIe Signal Connections
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Ball Name	Туре	Termination	Description
PEX_USB3_TXOP/N PEX_TX[4:2]P/N	DIFF OUT	Series 0.1uF caps close to connector or close to Tegra if direct device connection.	<b>Differential Transmit Data Pairs:</b> Connect to PCIe <b>TX_P</b> pins of PCIe device/connector through AC cap according to supported configuration. See Note 1.
PEX_USB3_RXOP/N PEX_RX[4:2]P/N	DIFF IN	Series 0.1uF caps only if direct device connection. Place close to PCIe device.	<b>Differential Receive Data Pairs</b> : Connect to PCIe <b>RX_P</b> pins of PCIe device/connector through AC cap according to supported configuration.
PEX_L[1:0]_CLKREQ _N	I		PCIe Clock Request: Connect to CLKREQ pins on device/connector(s)
PEX_L[1:0]_RST_N	I		PCIe Reset: Connect to PERST pins on device/connector(s)
PEX_WAKE_N	I	100KΩ pullup to +3.3V_LPO supply	PCIe Wake: Connect to WAKE pins on device or connector
PEX_TERMP	А	2.49KΩ, 1% to GND	PCIe Calibration: Connect to GND through termination (resistor)
PEX_REFCLKP/N	DIFF OUT		PCIe Reference Clock: Unused, connect to GND. See note 1.
PEX_TSTCLKP/N	DIFF OUT		PCIe Test Clock: Unused - Leave NC
DVDDIO_PEX	Р		PCIe Digital I/O Power Rail: Connect to 1.05V supply
AVDDIO_PEX	Ρ		PCIe Analog I/O Power Rail: Connect to 1.05V supply through bead
AVDD_PEX_PLL	Ρ		PCIe Analog Power Rail for Transmit PLL: Connect to 1.05V supply
HVDD_PEX	Р		PCIe High Voltage Power Rail: Connect to 3.3V supply
HVDD_PEX_PLL_E			PCIe High Voltage Power Rail for Transmit PLL: Connect to 3.3V supply
VDDIO_PEX_CTL	Р		PCIe Control I/O Block Power Rail: Connect to 3.3V supply



Table 62. PCIe Interface Package Delays

Signal Name	Ball #	Pkg Delay (ps)	Signal Name	Ball #	Pkg Delay (ps)	Signal Name	Ball #	Pkg Delay (ps)	Signal Name	Ball #	Pkg Delay (ps)
PEX_CLK1N	AG26	73	PEX_USB3_TX1N	AG21	26	PEX_RX3N	AK24	45	PEX_TX4N	AH26	39
PEX_CLK1P	AF26	72	PEX_USB3_TX1P	AF21	26	PEX_RX3P	AL24	45	PEX_TX4P	AJ26	39
PEX_CLK2N	AC27	67	PEX_RX2N	AE21	39	PEX_TX3N	AG23	29	PEX_TERMP	AL22	54
PEX_CLK2P	AC26	64	PEX_RX2P	AD21	38	PEX_TX3P	AF23	28			
PEX_USB3_RX1N	AL23	46	PEX_TX2N	AJ23	37	PEX_RX4N	AL26	49			
PEX_USB3_RX1P	AK23	46	PEX_TX2P	AH23	36	PEX_RX4P	AK26	48			

# 3.4.3 SATA

A Gen 2 SATA controller is implemented on Tegra. The example below is from the Jetson design which brings this interface to a standard SATA connector & provides control for an LED & power connector.



Figure 26. Jetson SATA Connections

Notes: - AC caps are used on the for both the Tegra TX & RX lines. The AC caps should be located near the connector.

- See the "Power Decoupling Guidelines" section for power rail decoupling and filter requirements



# **NVIDIA**.

#### Table 63. SATA Signal Routing Requirements

Parameter	Requirement	Units	Notes		
Max Frequency Bit Rate / UI	3.0 / 333.3	Gbps / ps	1.5GHz		
Topology	Point to point, unidirectional, differential				
Configuration / Device Organization	1	load			
Max Load (per pin)	0.5	pf			
Termination	100	Ω	On die termination		
Reference plane	GND				
Breakout Region Impedance Trace Width / Line separation	4 4	mils			
Trace Impedance Differential Pair / Single Ended	90 55	Ω	±15%		
Pair to Pair Trace Spacing Stripline / Microstrip	3x / 3x	Dielectric			
Max Trace Delay	1360 (8)	ps (in)	See Note 1 & 2		
Max Intra-Pair Trace Delay Skew	1	ps	See Note 1 & 2		
Keep critical PCIe/SATA related traces such as PCIe/SATA_TX/RX, PCIe/SATA_TERMP etc. away from other signal traces or unrelated power traces/areas or power supply components					

Note: 1. If routing to SATA device or SATA connector includes a flex or 2<sup>nd</sup> PCB, the total routing including all PCBs/flexes must be used for the max trace & skew calculations

2. Include Package & PCB routing delays for Max trace delays and max trace delay skew parameters.

#### Table 64. SATA\_TERMP Routing Requirements

Parameter	Requirement	Units	Notes
Reference plane	GND		
Trace Impedance	50	Ω	±15%
Max Trace Delay	75	ps	Include only PCB routing delay

#### Table 65. Additional SATA Interface Signal Routing Guidelines





Preferred routing layer for SMT SATA Connector	For SMT connector AC caps should be on top layer. PCB trace connecting AC caps & SATA connector, & Tegra to AC caps should be on top layer as microstrip. Tegra Microstrip - AC Cap Connector TX/RX Top side Signal Path Microstrip - Bottom side
Recommendations for SMT Connector	GND plane under signal pad should be voided for better differential mode & common mode return loss. Size of void should be 5 mils larger than SMT SATA connector pad in each direction.
Delay Matching	Do trace delay matching before the vias to transition to different layers
Maximal # of vias	Maximum of 4 vias per TX traces and 2 vias per RX trace
Routing over voids	Where signal pair approaches vias, maximal trace length across void on plane is 1.27mm
Serpentine line rule	For microstrip line, minimal spacing between each turn is 4x dielectric; For stripline, it is 3x dielectric height (3x of thinner of above & below)
DC Blocking capacitor location	Place DC blocking capacitors less than 12.5mm from connector.
DC Blocking capacitor GND removal	Remove plane underneath the DC blocking capacitor pads. If board has ICT pads, remove plane under those as well. Void is size of pad + ring equal to dielectric thickness.
Anti-pad for connector pin	Not required if PCB trace connecting AC cap & connector is on bottom layer. In case PCB trace connecting AC cap & connector is on top layer, increase size of anti-pads for connector pins to 35mm & void out ground planes whenever there are solder pads

Table 66.	SATA Signal	Connections
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Ball Name	Туре	Termination	Description
SATA_LO_TXP/N	DIFF OUT	Series 0.01uF caps close to connector or close to Tegra if direct device connection.	<b>Differential Transmit Data Pair</b> : Connect to <b>SATAN/P</b> /pins of SATA device/connector through termination (capacitor)
SATA_LO_RXP/N	DIFF IN	Series 0.01uF caps only if direct device connection. Place close to SATA device.	<b>Differential Receive Data Pair:</b> Connect to <b>SATAN/P</b> pins of SATA device/connector through termination (capacitor)
SATA_TERMP	А	2.49KΩ, 1% to GND	SATA Calibration: Connect to GND through termination (resistor)
SATA_TSTCLKP/N	DIFF OUT		SATA Test Clock: Unused - Leave NC
VDDIO_SATA	Р		SATA I/O Power Rail: Connect to 1.05V supply.
AVDD_SATA_PLL	Р		SATA Analog Power Rail for Transmit PLL: Connect to 1.05V supply
HVDD_SATA	Р		SATA High Voltage Power Rail: Connect to 3.3V supply

Signal Name	Ball #	Pkg Delay (ps)	Signal Name	Ball #	Pkg Delay (ps)
SATA_L0_RXN	AH27	44	SATA_L0_TXN	AK27	50
SATA_L0_RXP	AJ27	44	SATA_L0_TXP	AL27	49
SATA_TERMP	AL25	55			



Tegra supports two HSIC interfaces. These 2-pin, 1.2V CMOS interfaces can connect to compatible modems, Wi-Fi controllers, USB PHYs, etc. The example below from the Jetson design brings the HSIC1 interface to the General Expansion Header.

# Figure 27. Jetson HSIC connections



- Note: VDDIO\_HSIC must remain powered in Deep Sleep if connected device must maintain connection. Powering off/on VDDIO\_HSIC will require re-enumeration of the HSIC interface.
  - Series resistors near Tegra are recommended for early builds for use as test points, or possible signal conditioning
  - See the "Power Decoupling Guidelines" section for power rail decoupling and filter requirements

#### **HSIC Design Guidelines**

Table 68.	<b>HSIC Interface</b>	Signal	Routing	Requirements

Parameter	Requirement	Units	Notes
Max Frequency (High Speed) Bit Rate / UI period / Freq.	480 / 2.083 / 240	Mbps / ns / MHz	
Input Buffer Loading	1 - 5	pF	
Reference plane	GND		
Max PCB breakout delay	17	ps	
Trace Impedance	50	Ω	±15%
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Trace spacing Microstrip / Stripline	4x / 3x	dielectric	
Trace Delay Min / Max	133 / 667	ps	See Note 2
Max Trace Delay Skew between HSIC[2:1]_STROBE & DATA	15	ps	See Note 2

Note: 1. Up to 4 signal vias can share a single GND return via

2. Include Package & PCB routing delays for Max trace delays and max trace delay skew parameters.

#### Table 69. HSIC\_REXT Routing Requirements

Parameter	Requirement	Units	Notes		
Reference plane	GND if possible		See note 1		
Trace Impedance	50	Ω	±15%		
Max Trace Delay         140         ps         Include Package & PCB routing delays					
Keep HSIC related traces including HSIC_REXT away from other signal traces or unrelated power traces/areas or power supply components					



- Note: 1. If stack-up makes GND reference difficult, keep routing distance very short & have GND areas next to HSIC\_REXT trace.
  - 2. Use reference platform layout as a guideline for routing & location of HSIC\_REXT resistor.
  - 3. Avoid routing signal traces directly below and in parallel with these critical rails.

Table 70. HSIC Signal Connections

Ball Name	Туре	Termination	Description
HSIC[2:1]_STROB E	1/0	$0\Omega$ series resistors (for early designs)	HSICx Strobe: Connect to STROBE pins on HSIC device
HSIC[2:1]_DATA	I/0	Same as above	HSICx Data: Connect to DATA pins on HSIC device
HSIC_REXT	А	1.0KΩ, 1% to GND	HSIC External Reference Resistor. Connect to termination to GND

Table 71. HSIC Interface Package Delays

Signal Name	Ball #	Pkg Delay (ps)
HSIC1_DATA	AF18	54
HSIC1_STROBE	AE18	55
HSIC2_DATA	AG18	57
HSIC2_STROBE	AD18	82
HSIC_REXT	AH18	58

# 3.5 Display

Tegra supports eDP, LVDS or DSI for embedded displays as well as HDMI for external displays. The Jetson TK1 design provides access to the eDP/LVDS display options on the Display/Touch Expansion header.

Figure 28: Jetson Display Block Diagram





Jetson supports up to a 4-lane single-link LVDS interface or up to a 4-lane eDP interface. The maximum resolution supported with LVDS is 1920x1200 @ 60fps (24bpp color depth). With eDP, the maximum supported using the full 4 lanes is 3840x2160 @ 60fps. LVDS and eDP are multiplexed on the same pins. See LVDS/eDP Pin Assignment Options table below for pin assignments for each interface.

Tegra Ball	LVDS (3-lane)	LVDS (4 lane)	eDP
LVDS0_TXD0_P/N	LVDS lane 0	LVDS lane 0	eDP lane 2
LVDS0_TXD1_P/N	LVDS lane 1	LVDS lane 1	eDP lane 1
LVDS0_TXD2_P/N	LVDS lane 2	LVDS lane 2	eDP lane 0
LVDS0_TXD3_P/N	N/A	LVDS lane 3	N/A
LVDS0_TXD4_P/N	LVDS clock lane	LVDS clock lane	eDP lane 3

Table 72. eDP/LVDS Pin Assignment Options





- Notes: Filters on the DSI signals are not recommended. If EMI is a concern, other solutions, such as using PCB GND layers or other shielding is preferred. If EMI devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing & Vil/Vih requirements at the receiver & not introduce glitches on the signal edges. Any ESD solution must also maintain signal quality and meet requirements for the frequencies supported by the design.
  - See the "Power Decoupling Guidelines" section for power rail decoupling and filter requirements.



Figure 30: LVDS 4-Lane Connection Example



- Note: Filters on the DSI signals are not recommended. If EMI is a concern, other solutions, such as using PCB GND layers or other shielding is preferred. If EMI devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing & Vil/Vih requirements at the receiver & not introduce glitches on the signal edges. Any ESD solution must also maintain signal quality and meet requirements for the frequencies supported by the design.
  - See the "Power Decoupling Guidelines" section for power rail decoupling and filter requirements.

CDI Dobigii Culucililos	eDP	Design	Guidelines
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Table 73.	eDP	(HBR2)	) Main	Link S	ignal F	Routing	Req	uireme	ents
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Parameter	Requirement	Units	Notes
Max Data Rate (per data lane) HBR2 / HBR / RBR	5.4 / 2.7 / 1.62	Gbps	
Min UI HBR2 / HBR / RBR	185 / 370 / 617	ps	
Number of Loads	1	load	
Тороlоду			Point-Point, Differential, Unidirectional
Termination	100	Ω	On die at TX/RX
Reference plane	GND		
Max PCB breakout length	7.63 (0.3)	mm (in)	
Trace Impedance Diff pair / Single Ended	90 / 45-60	Ω	±15%
Stripline Routing for Main Trunk			
Max trace length from Tegra TX pin to connector RBR/HBR HBR2 Max Propagation Delay - HBR2	215 (8.5) 165 (6.5) 1137	mm (in) mm (in) ps	See Note 1 175ps/inch delay assumption for stripline
Max number of signal vias RBR, HBR / HBR2	4 / 2		HBR2: One more test via right after AC cap OK
PCB pair-to-pair spacing	3x	dielectric height	3x of the thinner of above and below



Parameter	Requirement	Units	Notes
PCB main link to AUX Spacing	3х	dielectric height	3x of the thinner of above and below
Max stub length on the Vias Allowed			Rout below core to minimize stub length
Microstrip Routing for Main Trunk			
Max trace length from Tegra TX pin to connector HBR2 (5x / 7x spacing) Max Propagation Delay - HBR2 (5x / 7x spacing)	215 (8.5) 127 (5) / 152.4 (6) 750 / 900	mm (in) mm (in) ps	See Note 1 150ps/inch delay assumption for microstrip
Max number of signal vias RBR, HBR / HBR2	4 / 2		HBR2: One more test via right after AC cap OK
PCB pair-pair spacing RBR,HBR / HBR2	4x / 5x-7x	dielectric height	
PCB main link to AUX Spacing	5x	dielectric height	
Signal Skews (Stripline or Microstrip)			
Max Intra-pair (within pair) Skew	1	ps	See Note 1 & 2
Max Inter-pair (pair-pair) Skew	150	ps	See Note 1 & 2

Note: - Max Trace Delay & Max Trace Delay Skew matching must include substrate pin delays unless otherwise specified

- Recommend doing trace length matching to <1ps before vias or any discontinuity to minimize common mode conversion

#### Table 74. Additional eDP Requirements/Recommendations

Parameter		Requirement	Units	Notes
Max PCB via distance from BGA	RBR/HBR HBR2	No requirement 7.63 (0.3)	mm (in)	
Max signal transition vias		2		Recommend = 2 for predominately stripline routing & </=n 4 for predominately microstrip routing.</td
Main Trunk routing		Stripline		Recommended
Max GND transition via distance		< 1x	diff pair pitch	For signals switching reference layers, add symmetrical ground stitching via near signal vias.
AC coupling cap		100	nF	Discrete 0402
Max Distance from AC cap to conn. I	rbr/Hbr Hbr2	No requirement 0.5	in	RBR and HBR: no requirement HBR2: less than 0.5 inch
AC cap pad voiding	RBR/HBR HBR2	No voiding required Voiding required		HBR2: Voiding the plane directly under the pad 3-4 mils larger than the pad size is recommended.
Connector voiding	RBR/HBR HBR2	No voiding required Voiding required		HBR2: Standard DP Connector: Voiding requirement is stack-up dependent. For typical stack-ups, voiding on the layer under the connector pad is recommended to be 5.7mil larger than the connector pad.
ESD protection device				ESD protection required to meet device testing beyond 2kV HMM (human metal model) direct pin injection test.



# Table 75. eDP Auxiliary Channel Signal Routing Requirements

Parameter	Requirement	Units	Notes
Termination, Reference plane, Max breakout, Impedance, Max trace length, Max Vias	Same as Main Link		
PCB pair-to-pair spacing Stripline/Microstrip	2x/3x	dielectric height	
Max Intra-pair (within pair) Skew	Same as Main Link		
Max Inter-pair (pair-pair) Skew	No requirement		

# Table 76. LVDS Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency / Bit Rate	135 / 945	MHz / Mbps	
Number of Loads	1	load	
Topology			Point-Point or Multi-drop, Differential, Unidirectional
Termination	100	Ω	At the receiver (on die or on board)
Reference Plane	GND		
Trace Impedance Diff pair / Single Ended	90 / 45-55	Ω	±15%
Max Trace Length Stripline / Microstrip	10 / 12	in	See Note 1
PCB pair-to-pair spacing Stripline / Microstrip	3x / 4x	dielectric height	3x of the thinner of above and below
Max Intra-pair (within pair) Skew	5	ps	See Note 1
Max Inter-pair (pair-pair) Skew	100	ps	See Note 1

Note: Include Package & PCB routing delays for Max trace delays and max trace delay skew parameters.

#### Table 77. LVDS Multi-drop Signal Routing Requirements

Parameter	Requirement	Units	Notes
Stub length	< 15	% (of rise time)	
External termination resistor	100	Ω	Placed at the far end (last receiver).
On chip termination receiver	90 ≤ ZL ≤ 132	Ω	Total load

#### Table 78. LVDS0\_RSET Routing Requirements

Parameter	Requirement	Units	Notes
Reference plane	GND if possible		See note 1
Trace Impedance	50	Ω	±15%
Max Trace Delay	40	ps	Include only PCB routing delay

# Note: If stack-up makes GND reference difficult, keep routing distance very short & have GND areas next to LVDS0\_RSET trace.



# Common eDP/LVDS Routing Guidelines

#### Guideline

If routing to eDP or LVDS device includes a flex or 2<sup>nd</sup> PCB, the max trace & skew calculations must include all the PCBs/flex routing

Keep critical eDP/LVDS related traces including differential clock/data traces & RSET trace away from other signal traces or unrelated power traces/areas or power supply components

#### Table 79. eDP Signal Connections

Ball Name	Туре	Termination	Description
LVDS0_TXD[4:0]_P/ N	0	eDP: Series 0.1uF capacitors	eDP/LVDS CLK/Data Lanes: See eDP/LVDS Pin Assignment Options table or diagrams for correct connection to display connector.
LVDSO_RSET	А	1KΩ, 1% to GND	eDP Current Reference: Connect to resistor to GND.
AVDD_LVDS0_IO	Р	Note 1	eDP IO Power Rail: Connect to 1.05V supply
AVDD_LVDS0_PLL	Ρ	Note 1	eDP Dedicated PLL Power Rail: Connect to 3.3V supply for eDP
DP_AUX_CH0_P/N	0	100K $\Omega$ pull-downs on both lines near Tegra, series 0.1uF capacitors, then 100K $\Omega$ pull-down on AUX_P & 100K $\Omega$ pull- up on AUX_N.	eDP Auxiliary Channel: Connect to AUX_CH_P/N on display connector.
DP_HPD	I/OD		eDP Hot Plug Detect: Connect to HPD on display connector.

Note: \_ DP\_AUX\_CH0\_P/N (I2C6) & DP\_HPD only supported when IF block powered by VDDIO\_HV is from 2.8-3.3V.

#### Table 80. LVDS Signal Connections

Ball Name	Туре	Termination	Description
LVDS0_TXD[4:0]_P/ N	0		<b>LVDS CLK/Data Lanes:</b> See eDP/LVDS Pin Assignment Options table or diagrams for correct connection to display connector.
LVDS0_RSET	А	1KΩ, 1% to GND	LVDS Current Reference: Connect to resistor to GND.
AVDD_LVDS0_IO	Р	Note 1	LVDS IO Power Rail: Connect to 1.05V supply
AVDD_LVDS0_PLL	Р	Note 1	LVDS Dedicated PLL Power Rail: Connect to 1.8V for LVDS.

Table 81. LVDS/eDP Interface Package Delays

Signal Name	Ball #	Pkg Delay (ps)	Signal Name	Ball #	Pkg Delay (ps)
LVDS0_TXD0N	AJ2	50	LVDS0_TXD3N	AG1	46
LVDS0_TXD0P	AJ3	51	LVDS0_TXD3P	AG2	47
LVDS0_TXD1N	AG3	44	LVDS0_TXD4N	AF3	38
LVDS0_TXD1P	AG4	45	LVDS0_TXD4P	AF4	38
LVDS0_TXD2N	AG5	30	LVDS0_RSET	AK3	46
LVDS0_TXD2P	AG6	30			



# 3.5.2 MIPI DSI

Tegra supports eight total MIPI DSI data lanes and two clock lanes, allowing up to two 4-lane interfaces. Each data channel has peak bandwidth up to 1.5Gbps.

Additional Functions:

- Tearing Effect input to allow the display controller to synchronize to panel drivers with their own timing controllers.
- Backlight PWM
- Various GPIOs to support display power sequencing, power management, etc.





- Note: Filters on the DSI signals are not recommended. If EMI is a concern, other solutions, such as using PCB GND layers or other shielding is preferred. If EMI devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing & Vil/Vih requirements at the receiver & not introduce glitches on the signal edges. Any ESD solution must also maintain signal quality and meet requirements for the frequencies supported by the design.
  - See the "Power Decoupling Guidelines" section for power rail decoupling and filter requirements.



MIPI DSI and CSI Design Guidelines

Table 82		CSI Interface	Signal	Routing	Requirements
	WIFT D3F &		Jiynar	Routing	Requirements

Parameter	Requirement	Units	Notes			
Max Frequency/Data Rate (per data lane)	750 / 1500	MHz/Mbps				
Number of Loads / Max Loading (per pin)	1 / 10	Load / pf				
Reference plane	GND or PWR		See Note 1			
Breakout Region Impedance Diff pair / Single Ended	90 / 45-55	Ω	±15%			
Max PCB breakout delay	48	ps				
Trace Impedance Diff pair / Single Ended	90 / 45-55	Ω				
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 2			
Trace spacing Microstrip / Stripline	2x / 2x	dielectric				
Max Trace Delay	1620	ps	See Note 3			
Max Intra-pair Skew	1	ps	See Note 3			
Max Trace Delay Skew between DQ & CLK	10	ps	See Note 3			
If routing to DSI or CSI device includes a flex or 2 <sup>nd</sup> PCB, the max trace & skew calculations must include all the PCBs/flex routing						
Keen critical DSI/CSI related traces including DSI/CSI clock	/data traces & RDN/RUP trace	s away from o	ther signal traces or unrelated			

Keep critical DSI/CSI related traces including DSI/CSI clock/data traces & RDN/RUP traces away from other signal traces or unrelated power traces/areas or power supply components

Note: 1. If PWR, 0.01uF decoupling cap required for return current

- 2. Up to 4 signal vias can share a single GND return via
- 3. Include Package & PCB routing delays for Max trace delays and max trace delay skew parameters.

#### Table 83. CSI\_DSI\_RDN/RUP Routing Requirements

Parameter	Requirement	Units	Notes
Reference plane	GND if possible		See note 1
Trace Impedance	50	Ω	±15%
Max Trace Delay	40	ps	Include only PCB routing delay

Note: 1. If stack-up makes GND reference difficult, keep routing distance very short & have GND areas next to CSI\_DSI\_RDN/RUP traces.

2. Use reference platform layout as a guideline for routing & location of CSI\_DSI\_RDN/RUP resistors.

3. Avoid routing signal traces directly below and in parallel with these critical rails.

Ball Name	Туре	Termination	Description
DSI_A_CLK_N/P	0		DSI Differential A Clock: Connect to CLKn & CLKp pins of receiver
DSI_A_D[3:0]_N/P	1/0		DSI Differential A Data Lanes: Connect to up to 4 sets of Dn & Dp pins of Primary DSI display
DSI_B_CLK_N/P	0		Differential B Clock: Connect to CLKn & CLKp pins of secondary receiver
DSI_B_D[3:0]_N/P	1/0		<b>Differential B Data Lanes:</b> Connect to up to 4 sets of <b>Dn &amp; Dp</b> pins of secondary DSI display, or second set of 4 lanes to primary display.

#### Table 84. MIPI DSI Signal Connections



Ball Name	Туре	Termination	Description
CSI_DSI_RDN	А	49.9Ω, 1% to GND	DSI/CSI Voltage Reference Pulldown:
CSI_DSI_RUP	А	453Ω, 1% to <b>1.2V</b>	DSI/CSI Voltage Reference Pull-up:
AVDD_CSI_DSI	Р		MIPI DSI & CSI Shared Power Rail: Connect to 1.2V supply

Table 85. DSI Interface Package Delays

Signal Name	Ball #	Pkg Delay (ps)									
DSI_A_CLK_N	AJ14	66	DSI_A_D2_N	AL15	75	DSI_B_D0_N	AH12	67	DSI_B_D3_N	AF12	55
DSI_A_CLK_P	AH14	66	DSI_A_D2_P	AK15	75	DSI_B_D0_P	AJ12	67	DSI_B_D3_P	AG12	56
DSI_A_D0_N	AK11	76	DSI_A_D3_N	AG14	56	DSI_B_D1_N	AE12	47	CSI_DSI_RDN	AG11	61
DSI_A_D0_P	AL11	75	DSI_A_D3_P	AF14	57	DSI_B_D1_P	AD12	48	CSI_DSI_RUP	AF11	61
DSI_A_D1_N	AD14	50	DSI_B_CLK_N	AJ11	68	DSI_B_D2_N	AL12	74			
DSI_A_D1_P	AE14	51	DSI_B_CLK_P	AH11	67	DSI_B_D2_P	AK12	73			

# 3.6 HDMI

A standard HDMI V1.4b interface is supported.





- Note: 1. The backdrive block associated w/AVDD\_HDMI is used to prevent current passing back through Tegra when the 3.3V supply is off, but the device is connected to a powered display.
  - 2. Any ESD solution must also maintain signal integrity & meet the HDMI requirements for the modes to be supported
  - 3. Ensure AVDD\_HDMI supply can handle >= 100mA as there can be an increase in power consumption for ~1second when the HDMI cable is unplugged from the display device before SW has a chance to disable the HDMI pads.



- 4. Filters on HDMI Clock/Data lines are not recommended. If EMI devices are necessary, they must be tuned to maximize signal quality, which must meet the HDMI specification for the modes to be supported.
- 5. See the "Power Decoupling Guidelines" section for power rail decoupling and filter requirements

HDMI Design Guidelines

Figure 33: HDMI Differential Clock & Data Topology



Table 86. HDMI Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Max Frequency		297	MHz	Data rate (1/UI) is ten times larger than the pixel frequency (1/T_pixel)
Тороlоду		Point to point		
Termination	At Receiver On-board	50 500	Ω	To 3.3V at receiver To GND near connector
Reference plane		GND		
Max Breakout Length / Delay		7.62 (52.5)	mm (ps)	
Trace Impedance	Diff pair / Single Ended	90 / 45-60	Ω	±15%
Trace spacing	Microstrip / Stripline	4x / 3x	dielectric	See Note 1
Max Trunk Delay (297)	Microstrip Stripline	114/4.5 (675) 114/4.5 (787)	mm/in (ps)	See Note 2 & 3
Max Trunk Delay (225)	Microstrip Stripline	254/10 (1500) 204/8 (1400)	mm/in (ps)	See Note 2 & 3
Max Trunk Delay (165)	Microstrip Stripline	320/12.5 (1870) 254/10 (1500)	mm/in (ps)	See Note 2 & 3
Max distance from ESD to connect	tor (Seg A)	12.7 (87)	mm (ps)	
Max distance from signal line to E	ESD pad (Seg B)	6.35 (37.5)	mm (ps)	Keep stub connecting ESD to signal trace very short or overlay pad on signal trace. See example layout figure below table)
Max Intra-Pair (within pair) Skew		1	ps	See Note 2 & 3
Max Inter-Pair (pair to pair) Skew	1	150	ps	See Note 2 & 3

Note: 1. Microstrip routing is recommended for HDMI due to limited eye height and has longer MAX length

2. Include Package & PCB routing delays for Max trace delays and max trace delay skew parameters.

3. If routing to HDMI connector includes a flex or 2<sup>nd</sup> PCB, the max trace delay & skew calculations must include all the PCBs/flex routing







Table 87.	Additional HD	MI Requirements	/Recommendations
	/ autonut no	mi negun cincinta	

Parameter	Requirement	Units	Notes
Max signal transition vias	2		Recommend = 2 for predominately stripline routing & </=n 4 for predominately microstrip routing.</td
Stripline routing			Recommend routing near bottom layer to minimize via stub lengths
GND transition via	< 1x	diff pair pitch	For signals switching reference layers, add symmetrical ground stitching via near signal vias. GND via distance should be < 1X diff pair via pitch
Padstack of signal via (pad/drill/antipad)	0.45/0.25/0.86	mm	Recommended to reduce capacitance and loss (Guideline intended for PTH - Plated Through-Hole Vias)
Connector voiding			Voiding GND below the signal lanes 5.7mil larger than the pin itself is recommended (see figure)
ESD protection device			ESD protection required to meet device testing beyond 2kV HMM (human metal model) direct pin injection test.
Filter Capacitor on 5V	100	pF	0402 size capacitor on the 5V output is required for EMI reduction
Routing Over void not allowed			Exception is anti-pad at connector pins which causes voids. Route traces w/min. void references.
Routing away from sources of noise			Keep critical HDMI related traces including differential clock/data traces & RSET trace away from other signal traces or unrelated power traces/areas or power supply components

#### Table 88. HDMI\_RSET Routing Requirements

Parameter	Requirement	Units	Notes
Reference plane	GND if possible		See note 1
Trace Impedance	50	Ω	±15%
Trace Spacing	2x	dielectric	
Max Trace Delay	75	ps	Include only PCB routing delay

Note: 1. If stack-up makes GND reference difficult, keep routing distance very short & have GND areas next to HDMI\_RSET trace.

2. Use reference platform layout as a guideline for routing & location of HDMI\_RSET resistor.

3. Avoid routing signal traces directly below and in parallel with these critical rails.



Table 89. HDMI Signal Connections

Ball Name	Туре	Termination (see note on ESD)	Description
HDMI_TXCN/P	0		HDMI Differential Clock: Connect to CN/CP pins on HDMI Connector
HDMI_TXD[2:0]N/P	0		HDMI Differential Data: Connect to D[2:0]+/- pins HDMI Connector
HDMI_INT	I	Series $1K\Omega$ resistor	HDMI Interrupt (Hot Plug Detect): Connect to HP_DET on HDMI Connector w/termination described.
HDMI_CEC	I/OD	See reference schematics for details	HDMI Consumer Electronics Control: Connect to CEC on HDMI Connector through circuitry shown in connection example.
HDMI_RSET	А	1KΩ, 1% to GND	HDMI Current Reference: Connect to resistor to GND.
AVDD_HDMI	Р	Dual FET back-drive blocking circuitry - See "HDMI Connection Example" diagram	HDMI I/O Power Rail: Connect to 3.3V supply gated by AVDD_HDMI_PLL (see note under connection figure)
AVDD_HDMI_PLL	Ρ		<b>HDMI PLL Power Rail:</b> Connect to $+1.05V$ ( $\leq 165MHz$ ) or $+1.2V$ (>165MHz) supply through FET (load switch) enabled by GPIO_PH7.
DDC_SCL/SDA	I/OD	120Ω@100mhz bead & 1.8KΩ pull-up resistor to +5V_HDMI supply each.	DDC Interface - Clock and Data: Connect to SCL/SDA on HDMI Connector w/termination described.
VDDIO_HV	Р		High Voltage Tolerant I/O Power Rail: Connect to +3.3V_LP0 supply.
+5V_HDMI		$120\Omega@100$ mhz bead & 0.1uF decoupling capacitor	HDMI 5V supply to connector: Connect through filter to +5V on HDMI Connector.

 Table 90.
 HDMI Interface Package Delays

Signal Name	Ball #	Pkg Delay (ps)									
HDMI_TXCN	AF5	29	HDMI_TXDON	AD5	29	HDMI_TXD1N	AD4	38	HDMI_TXD2N	AD2	49
HDMI_TXCP	AF6	29	HDMI_TXD0P	AD6	29	HDMI_TXD1P	AD3	39	HDMI_TXD2P	AD1	50
HDMI_RSET	AF2	43									

# 3.7 MIPI CSI (Camera)

Tegra supports three MIPI CSI interfaces, allowing a variety of device types and combinations to be supported. Up to two quad lane & one single lane connections are available. Each data channel has peak bandwidth of up to 1.2Gbps.

The figure below shows the configuration supported on the Jetson TK1 platform, supporting two CSI imagers (Camera #1 & #2). Camera #1 uses 4 CSI lanes (CSIA[1:0] & CSIB[1:0]). Camera #2 uses a single lane (CSIE[0]). Other combinations are possible, and listed in the CSI Configurations table.



Figure 35: Camera Connection Example



- Note: 1. Filters on CSI, MCLK & I2C signals are not recommended. If EMI is a concern, other solutions (PCB GND layers, external shielding, etc.) is preferred. If EMI devices are used, they must be tuned such that the signals meet the timing & electrical requirements of the related specification for the frequencies to be supported.
  - 2. If Tegra is providing flash control (as shown above), GPIO\_PBB[4] must be used.
  - 3. Care must be taken to ensure any ESD and/or EMI solution must support the frequencies required in the design.
  - 4. A privacy LED may be a requirement in some designs. Ensure the LED is on whenever the camera is active such that this cannot be disabled through software means.
  - 5. See the "Power Decoupling Guidelines" section for power rail decoupling and filter requirements.



# **NVIDIA**

Table 91. CSI Configurations (Including optional use of DSI\_B pins as additional CSI lanes)

Togra Ball Namos	CSI Signals	Camera 1	Camera 2 (> 1 Iane)	Stereo Rear-facing (dual 4-lane camera config. shown)		Camera 2 (1 Iane)
regra ban Names				Left RF	Right RF	
		up to x4	up to x4	up to x4	up to x4	x1
CSI_A_CLK_N/P	CSI_A_CLK_N/P	Г		Г		
CSI_A_D[1:0]_N/P	CSI_A_D[1:0]_N/P	Г		Г		
CSI_B_D[1:0]_N/P	CSI_B_D[1:0]_N/P	ſ		Г		
DSI_B_CLK_N/P	CSI_C_CLK_N/P		Г		Г	
DSI_B_D[1:0]_N/P	CSI_C_D[1:0]_N/P		Г		Г	
DSI_B_D[3:2]_N/P	CSI_D_D[1:0]_N/P		Г		ſ	
CSI_E_CLK_N/P	CSI_E_CLK_N/P					ſ
CSI_E_D_N/P	CSI_E_D_N/P					ſ

CSI Design Guidelines

## Table 92. MIPI CSI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency/Data Rate (per data lane)	750 / 1500	MHz/Mbps	
Number of Loads	1	load	
Max Loading (per pin)	10	pF	
Reference plane	GND or PWR		See Note 1
Breakout Region Impedance Diff pair / Single Ended	90 / 45-55	Ω	±15%
Max PCB breakout delay	48	ps	
Trace Impedance Diff pair / Single Ended	90 / 45-55	Ω	
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 2
Trace spacing Microstrip / Stripline	2x / 2x	dielectric	
Max Trace Delay	1620	ps	See Note 3
Max Intra-pair Skew	1	ps	See Note 3
Max Trace Delay Skew between DQ & CLK	10	ps	See Note 3

Note: 4. If PWR, 0.01uF decoupling cap required for return current

- 5. Up to 4 signal vias can share a single GND return via
- 6. Include Package & PCB routing delays for Max trace delays and max trace delay skew parameters.

## Table 93. CSI\_DSI\_RDN/RUP Routing Requirements

Parameter	Requirement	Units	Notes
Reference plane	GND if possible		See note 1
Trace Impedance	50	Ω	±15%



Parameter	Requirement	Units	Notes
Max Trace Delay	40	ps	Include only PCB routing delay

Note: 4. If stack-up makes GND reference difficult, keep routing distance very short & have GND areas next to CSI\_DSI\_RDN/RUP traces.

- 5. Use reference platform layout as a guideline for routing & location of CSI\_DSI\_RDN/RUP resistors.
- 6. Avoid routing signal traces directly below and in parallel with these critical rails.

#### Additional CSI Routing Guidelines

Guideline
If routing to DSI or CSI device includes a flex or 2 <sup>nd</sup> PCB, the max trace & skew calculations must include all the PCBs/flex routing

Keep critical DSI/CSI related traces including DSI/CSI clock/data traces & RDN/RUP traces away from other signal traces or unrelated power traces/areas or power supply components

#### Table 94. MIPI CSI Signal Connections

Ball Name	Туре	Termination	Description
CSI_A_CLK_N/P	I		CSI A Differential Clock: Connect to CLKn & CLKp pins of Camera #1
CSI_A_D[1:0]_N/P CSI_B_D[1:0]_N/P	1/0		CSI A/B Differential Data Lanes: Connect to Dn & Dp pins of Camera #1
CSI_E_CLK_N/P	I		CSI E Differential Clock: Connect to CLKn & CLKp pins of Camera #2.
CSI_E_D_N/P	I/0		CSI E Differential Data Lanes: Connect to Dn & Dp pins of Camera #2
CSI_DSI_RDN	A	49.9Ω to GND	DSI/CSI Voltage Reference Pull-down: Connect through termination to GND
CSI_DSI_RUP	A	$453\Omega$ to +1.2V_GEN_AVDD	DSI/CSI Voltage Reference Pull-up: Connect through termination indicated to same rail as AVDD_CSI_DSI
AVDD_CSI_DSI	Ρ		MIPI DSI & CSI Shared Power Rail: Connect to +1.2V_GEN_AVDD supply

Note: Depending on the mechanical design of the platform and camera modules, ESD protection may be necessary. Any ESD solution must be compatible with the frequency required by the design.

Table 95.	Miscellaneous Camera Connection	าร
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Ball Name	Туре	Termination	Description
CAM_I2C_SCL CAM_I2C_SDA	1/0	Pull-ups to +1.8V_RUN_CAM.	Camera I2C Interface: Connect to I2C SCL & SDA pins of cameras
CAM_MCLK	0		Camera #1 Master Clock: Connect to Camera #1 reference clock input.
GPIO_PBB0	1/0		CAM2_MCLK - Camera #2 Master Clock: Connect to Camera #2 clock input.
GPIO_PBB3			CAM_RST_L - Camera Reset: Connect to Camera reset inputs.
GPIO_PBB4			CAM_FLASH - Camera Flash: Connect to Flash driver enable if supported.
GPIO_PBB5			CAM1_PWND - Camera #1 Powerdown: Connect to Camera #1 powerdown input.
GPIO_PBB6			CAM2_PWND - Camera #1 Powerdown: Connect to Camera #2 powerdown input.
GPIO_PBB7			CAM1_AF_PWND - Camera #1 Autofocus Powerdown: Connect to Camera


Ball Name	Туре	Termination	Description
			#1 Autofocus powerdown input.
GPIO_PCC1			CAM1_GPIO - Camera #1 General Purpose IO: Available GPIO for Camera #1
GPIO_PCC2			CAM1_GPIO - Camera #2 General Purpose IO: Available GPIO for Camera #2

Note: Depending on the mechanical design of the platform and camera modules, ESD protection may be necessary. Any ESD solution must be compatible with the frequency required by the design.

Table 96. CSI Interface Package Delays

Signal Name	Ball #	Pkg Delay (ps)									
CSI_A_CLK_N	AE11	46	CSI_A_D1_N	AE9	61	CSI_B_D1_N	AJ9	66	CSI_E_DO_N	AF9	57
CSI_A_CLK_P	AD11	46	CSI_A_D1_P	AD9	62	CSI_B_D1_P	AH9	67	CSI_E_D0_P	AG9	58
CSI_A_D0_N	AK9	81	CSI_B_D0_N	AK8	78	CSI_E_CLK_N	AJ8	67	CSI_DSI_RDN	AG11	61
CSI_A_D0_P	AL9	81	CSI_B_D0_P	AL8	79	CSI_E_CLK_P	AH8	68	CSI_DSI_RUP	AF11	61

Note: If additional CSI pins are used from the DSI block, the package delays for those can be found at the end of the DSI section.

#### 3.8 SDMMC

Tegra has four SD/MMC controllers. Jetson uses SDMMC3 for an SD Card interface and SDMMC4 to interface to an eMMC device (one of the boot options). SDMMC1 is available to use as SDIO to connect to a WiFi controller. SDMMC2 on the GMI block is available for SDIO use as well.

For the SD card and SDIO interfaces, SDMMC[3:1] support up to UHS-1. For eMMC, SDMMC4 supports up to HS200.

#### 3.8.1 eMMC

Figure 36. Jetson eMMC Device Connections



Note: - An EMI filter on SDMMC4\_CLK or other eMMC signals is not recommended. If EMI is a concern, other solutions (PCB GND layers, external shielding, etc.) are preferred. If EMI devices are used, they must be tuned such that the signals meet the timing & electrical requirements of the eMMC specification. If included, the filter should be near Tegra

- See the "Power Decoupling Guidelines" section for power rail decoupling and filter requirements.



#### SDMMC4 (eMMC) Design Guidelines

Table 97. SDMMC4 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency Standard Mode High Speed Modes 52M DDR 52M HS200	26 (26) 52 (52) 52 (104) 200 (200)	MHz (MB/s)	w/8-bit width See Note 1
Topology	Point to point		
Max Loading	10	pF	
Reference plane	GND or PWR		See Note 2
Breakout Region Impedance	45-50	Ω	±15%
Max PCB breakout delay	30	ps	
Trace Impedance	45-50	Ω	±15%
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 3
Trace spacing Microstrip / Stripline	4x / 2x	dielectric	
Max Trace	730	ps	See Note 4
Max Trace Delay Skew in/between CLK & CMD/DAT	50	ps	See Note 4

# Note: 1. Actual frequencies may be lower due to clock source/divider limitations. Where frequencies cannot be achieved, the next lower divider option will be used. The clock source used for all but HS200 is PLLP at 408MHz.

- 2. If PWR, 0.01uF decoupling cap required for return current
- 3. Up to 4 signal vias can share a single GND return via
- 4. Include Package & PCB routing delays for Max trace delays and max trace delay skew parameters.

#### Table 98. SDMMC4\_COMP\_PU/PD Routing Requirements

Parameter	Requirement	Units	Notes
Reference plane	GND if possible		See Note
Trace Impedance	50	Ω	±15%
Max Trace Delay	240	ps	Include Package & PCB routing delays

Notes: - Keep SDMMC\_COMP\_PU/PD routing away from other traces on same layer or on adjacent layers.

#### Table 99. SDMMC4 (eMMC) Signal Connections

Function Signal Name	Туре	Termination	Description
SDMMC4_CLK	0		eMMC Clock: Connect to CLK pin of device
SDMMC4_CMD	I/0	4.7KΩ pull-up to VDD_1V8	eMMC Command: Connect to CMD pin of device
SDMMC4_DAT[7:0]	I/0	No external pull-ups required	eMMC Data: Connect to Data pins of device
SDMMC4_COMP_PU SDMMC4_COMP_PD	A	49.9Ω, 1% to VDD_1V8 49.9Ω, 1% to GND	SDMMC4 Compensation Pull-up/Pull-down Connect as shown in termination column
eMMC RST			eMMC Reset: Connect PMU system reset output (same as used for Tegra SYS_RST_IN to RST_N line of eMMC device



Table 100	SDMMC4	Interface	Package	Delay	IS
	3DIVIIVIC4	michace	I ackage	Delay	3

Signal Name	Ball #	Pkg Delay (ps)	Signal Name	Ball #	Pkg Delay (ps)	Signal Name	Ball #	Pkg Delay (ps)	Signal Name	Ball #	Pkg Delay (ps)
SDMMC4_CLK	G31	74	SDMMC4_DAT1	F30	71	SDMMC4_DAT4	D31	79	SDMMC4_DAT7	F28	62
SDMMC4_CMD	E31	85	SDMMC4_DAT2	E28	66	SDMMC4_DAT5	E30	79	SDMMC4_COMP_PD	H29	67
SDMMC4_DAT0	F29	63	SDMMC4_DAT3	H31	71	SDMMC4_DAT6	E29	71	SDMMC4_COMP_PU	H30	75

#### 3.8.2 SD Card Connections

The Figure shows a standard Micro SD socket. An SD Card should use SDMMC3 which includes a loopback clock feature to improve read timing. The internal Pull-up resistors on the SDMMC Data/CMD lines are strong (see Tegra K1 Data Sheet for values), so external pull-ups are not required.





- Notes: An EMI filter on SDMMC3\_CLK or other SD signals is not recommended. If EMI is a concern, other solutions (PCB GND layers, external shielding, etc.) are preferred. If EMI devices are used, they must be tuned so the signals meet the timing & electrical requirements of the SD specification for the modes supported. If included, the filter should be near Tegra
  - See the "Power Decoupling Guidelines" section for power rail decoupling and filter requirements.
  - Any supply used to power the SD Card must be current limited if the supply is shorted to GND.

Table 101.	SDMMC[3:1]	Interface Signal	Routina	Requirements

Parameter			Requirement	Units	Notes
Max Frequency	3.3V Signaling 1.8V Signaling	DS HS SDR12 SDR25 SDR50 SDR104 DDR50	25 (12.5) 50 (25) 25 (12.5) 50 (25) 100 (50) 208 (104) 50 (50)	MHz (MB/s)	See Note 1 SDMMC1 & SDMMC3 only SDMMC1 & SDMMC3 only SDMMC1 & SDMMC3 only
Topology			Point to point		
Max Loading			10	pF	
Reference plane			GND or PWR		See Note 2
Breakout Region Impedance			45-50	Ω	±15%



Parameter	Requirement	Units	Notes	
Max PCB breakout delay		30	ps	
Trace Impedance		45-50	Ω	±15%
Via proximity (Signal to reference	< 3.8 (24)	mm (ps)	Up to 4 signal vias can share 1 GND return via	
Trace spacing	Microstrip / Stripline	4x / 2x	dielectric	
Max Trace Delay	SDR12, SDR25, SDR50 SDR104	1100 745	ps	See Note 3 & 4
Max Trace Delay Skew in/betweer (CMD/DAT compared to CLK)	100 20	ps	See Note 3 & 4	
Loopback Clock Routing: LB_OUT to LB_IN = CLK lengt	+/- 150	ps		

Keep SDMMC CLK, CMD, DATA, COMP & Loopback clock traces away from other signal traces or unrelated power traces/areas or power supply components

Note: 1. Actual frequencies may be slightly different due to clock source/divider limitations.

- 2. If **PWR**, 0.01uF decoupling cap required for return current
- 3. Include Package & PCB routing delays for Max trace delays and max trace delay skew parameters.
- 4. If routing to SD/SDIO device/socket includes a flex or 2<sup>nd</sup> PCB, the max trace & skew calculations must include all the PCBs/flex routing. Maximum frequencies may not be achievable, even if max trace & skew delays met due to impact on signal guality caused by additional connector & dependent on flex design.

#### Table 102. SDMMC[3:1]\_COMP\_PU/PD Routing Requirements

Parameter	Requirement	Units	Notes
Reference plane	GND		
Trace Impedance	50	Ω	±15%
Max Trace Delay	240	ps	Include Package & PCB delays

Notes: - Keep SDMMCx\_COMP\_PU/PD routing away from other traces on same layer or on adjacent layers.

Function Signal Name	Туре	Termination	Description
SDMMC[3:1]_CLK	0	See note for ESD protection	SDMMC Clock: Connect to CLK pin of device or socket
SDMMC[3:1]_CMD	1/0	No external pull-ups required See note for ESD protection	SDMMC Command: Connect to CMD pin of device or socket
SDMMC[3,1]_DAT[3:0] SDMMC2_DAT[7:0]	1/0	No external pull-ups required. See note for ESD protection	SDMMC Data: Connect to Data pins of device or socket
SDMMC3_CLK_LB_OUT/I N			SDMMC3 Loopback Clock Out/In: Route trace out from SDMMC3_CLK_LB_OUT and back to SDMMC_CLK_LB_IN. Length should match SDMMC3_CLK + Average of SDMMC3_DAT[3:0].
SDMMC[3:1]_COMP_PU SDMMC[3:1]_COMP_PD	A	33.2Ω, 1% to VDDIO_SDMMC3 33.2Ω, 1% to GND	SDMMC Compensation Pull-up/Pull-down: Connect as shown in termination column
SD Card Detect	I	See note for ESD protection	<b>SDMMC Card Detect</b> : Connect <b>GPIO</b> to <b>Card Detect</b> pin on socket. Use Wake-capable pin if wake required on insertion.

#### Table 103. SD/SDIO Signal Connections



Note: -

 $\ensuremath{\mathsf{ESD}}$  protection strongly recommended for  $\ensuremath{\mathsf{SDMMC3}}$  when used as the SD Card socket interface.

- SDMMC3\_COMP\_PU/PD resistors can be 49.9Ω, 1%, if limited to SDR25 (50MHz) operation

Signal Name	Ball #	Pkg Delay (ps)	Signal Name	Ball #	Pkg Delay (ps)	Signal Name	Ball #	Pkg Delay (ps)
SDMMC1_CLK	L7	97	SDMMC3_CLK	F5	63	GPIO_PK1 (SDMMC2_CLK)	R3	63
SDMMC1_CMD	L8	86	SDMMC3_CMD	F2	76	GPIO_PH7 (SDMMC2_CMD)	U2	71
SDMMC1_DAT0	L2	68	SDMMC3_DAT0	H2	74	GPIO_PH4 (SDMMC2_DAT0)	R5	80
SDMMC1_DAT1	L3	68	SDMMC3_DAT1	H1	89	GPIO_PI5 (SDMMC2_DAT1)	U7	52
SDMMC1_DAT2	L1	69	SDMMC3_DAT2	F1	77	GPIO_PH5 (SDMMC2_DAT2)	R4	67
SDMMC1_DAT3	3L	90	SDMMC3_DAT3	G1	72	GPIO_PH6 (SDMMC2_DAT3)	U8	52
SDMMC1_COMP_PD	L6	56	SDMMC3_CLK_LB_IN	F3	72	GPIO_PK3 (SDMMC2_DAT4)	R2	71
SDMMC1_COMP_PU	J7	63	SDMMC3_CLK_LB_OUT	F4	73	GPIO_PK4 (SDMMC2_DAT5)	T1	77
			SDMMC3_COMP_PD	E5	86	GPIO_PI2 (SDMMC2_DAT6)	V1	76
			SDMMC3_COMP_PU	E2	77	GPIO_PI6 (SDMMC2_DAT7)	R1	74
						SDMMC2_COMP_PD	R6	78
						SDMMC2_COMP_PU	U5	54

Table 104. SDMMC[3:1] Interface Package Delays

#### 3.9 Audio

Tegra supports Multiple PCM/I2S audio interfaces & includes a flexible audio-port switching architecture. Jetson uses DAP2 to interface to an audio Codec. The Codec receives a master audio-reference clock from the DAP\_MCLK1 pin on Tegra.







Notes: See the "Power Decoupling Guidelines" section for power rail decoupling and filter requirements.

#### **I2S Design Guidelines**

Table 105. I2S Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Configuration / Device Organization	1	load	
Max Loading	8	pF	
Topology	Point to Point		
Reference plane	GND		
Breakout Region Impedance	Min width/spacing		
Trace Impedance	50	Ω	±20%
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Trace spacing Microstrip / Stripline	2x / 2x	dielectric	
Max Trace Delay	3600 (~22)	ps (in)	See Note 2
Max Trace Delay Skew between SCLK & SDATA_OUT/IN	250 (~1.6")	ps (in)	See Note 2

Note: 1. Up to 4 signal vias can share a single GND return via
 2. Include Package & PCB routing delays for Max trace delays and max trace delay skew parameters.

Table 106.	<b>I2S Signal Connections</b>
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Tegra Ball Name	Function Name	Туре	Termination	Description
DAP[4:1]_SCLK	I2S[3:0]-SCLK	1/0		DAP Serial Clock: Connect to I2S/PCM CLK pin of audio device.
DAP[4:1]_FS	I2S[3:0]-LRCK	1/0		DAP Field Select (Word Select for I2S): Connect to WS (I2S) or FS/SYNC (PCM) pin of audio device.
DAP[4:1]_DOUT	I2S[3:0]-SDATA_OUT	0		DAP Data Output: Connect to Data Input pin of audio device.
DAP[4:1]_DIN	I2S[3:0]-SDATA_IN	I		DAP Data Input: Connect to Data Output pin of audio device.
DAP_MCLK1	EXTPERIPH1_CLK	0		External Peripheral 1 Clock: Connect to MCLK pin of Audio device if reference clock required.

Table 107. DAP[4:1] (I2S[3:0]) Interface Package Delays

Signal Name	Ball #	Pkg Delay (ps)									
DAP1_DIN	H28	66	DAP2_DIN	L30	69	DAP3_DIN	AF17	56	DAP4_DIN	P3	66
DAP1_DOUT	L28	58	DAP2_DOUT	J29	61	DAP3_DOUT	AE17	53	DAP4_DOUT	P5	61
DAP1_FS	J28	59	DAP2_FS	R30	78	DAP3_FS	AE15	55	DAP4_FS	P1	72
DAP1_SCLK	P31	82	DAP2_SCLK	M29	64	DAP3_SCLK	AJ17	66	DAP4_SCLK	N1	71



Tegra has six I2C controllers: PWR\_I2C, I2C1 (GEN1\_I2C), I2C2 (GEN2\_I2C), I2C3 (CAM\_I2C) I2C4 (DDC) & I2C6 (eDP option). The following assignments should be used for the I2C interfaces:

I2C Pins (Function/Controller)	I/O Block	Use
GEN1_I2C (I2C1)	UART	General use (Codec, Sensors, etc.)
GEN2_I2C (I2C2)	GMI	Touch Screen, Battery Pack
CAM_I2C (I2C3)	CAM	Cameras & camera related functions (AF, etc.)
DDC (12C4)	HV	HDMI
PWR_12C (12C5)	SYS	PMU, Ext. CPU Regulator (if required). See PWR_I2C Usage Restrictions section.
I2C6 (on DP_AUX_CH0_P/N pins)	HV	eDP. I2C6 can only operate with VDDIO_HV at 2.8-3.3V

#### I2C Design Guidelines

Care must be taken to ensure I2C peripherals on same I2C bus connected to Tegra do not have duplicate addresses. Addresses can be in two forms: 7-bit, with the Read/Write bit removed or 8-bit including the Read/Write bit. Be sure to compare I2C device addresses using the same form (all 7-bit or all 8-bit format).

- Note: Due to the general purpose design of the I2C drivers the strong drive strengths of the Tegra pads violate the minimum fall time specification for FM mode & minimum rise/fall time specification for HS mode. We do not expect the faster rise/fall times to cause any functional failures for I2C but to be fully compliant with the NXP I2C V.3 specifications, implement the following board level solution:
  - For FM mode: Include a provision to add a shunt capacitor close to the Tegra drivers before the pull-up resistors. Ensure the total minimum capacitance on the SCL/SDA signals is 350pF. The total capacitance includes capacitance of the slave devices, trace capacitance & any required shunt capacitance. Calculate the value of the shunt capacitance accordingly.
  - For HS mode: Include a provision to add an RC circuit close to the Tegra drivers before the pull-up resistors. Ensure the series resistor of the RC circuit has a resistance of 150 Ohms. Ensure the total capacitance on the SCL/SDA signals is 100pF. The total capacitance includes capacitance of the slave devices, trace capacitance & any required shunt capacitance. Calculate the value of the shunt capacitance of the RC circuit accordingly

#### PWR\_I2C Usage Restrictions

The PWR\_I2C interface latencies must be controlled, therefore the following restrictions must be observed:

- Devices do not stretch clock pulses (exception is any stretching performed by the approved PMUs, which have been evaluated & do not risk increasing the latency significantly enough to be a concern).
- Limit the number of devices on the PWR\_I2C bus to lower bus capacitance in order to hit Fast-mode Plus (FM+) speeds (>1Mbps). Only external CPU regulator or possibly Pre-PMU should be on the bus with the PMU.
- All slave devices on the physical PWR\_I2C bus should support Fm+ bus speeds.

#### Table 108. I2C Interface Signal Routing Requirements for Standard, Fast & HS (High-Speed) Modes

Parameter		Requirement Units		Notes		
Max Frequency	Standard / Fast Mode / Fast Mode Plus High-Speed Mode	100 / 400 / 1000 3.4	kHz MHz	See Note 1		
Topology		Single ended, bi-directional, multiple masters/slaves				
Max Loading	Standard / Fast Mode / Fast Mode Plus High-Speed Mode	400 100	pF	Total of all loads		
Reference plane		GND or PWR				



Parameter		Requirement	Units	Notes
Trace Impedance		50 - 60	Ω	±15%
Trace Spacing		1x	dielectric	
Max Trace Delay	Standard Mode Fast Mode, Fast Mode Plus & HS Modes	3400 (~20) 1700 (~10)	ps (in)	Include Package & PCB routing delays

Note: 1. DDC supports only up to Fast Mode Plus speeds

- 2. Avoid routing I2C signals near noisy traces, supplies or components such as a switching power regulator.
- 3. No requirement for decoupling caps for PWR reference

Table 109. I2C Signal Connections

Function Name	Туре	Termination	Description
PWR_I2C_SCL/SDA	OD	Pull-up (see note 1) to 1.8V	Power I2C Clock & Data. Connect to CLK & Data pins of any devices
GEN1_I2C_SCL/SDA	OD	Pull-up (see note 1) to 1.8V or up to 3.3V	Generic I2C 1 Clock & Data. Connect to CLK & Data pins of any devices
GEN2_I2C_SCL/SDA	OD	Pull-up (see note 1) to 1.8V or up to 3.3V	Generic I2C 2 Clock & Data. Connect to CLK & Data pins of any devices
CAM_I2C_SCL/SDA	OD	Pull-up (see note 1) to 1.8V or up to 3.3V	Camera I2C Clock & Data. Connect to CLK & Data pins of any devices
DDC_SCL/SDA	OD	Pull-up (see note 1) to VDDIO_HV level (2.8V-3.3V - See note 2) if level shifters used (5V if direct to HDMI connector)	DDC I2C 2 Clock & Data. Connect to DDC CLK & Data pins of any devices
12C6			I2C 6 interface on DP_AUX_CH0_P/N pins: See eDP connections.

- Note: 1. To determine pull-up resistor values for SCL/SDA for various loading conditions, refer to section 7.1 of the NXP/Philips I2C-bus specification & user manual (Version 3). 1KΩ pull-up resistors recommended for the most common loading conditions for Standard Mode, Fast Mode and Fast Plus Mode and 750Ω pull-up resistors for High Speed mode.
  - 2. If the DDC\_SCL/SDA interface is not used for HDMI DDC, not used, or used as an I2C interface to a device that operates at 1.8V, VDDIO\_HV can operate at 1.8V.
  - 3. GEN[2:1]\_I2C, CAM\_I2C, PWR\_I2C & I2C6 are 3.3V tolerant. If all devices on one of these I2C interfaces require 3.3V levels, the bus can be pulled up to 3.3V instead of the normal 1.8V power rail voltage. DDC is 5V tolerant.
  - 4. If some devices require a different voltage level than others connected to the same I2C bus, level shifters are required.
  - 5. For I2C interfaces that are pulled up to 1.8V, disable the OD (Open Drain) option for these pads. For I2C interfaces that are pulled up to 2.8V or higher, enable the OD (Open Drain) option.

#### De-bounce

The tables below contain the allowable De-bounce settings for the various I2C Modes.

I2C Mode	Clock Source	Source Clock Freq	I2C Source Divisor	SM/FM Divisor	De-bounce Value	I2C SCL Freq
					0	1016KHz
FM+	PLLP_OUT0	408MHz	5 (0x04)	10 (0x9)	5:1	905.8KHz
					7:6	816KHz

#### Table 110. De-bounce Settings (Fast Mode Plus, Fast Mode & Standard Mode)



I2C Mode	Clock Source	Source Clock Freq	I2C Source Divisor	SM/FM Divisor	De-bounce Value	I2C SCL Freq
FM	PLLP_OUT0	408MHz	5 (0x4)	26 (0x19)	7:0	392KHz
SM	PLLP_OUT0	408MHz	20 (0x13)	26 (0x19)	7:0	98KHz

Table 111. Debounce Settings (High-Speed Mode)

Mode	Source	PLLP_OUT0	I2C Source Div	HS Div	De-bounce	I2C Freq
LIC.			3 (0x2)	2 (0×2)	0	3.48MHz
13	PLLP_OUT0	408MHZ		3 (Ux2)	7:1	Not allowed

Table 112. I2C Interface Package Delays

Signal Name	Ball #	Pkg Delay (ps)	Signal Name	Ball #	Pkg Delay (ps)	Signal Name	Ball #	Pkg Delay (ps)	Signal Name	Ball #	Pkg Delay (ps)
CAM_I2C_SCL	AF8	51	GEN1_I2C_SCL	P6	61	GEN2_I2C_SCL	Y2	74	PWR_I2C_SCL	J4	70
CAM_I2C_SDA	AG8	55	GEN1_I2C_SDA	M6	61	GEN2_I2C_SDA	AA2	87	PWR_I2C_SDA	J3	70

#### 3.11 SPI

Tegra has multiple SPI controllers. Jetson uses SPI4 on the GMI block for a SPI ROM (optional boot device) and SPI1 for an interface option to a touchscreen controller. SPI2 is also available for use & is located on the ULPI data lines on the BB block.

Figure 39. Jetson SPI ROM Connections







#### Table 113. SPI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency	50	MHz	
Max Loading (total of all loads)	15	pF	
Reference plane	GND		
Max PCB breakout delay	75	ps	
Trace Impedance	50 - 60	Ω	±15%
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Trace spacing Microstrip / Stripline	4x / 3x	dielectric	
Max Trace Delay	890 (~5)	ps (in)	See Note 2
Max Trace Delay Skew between MOSI (DOUT), MISO (DIN) & CS to SCK	50	ps	

#### Note: 1. Up to 4 signal vias can share a single GND return via

2. Include Package & PCB routing delays for Max trace delays and max trace delay skew parameters.

Table 114.	SPI Signal Connections
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Function Name	Туре	Termination	Description
SPIx-SCK	1/0		SPI Clock.: Connect to Peripheral CLK pin
SPIx-MOSI	1/0		SPI Master Out / Slave In: Connect to Peripheral MOSI pin
SPIx-MISO	1/0		SPI Master In / Slave Out: Connect to Peripheral MISO pin
SPIx-CSx	1/0		SPI Chip Selects.: Connect to Peripheral CS_N pin per

Table 115. SPI Interface Package Delays

Signal Name (SPI1A - Touch, etc.)	Ball #	Pkg Delay (ps)	Signal Name (SPI4 - SPI ROM, etc.)	Ball #	Pkg Delay (ps)
ULPI_NXT (SPI1A_SCK)	AK17	71	GPIO_PG5 (SPI4_SCK)	AA3	66
ULPI_STP (SPI1A_CS0)	AL16	75	GPIO_PI3 (SPI4_CS0)	V7	54
ULPI_CLK (SPI1A_DOUT)	AK17	71	GPIO_PG6 (SPI4_DOUT)	Y8	64
ULPI_DIR (SPI1A_DIN)	AL18	80	GPIO_PG7 (SPI4_DIN)	V3	69

#### 3.12 Thermal Sensor

#### **External Thermal Sensor**

Tegra contains a single, on-die thermal diode that is accessed via an external i2c temperature monitor (TI TMP451). The same temperature monitor IC used for accessing the thermal diode also contains an internal temperature sensor, whose sensed temperature is referred to as Tboard. This temperature is correlated to the internal PCB temperature and not entirely dominated by the Tegra temperature. This board sensor is a required and essential part of the Tskin estimation and governing mechanisms. It is recommended that the external thermal sensor should be located ~15-20mm from Tegra and between the PMIC and CPU.



When the external temperature monitor detects that the TDIODE temperature is above a pre-programmed Tshutdown, the monitor's THERM output signals the PMIC to shut down the system without any software control. This is a back-up mechanism to the internal sensor-based shutdown, so its Tshutdown is intentionally margined to a higher temperature to avoid contention with internal sensor-based shutdown





Table 116.	Thermal Diode /	Temperature Sensor	Interface Signal	Routing Requirements
	mermar broac /	remperator comport	interruce orginar	Routing Requirements

Parameter		Requirement	Units	Notes
Configuration / Device Organization		1	load	
Reference plane		GND		
Breakout Region Impedance		Min width/spacing		
Max PCB breakout delay	100	ps	minimum spacing rules	
Trace Impedance Differential	/ Single-end	90 / Nominal	Ω	±15%
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 1	
Trace spacing Microstri	o / Stripline	4x / 3x	dielectric	See Note 2.
Max Trace Delay		1700 (~10)	ps (in)	See Note 3
Max Trace Intra-pair Skew	5ps	ps	between all discontinuities & overall. See Note 3	

Note: 1. Up to 4 signal vias can share a single GND return via

- 2. Keep switch-mode supply as distant as possible
- 3. Include Package & PCB routing delays for Max trace delays and max trace delay skew parameters.

Table 117.	Thermal Diode Signal Connection	۱S
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Ball Name	Туре	Termination	Description
THERMD_P/N	DIFF IN	1000pF cap between signals & $100\Omega$ Series resistors	Thermal Diode: Connect THERMD_P/N pins to sensor D+/-
GEN1_I2C_SCL GEN1_I2C_SDA	OD I/OD	Pull-up resistor to VDDIO_UART. See I2C section for appropriate values based on frequency & load.	<b>I2C Clock &amp; Data:</b> Connect to I2C interface on Thermal Sensor for configuration and to read temperature data.
ALERT (Sensor)	OD	$10K\Omega$ to GPIO rail (depends on GPIO used - not required in Phone case using GPIO_X6_AUD.	Thermal Alert Notification: Connect to appropriate GPIO on Tegra.
THERM (Sensor)	OD		<b>Critical Thermal Indication</b> : Connect to PMU or other circuitry that will power off device in case of critical Thermal issue.

#### Table 118. Thermal Sensor Interface Package Delays

Signal Name	Ball #	Pkg Delay (ps)	Signal Name	Ball #	Pkg Delay (ps)
THERM_DN	U29	63	THERM_DP	U28	62



#### 3.13 JTAG

JTAG is not required, but may be useful for new design bring-up. Regardless of whether JTAG is implemented, the JTAG\_TCK pull-down resistor shown in the figure is required. Note that JTAG\_TRST\_N is not used as a conventional JTAG reset line. Instead, this pin selects whether JTAG is to be used for communicating with the Tegra CPU complex, or for Test/Scan purposes. When JTAG\_TRST\_N is pulled low, the JTAG interface is enabled for access to the CPU complex. When high, it is in Test/Scan mode. For normal operation, JTAG\_TRST\_N must be pulled low.

#### Figure 42. JTAG Connections



Notes: See the "Power Decoupling Guidelines" section for power rail decoupling and filter requirements.

Table 119.	JTAG Sig	nal Connections
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Ball Name	Туре	Termination	Description
JTAG_TMS	I		JTAG Mode Select: Connect to TMS pin of connector
JTAG_TCK	I	100kΩ to GND	JTAG Clock: Connect to TCK pin of connector
JTAG_TDO	0		JTAG Data Out: Connect to TDO pin of connector
JTAG_TDI	I		JTAG Data In: Connect to TDI pin of connector
JTAG_RTCK	I		JTAG Return Clock: Connect to RTCK pin of connector
JTAG_TRST_N	I	100kΩ to GND	<ul> <li>JTAG Reset (Repurposed to select Normal JTAG or Scan mode):</li> <li>Normal operation: Pulldown only.</li> <li>Scan test mode: Pull strongly (~1kΩ) to +1.8V_VDDIO.</li> </ul>

#### 3.14 **Strapping Pins**

The straps need to be at a valid logic level from the rising edge of SYS\_RESET\_N and must remain valid for at least 12.5us afterwards. During this period, the BootROM reads the values of the strap settings. Straps are re-sampled exiting Deep Sleep. However, the BootROM ignores most straps. GPIO\_PIO is an exception & must be at a valid level (high) when Deep Sleep is exited. An external pull-up is required. Before entering Deep Sleep, ensure this pin has its TRISTATE enable set & internal PD (pull-down) disabled, or programmed it to drive a high level.

Figure 43. Power-on Strapping Connections



Note: -Boot Select can be selected via Fuses instead of straps.

- If boot device is 8-bit eMMC, use setting 1011 for BootModeOFF.
- GPI0\_PI1 (FORCE\_RECOVERY strap) has internal Pull-up (~50KΩ) enabled at boot. Pull-down resistor must be strong enough to overcome the internal resistor. 2.2K $\Omega$  is recommended.
- See the "Power Decoupling Guidelines" section for power rail decoupling and filter requirements.

Strap Options	Strap Pins	Description
USB_RECOVERY	GPIO_PI1	0: USB Recovery Mode 1: Boot from secondary device
Reserved	GPIO_PIO	0: Not Allowed 1: Normal Operation
JTAG_ARM1 JTAG_ARM0	GPIO_PK7, GPIO_PJ7	00: Serial JTAG chain, MPCORE and AVP 01: MPCore only JTAG 10: AVP only JTAG 11: Reserved
RAM_CODE[3:0]	GPIO_PG[7:4]	[3:2] Selects secondary boot device configuration set within the BCT [1:0] Selects DRAM configuration set within the BCT
BOOT_SELECT_CODE[3:0]	GPIO_PG[3:0]	Software reads value and determines Boot device to be configured and used 1000 = SPI Flash 1011 = eMMC x8 BootModeOFF 1111 = Use fuse data Others Reserved
Nvidia Test Mode	TESTMODE_EN	Tie to GND for normal operation

Table 120	Power-on	Stranning	Breakdown
10010 120.		Juapping	Dicakaowii



### 4.0 Pads

### 4.1 Pad Controls

The MPIO pins have output drive & input related controls that are on a Pin Config group basis. The control options available for the Pin Config groups are:

HSM	High Speed Mode (Enable/Disable). For better matching of rise/fall delays in outbound & inbound paths for driver & receiver. May be useful for clocks & high speed signaling where matching timings are critical.
SCHMT	Schmitt Trigger (Enable/Disable): Optional Schmitt Trigger mode for improved noise immunity.
DRVDN / UP	Drive Down / Up: Up to 5 bits (32 settings) of output drive strength control (see note)
DRVDN/UP_SLWR	Drive Down / Up Slew Rate: 4 levels of falling/rising edge (Drive Down/up) signal slew controls

Note: Schmitt Trigger mode should not be enabled for the OD type pads (Used for DDC\_SCL/SDA & HDMI\_INT) as this may result in V<sub>IL</sub>/V<sub>IH</sub> levels not meeting the DC Characteristics specifications in the Data Sheet.
 Not all controls listed in the table are available for all pin groups.

The table below provides estimated output drive values across minimum/maximum DRVUP/DRVDN settings. There are values for 1.8V, 2.8V and 3.3V power rail voltages.

		1.8V		2.8V		3.3V			
	Driv	Drive current (mA)		Drive current (mA)		Drive current (mA)		mA)	
DRVUP DRVDN	Min	Тур	Max	Min	Тур	Мах	Min Typ		Max
00000	7.2	15.5	23.8	11.9	22.2	32.5	16.5	28.3	40.0
11111	14.7	23.4	32.1	28.7	39.8	50.8	36.5	48.3	60.0

 Table 121. Output Drive Current Estimates across Pad Output Control settings



### 5.0 Unused Interface Terminations

### 5.1 Unused Muxed Standard CMOS Pad Interfaces

The following interfaces use the I/O pins that support multiple special functions (SFIO) and GPIO capabilities. Any unused interfaces or portions of these interfaces that are not used can be left unconnected or used for other SFIO functions or as GPIOs. Any of the power rails associated with these interfaces that are not used for any purpose can be left as no connects, or connected to GND.

Function/Interface	Block	Power Rail
SDMMC1	SDMMC1	VDDIO_SDMMC1
SDMMC2	GMI	VDDIO_GMI
SDMMC3	SDMMC3	VDDIO_SDMMC3
SDMMC4	SDMMC4	VDDIO_SDMMC4
I2Sx, Ux3 (UART), SPIx, PWFMx, EXTPERIPHx_CLK, GPIOx	Various	Various
I2Cx, I2CPMU, DDC	Various	Various
SPDIF	HV	VDDIO_HV
DTV	GMI, UART	VDDIO_GMI, VDDIO_UART
PEX_CTL	PEX_CTL	VDDIO_PEX_CTL
SOC_THERM_OC[3:0]_N	GMI, SYS	VDDIO_GMI, VDDIO_SYS
CLDVFS	AUDIO, GMI, SYS	VDDIO_AUDIO, VDDIO_GMI, VDDIO_SYS
USB_VBUS_EN[2:0]	PEX_CTL, HV	VDDIO_PEX_CTL, VDDIO_HV
DP_HPD	HV	VDDIO_HV
VGP[5:3]	САМ	VDDIO_CAM
VIMCLK_x, VIMCLK2_x	САМ	VDDIO_CAM
TRACEx	GMI	VDDIO_GMI
SYS_CLK_REQ	SYS	VDDIO_SYS
SATA_DEV_SLP	AUDIO	VDDIO_AUDIO

### 5.2 Unused Special Function Interfaces

See the Unused Special Function Pins section in the Checklist at the end of this document.



### 6.0 PCB Pad Layout Recommendations

#### Pad Size Recommendations

Recommended pad, etc. sizes for two outer rows of pads (not including 1 pad in each corner See note & associated diagram)

- PAD:
- 0.25mm wide & 0.35mm tall oval
- SOLDERMASK:
   PASTEMASK:
- 0.30mm wide & 0.40mm tall oval 0.25mm wide & 0.35mm tall oval



Note: Oval pads on outer two rows are outlined in dotted lines in figure below. Pad in inner second row corner is not oval.



Recommended Pad, etc. Sizes for All Other Pads

- PAD: 0.30mm round
- SOLDERMASK: 0.35mm round
- PASTEMASK: 0.30mm rount





#### Figure 44. Design Stack-up

			Special Mate	rial requirements	None		
Layer	Material	Thickness (MM)	Line Width (MM)	DIFF Line Spacing (MM)	DIFF Line Centers (MM)	SE Impedance (Ohms)	DIFF Impedance (Ohms)
1 - TOP	Signal 1/2 oz		0.100			50	
			0.101	0.160	0.261	50	90
			0.099	0.350	0.449	50	98
			0.158			40	
			0.131	0.170	0.301	44	80
	Dielectric	0.068					
2 - L2	Plane 1 oz						
	Dielectric	0.076					
3 - L3	Signal 1 oz		0.100	0.475	0.070	50	
			0.101	0.175	0.276	50	90
			0.095	0.350	0.445	50	98
			0.155			40	
			0.155	0.104	0.000	40	00
			0.128	0.194	0.322	44	80
	Dielectric	1.016					
4 -   4	Signal 1 oz	1.010	0 100			50	
	olgrid. For	F	0.101	0.175	0.276	50	90
		F	0.095	0.350	0.445	50	98
		1					
		Г	0.155			40	
			0.128	0.194	0.322	44	80
	Dielectric	0.076					
5 - L5	Plane 1 oz						
	Dielectric	0.068					
6 - BOTTOM	Signal 1/2 oz		0.100			50	
		L	0.101	0.160	0.261	50	90
			0.099	0.350	0.449	50	98
		L L L					
		Ļ	0.158			40	
			0.131	0.170	0.301	44	80

Desired overall thickness with Soldermask

1.564 MM

6

# of Layers

Notes: - Impedance tolerances are +/- 15% unless otherwise specified.

- Not all line widths listed may be present on a particular layer.

- Overall board thickness is +/- 10%.
- Individual layer thickness is +/- 10%.
- Dielectric means PrePreg, Core, or Core/PrePreg.
- If unspecified, then preferred copper fill is 1/2 oz copper for signal layers and 1 oz copper for planes.
- See FAB Drawing for additional information.



### 6.2 Breakout Examples

Several of the main, critical power rails are highlighted as follows:

- VDD\_CPU (Red)
- VDD\_GPU (Yell
- VDD\_CORE (Orange)
- VDDIO\_DDR/DRAM IO Rail (Violet)
- GND (Green)





Figure 46. Layer 2 Breakout





Figure 47. Layer 3 Breakout



Figure 48. Layer 4 Breakout



Figure 49. Layer 5 Breakout



Figure 50. Bottom Layer Breakout





## 7.0 Design Guideline Glossary

The Design Guidelines include various terms. The descriptions and diagrams in the table below are intended to show what these terms mean and how they should be applied to a design.







Pair to pair spacing - Spacing between differential traces	Signal Layer Ground Reference Layer
<ul> <li>Breakout spacing</li> <li>Possible exception to board trace spacing above is shown in figure to right where different spacing rules are allowed under Tegra in order to escape from Ball array.</li> <li>This includes spacing between adjacent traces &amp; between traces/vias or pads under the device in order to escape ball matrix. Outside device boundary, normal spacing rules apply.</li> </ul>	<ul> <li>Min Breakout Spacing</li> <li>Min Breakout Spacing</li> <li>Min Breakout Spacing</li> </ul>
Reference Return	
<ul> <li>Ground Reference Return Via &amp; Via proximity (signal to reference)</li> <li>Signals changing layers &amp; reference GND planes need similar return current path</li> <li>Accomplished by adding via, tying both GND layers together</li> <li>Via proximity (sig to ref) is distance between signal &amp; reference return vias</li> </ul>	Layer 1 (SIG)
<ul> <li>GND reference via for Differential Pair</li> <li>Where a differential pair changes GND reference layers, return via should be placed close to &amp; between signal vias (example to right)</li> <li>Signal to return via ratio</li> <li>Number of Ground Return vias per Signal vias</li> <li>For critical interfaces, ratio is usually 1:1</li> <li>For less critical interfaces, several trace vias can share fewer return vias (i.e. 3:2 - 3 trace vias &amp; 2 return vias).</li> </ul>	GND Reference Via
<ul> <li>Slots in Ground Reference Layer</li> <li>When traces cross slots in adjacent power or ground plane</li> <li>Return current has longer path around slot</li> <li>Longer slots result in larger loop areas</li> <li>Avoid slots in GND planes or do not route across them</li> </ul>	Avoid Slots/Voids in GND Refrence Layers Trace Over/Under GND Refrence GND Reference
<ul> <li>Routing over Split Power Layer Reference Layers</li> <li>When traces cross different power areas on power plane</li> <li>Return current must find longer path - usually a distant bypass cap</li> <li>If possible, route traces w/solid plane (GND or PWR) or keep routes across single area</li> <li>If traces must cross two or more power areas, use stitching capacitors</li> <li>Placing one cap across two PWR areas near where traces cross area boundaries provides high-frequency path for return current</li> <li>Cap value typically 0.1uF &amp; should ideally be within 0.1" of crossing</li> </ul>	PWR Area 1 Place 0.1uf Stitching Cap Across Gap Trace Crossing Over or Under Two PWR Refrence Areas PWR Area 2



## 8.0 Design Checklist

The checklist below is intended to help ensure that the correct connections have been made in a design. The check items describe connections for the various interfaces and the "Same/Diff/NA" column is intended to be used to indicate whether the design matches the check item description, is different, or is not applicable to the design.

Table	123.	Checklist

Check Item Description	Same/Diff/NA
Clocking	
XTAL_IN/ XTAL_OUT connect to terminals of external 12MHz crystal	
XTAL_IN & XTAL_OUT have 12pF Load caps to GND	
AVDD_OSC connects to 1.8V	
CLK_32K_IN connected to PMU 32kHz output clock	
Power	
Control	
PWR_I2C_SCL/SDA connect to PMU with 1Kohm pull-up resistors to +1.8V_VDDIO	
PWR_INT_N connects to Interrupt pin on PMU.	
CORE_PWR_REQ connects to CORE_PWRREQ of PMU	
CPU_PWR_REQ connects to CPU_PWRREQ of PMU	
VDD_CPU_SENSE connects to FB_SD0_P pin of PMU	
GND_CPU_SENSE connects to FB_SD0_N pin of PMU	
VDD_CORE_SENSE connects to FB_SD1_P pin of PMU	
GND_CORE_SENSE connects to FB_SD1_N pin of PMU	
VDD_GPU_SENSE connects to FB_SD6_P pin of PMU	
GND_GPU_SENSE connects to FB_SD6_N pin of PMU	
Power Tree (Matches Jetson TK1 board)	
TPS51220 3.3V SW used for +3.3V_SYS	
TPS51220 5.0V SW used for +5V_SYS	
SD0 (+AS3728 Power Stage) used for +VDD_CPU	
SD1 (+AS3728 Power Stage) used for +VDD_CORE	
SD6 (+AS3728 Power Stage) used for +VDD_GPU	
PMU LX_SD[3:2] used for +1.35V_LP0	
PMU LX_SD4 used for +1.05V_RUN	
PMU LX_SD5 used for +1.8V_VDDIO	
PMU LDO0 used for +1.05V_RUN_AVDD	
PMU LDO1 used for +1.8V_RUN_CAM	
PMU LDO2 used for +1.2V_GEN_AVDD	
PMU LDO3 used for +1.05V_LP0_VDD_RTC	



Check Item Description	Same/Diff/NA				
PMU LDO4 used for +2.8V_RUN_CAM					
PMU LD05 used for +1.2V_RUN_CAM_FRONT					
PMU LDO6 used for +VDDIO_SDMMC3					
PMU LDO7 used for +1.05V_RUN_CAM_REAR					
PMU LDO9 used for +3.3V_RUN_TOUCH					
PMU LDO10 used for +2.8V_RUN_CAM_AF					
PMU LDO11 used for +1.8V_RUN_VPP_FUSE					
Supply Connections					
Pre-PMU PMU Switcher connections match reference design					
PMU + Power Stage (CPU/CORE/GPU) connections match reference desig	ın				
PMU DC/DCs connections match reference design					
PMU LDOs connections match reference design					
PMU Power Control/GPIOs connections match reference design					
External Supply connections match reference design					
Critical Power Components					
VDD_CPU inductors & output caps matches or exceeds specs of device in Supply Considerations.	2.2 CPU	I, gpu, c	ORE & DD	R	
VDD_GPU inductors & output caps matches or exceeds specs of device in Supply Considerations.	DR				
VDD_CORE Inductor & output caps matches or exceeds specs of device in Supply Considerations.	n 2.2 CPL	J, GPU, C	ore & De	DR	
Peripheral Power					
Any additional peripheral devices have dedicated supply or load switch t used	o allow i	t to be sh	ut off wh	ien not	
Power/Voltage Monitoring					
SOC Therm connections match reference design					
Power monitor implemented if 5V or Single-cell design. Device/connect (shown in section 2.6.1)					
Voltage monitor implemented if 5V or Single-cell design. Device/connect (shown in section 2.6.2)					
Power Decoupling/Filtering	4.7uF (0201- 0402)				
Decoupling for VDD_CORE is	3	0	0	7	
Decoupling for VDD_CPU is	Decoupling for VDD_CPU is 4 0 0 8				
Decoupling for VDD_GPU is 3 0 0 6					
Decoupling for VDD_RTC is 1 0 0					
Decoupling for AVDD_OSC is	0	0	0	1	
AVDD_OSC has power filter (Ferrite Bead - 30Ω @100MHz )					



Check Item Description					Same/Diff/NA
Decoupling for VDDIO_DDR_MCLK/VDDIO_DDR together is	2	0	0	5	
Decoupling for VDDIO_DDR_HS & AVDD_PLL_APC2C3) is	1	0	1	0	
Decoupling for AVDD_PLL_M is	1	0	1	0	
Decoupling for AVDD_PLL_CG & AVDD_PLL_X together is	1	0	1	0	
Decoupling for AVDD_PLL_C4 is	1	0	1	0	
Decoupling for AVDD_PLL_UD2DPD is	1	0	1	0	
Decoupling for AVDD_PLL_EREFE is	1	0	1	0	
Decoupling for VDDIO_HV & AVDD_HDMI together is	1	0	0	1	
Decoupling for AVDD_HDMI_PLL is	1	0	1	0	
Decoupling for AVDD_CSI_DSI is	1	0	0	1	
Decoupling for AVDD_USB is	1	0	0	1	
Decoupling for AVDD_PLL_UTMIP is	1	0	0	1	
AVDD_PLL_UTMIP has filter (Ferrite Bead - 30Ω@100MHz)					
Decoupling for HVDD_PEX_PLL_E & HVDD_PEX together is	1	0	0	1	
Decoupling for AVDDIO_PEX, DVDDIO_PEX & AVDD_PEX_PLL together is	1	1	0	1	
AVDD_PEX_PLL has filter (Ferrite Bead - 30Ω@100MHz)					
Decoupling for VDDIO_SATA & AVDD_SATA_PLL together is	1	1	0	1	
Decoupling for AVDD_SATA_PLL has filter (Ferrite Bead - 30Ω@100MHz)					
Decoupling for HVDD_SATA & VDDIO_PEX_CTL together is	1	0	0	1	
Decoupling for VDDIO_PEX_CTL is	1	0	0	1	
Decoupling for AVDD_LVDS0_IO is	1	0	1	0	
Decoupling for AVDD_LVDS0_PLL is	1	0	0	1	
AVDD_LVDS_PLL has filter (Ferrite Bead - 30Ω@100MHz)					
Decoupling for VDDIO_HSIC is	1	0	0	1	
Decoupling for VDDIO_SYS i	1	0	0	1	
Decoupling for VDDIO_SYS2 is	1	0	0	1	
Decoupling for VDDIO_BB is	1	0	0	1	
Decoupling for VDDIO_UART & VDDIO_GMI together is	1	0	0	1	
Decoupling for VDDIO_SDMMC1 is	1	0	0	1	
Decoupling for VDDIO_SDMMC3 is	1	0	0	1	
Decoupling for VDDIO_SDMMC4 is	1	0	0	1	
Decoupling for VDDIO_AUDIO is	1	0	0	1	
Decoupling for VDDIO_CAM is	1	0	0	1	
Decoupling for VPP_FUSE is	1	0	0	0	



Check Item Description	Same/Diff/NA
DRAM	
Common (DDR3L or LPDDR3)	
Pin re-mapping matches configuration table in section 3.3.1 (DDR3L) or 3.3.2 (LPDDR3) exactly.	
DDR_DQ[63:0] nets connect to same DQ pins of all DRAMs corresponding to the appropriate byte lane (groupings).	
DDR_DM[7:0] nets connect to same DM pins of all DRAMs corresponding to the appropriate byte lane (groupings).	
DDR_DQS[7:0]P/N nets connect to same DQS/DQS# pins of all DRAMs matching the appropriate byte lane (groupings).	
DDR0_CLKP/N connect to CK/CK# pins of all DRAMs used in the lower 32-bits	
DDR1_CLKP/N connect to CK/CK# pins of all DRAMs used in the upper 32-bits	
DDR0_CS[1:0]_N, DDR0_CKE[1:0] & DDR0_ODT[1:0] nets connect to matching CS/CKE/ODT pins of all DRAM used in the lower 32-bits	
DDR1_CS[1:0]_N, DDR1_CKE[1:0] & DDR1_ODT[1:0] nets connect to CS/CKE/ODT pins of all DRAM used in the upper 32-bits	
VDDIO_DDR_HS connects to 1.05V supply	
ZQ[1:0] on DRAM device connect to 240 $\Omega$ , 1% pull-downs to GND	
Decoupling on VDD for each DRAM device is 3 0.1uF & 1 4.7uF capacitors	
Decoupling on VDDQ for each DRAM device is 3 0.1uF & 1 4.7uF capacitors	
DDR3L Specific	
90 $\Omega$ (2, 45.3 $\Omega$ , 1%) between CLK_P & N pins + 0.01uF cap center-tapped to GND. Connected at end of main trunk.	
2.2pf capacitor between CLKP & CLKN close to Tegra pins	
DDR_A[15:6,2:0] nets connect to A[15:6,2:0] pins of all DRAMs.	
DDR0_A[5:3] nets connect to A[5:3] pins of all DRAM used in the lower 32-bits	
DDR1_A[5:3] nets connect to A[5:3] pins of all DRAMs used in the upper 32-bits	
DDR_BA[2:0] nets connect to same BA pins of all DRAMs.	
DDR_CAS_N, DDR_RAS_N, DDR_WE_N nets connect to CAS_N, RAS_N & WE_N pins respectively of all DRAMs.	
DDR_COMP_PU pulled up with 34 $\Omega$ , 1% to 1.35V & DDR_COMP_PD pulled down with 34 $\Omega$ , 1% to GND	
VDDIO_DDR, VDDIO_DDR_MCLK & DRAM VDD/VDDQ connect to 1.35V supply	
VSS, VSSQ on DRAM devices connect to GND	
Decoupling on VDD for each DRAM device is 3 0.1uF & 1 4.7uF capacitors	
Decoupling on VDDQ for each DRAM device is 3 0.1uF & 1 4.7uF capacitors	
LPDDR3 Specific	
DDR0_A[9:0] external signals connect to CA[9:0] pins of all DRAM used in the lower 32-bits.	
DDR1_A[9:0] external signals connect to CA[9:0] pins of all DRAM used in the upper 32-bits.	
DDR_COMP_PU pulled up with 40.2 $\Omega$ , 1% to 1.2V & DDR_COMP_PD pulled down with 40.2 $\Omega$ , 1% to GND	
VDDIO_DDR, VDDIO_DDR_MCLK & DRAM VDD2/VDDCA/VDDQ connect to 1.2V supply	



Check Item Description	Same/Diff/NA
DRAM VDD1 connects to 1.8V supply	
VSS, VSSQ, VSSCA on DRAM device connect to GND	
Decoupling on VDD1 for each DRAM device is 2 0.1uF & 2 4.7uF capacitors	
Decoupling on VDD2 for each DRAM device is 3 0.1uF & 1 1.0uF capacitors	
Decoupling on VDDCA for each DRAM device is 3 0.1uF & 2 4.7uF capacitors	
Decoupling on VDDQ for each DRAM device is 2 0.1uF capacitors	
USB/PEX/SATA/HSIC	
USB 2.0	
USB0 available to be used as device for USB recovery at a minimum	
GPIO_PI1 can be pulled to GND before SYS_RESET_N rises to enter recovery mode	
USB0_VBUS connected to output of 5V VBUS supply through load switch enabled by AVDD_USB supply.	
USB[2:0]_DP/N connect to USB connector, Mini-Card Socket, Hub, etc. (See Pins_EMI_ESD section for related checks).	
USB ID from conn. is pulled to 5V VBUS supply (100K $\Omega$ ) & connects to PMU PWM_CLK2 pin through FETs (matches reference design).	
USB_REXT connect through 1kΩ, 1% resistor to GND	
AVDD_USB connects to 3.3V Supply	
If USB Wake (using USB mechanism) required, AVDD_USB is powered in Deep Sleep & not connected to other rails that must be off.	
AVDD_PLL_UTMIP connects to 1.8V Supply	
USB 3.0	
USB3_RX0_P/N & PEX_USB3_RX1_P/N connect to USB 3.0 connectors, etc.	
USB3_TX0_P/N & PEX_USB3_TX1_P/N connects to USB 3.0 connector, etc. through 0.1uF series capacitors.	
PEX_TERMP connect through 2.49k $\Omega$ , 1% resistors to GND	
AVDDIO_PEX, DVDDIO_PEX & AVDD_PEX_PLL (required for USB3 & PEX) connect to 1.05V supply	
HVDD_PEX connects to 3.3V supply	
If USB 3.0 Wake (using USB mech.) is required, HVDD_PEX is powered in Deep Sleep & not connected to other rails that must be off.	
If USB 3.0 Connector used, it must be USB-IF certified	
PCIe	
Single Iane PCIe interfaces are be located at Lane 2 (PEX_TX/TX2N/P - Cont #1) &/or Lane 4 (PEX_TX/TX4N/P - Cont #0)	
Dual Lane PCIe interface are be located at Lanes [4:3] (PEX_TX/TX[4:3]N/P - Cont #0)	
Quad Lane PCIe interface are be located at Lanes [4:1] (PEX_TX/TX[4:1]N/P - Cont #0)	
PCIe controller #0 is associated with PEX_CLK1P/N, PEX_L0_CLKREQ_N & PEX_L0_RST_N	
PCIe controller #1 is associated with PEX_CLK2P/N, PEX_L1_CLKREQ_N & PEX_L1_RST_N	
PCIe TX Ianes (PEX_USB3_TX0P/N, PEX_TX[4:2]P/N) connect to TX_P pins of PCIe device/connector through 0.1uF caps	



Check Item Description	Same/Diff/NA
Connector case: PCIe RX lanes (PEX_USB3_RX0P/N, PEX_RX[4:2]P/N) connect to RX_P pins of PCIe connector	
Direct Device case: PCIe RX lanes (PEX_USB3_RX0P/N, PEX_RX[4:2]P/N) connect to RX_P pins of PCIe device through 0.1uF caps	
PEX_L[1:0]_CLKREQ_N connects to CLKREQ pins on device/connector(s)	
PEX_L[1:0]_RST_N connect to PERST pins on device/connector(s)	
PEX_WAKE_N connects to WAKE pins on device or connector w/100KΩ pullup to +3.3V_LP0 supply	
PEX_TERMP connects to GND through 2.49K $\Omega$ , 1% termination resistor to GND	
PEX_REFCLKP/N are Unused & connected to GND	
PEX_TSTCLKP/N are unused & left NC	
DVDDIO_PEX, AVDDIO_PEX & AVDD_PEX_PLL connect to +1.05V_RUN supply	
HVDD_PEX & HVDD_PEX_PLL_E & VDDIO_PEX_CTL Connect to +3.3V_LP0 supply	
SATA	
SATA_L0_TXP/N connect to TX_P pins of SATA device/connector through 0.1uF caps	
Connector case: SATA_L0_RXP/N pins connect to RX_P pins of SATA connector	
Direct Device case: SATA_L0_RXP/N pins connect to RX_P/N pins of SATA device through 0.1uF caps	
SATA_TERMP connects to GND through 2.49K $\Omega$ , 1% termination resistor to GND	
SATA_TSTCLKP/N are unused & left NC	
VDDIO_SATA & AVDD_SATA_PLL connect to +1.05V_RUN supply	
HVDD_SATA connects to +3.3V_LP0 supply	
HSIC	
HSIC[2:1]_STROBEs connect to STROBE pin on HSIC device(s).	
HSIC[2:1]_DATA connect to DATA pin on HSIC device(s).	
Series resistor pads placed near Tegra on STROBE/DATA (highly recommended for early designs in case signal tuning required)	
HSIC_REXT connects through 1.0k $\Omega$ , 1% resistor to GND	
VDDIO_HSIC connects to 1.2V supply	
SDMMC	
eMMC (SDMMC4)	
SDMMC4_CLK connects to CLK pin of eMMC device (See Pins_EMI_ESD section for related checks).	
SDMMC4_CMD connects to CMD pin of eMMC device. External 4.7KΩ pull-up resistor to the 1.8V rail used for VDDIO_SDMMC4.	
SDMMC4_DAT[7:0] connect to DAT pins of eMMC device. No external pull-ups required.	
SDMMC4_COMP_PU connect to 49.9Ω, 1% to 1.8V (same supply as VDDIO_SDMMC4)	
SDMMC4_COMP_PD connects to 49.9Ω, 1% to GND	
PMU Reset output connected to eMMC Reset.	



Check Item Description	Same/Diff/NA
SDMMC1	
SDMMC1_CLK connects to CLK pin of device	
SDMMC1_CMD connects to CMD pin of device. No external pull-ups required.	
SDMMC1_DAT[3:0] connect to DAT pins of device. No external pull-ups required	
SDMMC1_COMP_PU connect to 33.2 $\Omega$ , 1% to same supply as VDDIO_SDMMC1.	
SDMMC1_COMP_PD connects to 33.2Ω, 1% to GND	
SDMMC2	
SDMMC2_CLK connect to CLK pin of device (See Pins_EMI_ESD section for related checks).	
SDMMC2_CMD connect to CMD pin of device. External Pull-ups as required by peripheral.	
SDMMC2_DAT[7:0] connect to DAT pins of device. External Pull-ups as required by peripheral.	
SDMMC2_COMP_PU connect to 33.2 $\Omega$ , 1% to 1.8V (same supply as VDDIO_GMI).	
SDMMC2_COMP_PD connects to 33.2Ω, 1% to GND	
SDMMC3	
SDMMC3_CLK connects to CLK pin of socket (See Pins_EMI_ESD section for related checks).	
SDMMC3_CMD connecst to CMD pin of socket. No external pull-ups required.	
SDMMC3_DAT[3:0] connect to DAT pins of socket. No external pull-ups required	
SDMMC3_COMP_PU connect to 33.2 $\Omega$ , 1% to same supply as VDDIO_SDMMC3	
SDMMC3_COMP_PD connects to 33.2Ω, 1% to GND	
SDMMC3 Loopback Clock Out/In is routed as a loop (out from SDMMC3_CLK_LB_OUT & back to SDMMC_CLK_LB_IN)	
SD Card Detect: Connect SDMMC3_CD to CD pin on socket	
SD Card Write Protect (Full-size SD socket): Connect to KB_COL4	
Adequate bypass caps provided on SD Card VDD rail (matches reference design)	
Display	
DSI	
DSI_A_CLK_N/P Clock connects to CLKn & CLKp pins of DSI receiver	
DSI_A_D[3:0]_N/P Data Lanes connects to up to 4 sets of Dn & Dp pins of DSI receiver	
DSI_B_CLK_N/P Clock connects to CLKn & CLKp pins of upper half of 8-lane primary DSI receiver or to 2nd receiver (See Note)	
DSI_B_D[3:0]_N/P Data Lanes connect to upper half of 8-lane primary receiver, or up to 4 lanes of 2nd receiver (See Note)	
CSI_DSI_RDN connects to 49.9Ω, 1% resistor to GND	
CSI_DSI_RUP connects to 453Ω, 1% resistor to AVDD_DSI_CSI (1.2V)	
AVDD_CSI_DSI connects to 1.2V supply	
KB_ROW6 used for TE (Tearing Effect) signal from display if supported	



Check Item Description	Same/Diff/NA
eDP	
LVDS_TXD0_N/P connect to Lane 2 of eDP panel/connector through 0.1uF AC capacitors	
LVDS_TXD1_N/P connect to Lane 1 of eDP panel/connector through 0.1uF AC capacitors	
LVDS_TXD2_N/P connect to Lane 0 of eDP panel/connector through 0.1uF AC capacitors	
LVDS_TXD4_N/P connect to Lane 3 of eDP panel/connector through 0.1uF AC capacitors	
DP_AUX_CH0_N/P connect to Aux Lane of eDP panel/connector through 0.1uF AC capacitors	
100KΩ pull-downs on both DP_AUX_CH0_N/P lines near Tegra.	
100KΩ pull-down on DP_AUX_CH0_P & 100KΩ pull-up on DP_AUX_CH0_N near Connector/Device	
DP_HPD on VDDIO_HV block connects to HPD pin of eDP panel/connector	
LVDS0_RSET connects to 1.0KΩ, 1% resistor to GND	
AVDD_LVDS0_IO connects to 1.05V supply	
AVDD_LVDS0_PLL connects to 3.3V supply	
LVDS	
LVDS0_TXD[2:0]_N/P connect to Lanes [2:0] of LVDS panel/connector	
LVDS0_TXD3_N/P connect to Lane 3 of LVDS panel/connector (if required for 4-lane panel)	
LVDS0_TXD4_N/P connect to Clock Lane of LVDS panel/connector	
KB_ROW6 used for TE (Tearing Effect) signal from display if supported	
LVDS0_RSET connects to 1.0KΩ, 1% resistor to GND	
AVDD_LVDS0_IO connects to 1.05V supply	
AVDD_LVDS0_PLL connects to 1.8V supply	
HDMI	
HDMI_TXCN/P connect to CP-/CP+ pins on HDMI Connector (See Note)	
HDMI_TXD[2:0]N/P connect to D[2:0]-/ D[2:0]+ pins on HDMI Connector	
HDMI_RSET connects to $1k\Omega$ , 1% resistor to GND	
HDMI_INT connects to HP_DET pin on HDMI Connector through 1K $\Omega$ series resistor.	
AVDD_HDMI connects to 3.3V supply with Backdrive circuit	
Ensure supply for AVDD_HDMI can handle up to 100mA (short term spike when display disconnected while Tegra device powered)	
AVDD_HDMI_PLL connects to 1.05V supply	
VDDIO_HV connects to 1.8, 2.8-3.3V supply (2.8-3.3V used if DDC connected to HDMI connector)	
If VDDIO_HV connects to 1.8, the only SFIO function supported is DDC (I2C)	
DDC_SCL/SDA connect to corresponding pins of HDMI Connector through 33Ω series resistors. 1.8K pull-ups to VDD_HDMI 5V supply	
HDMI_CEC connects to CEC on connector through gating circuitry	



Check Item Description	Same/Diff/NA
Video Input	
Camera (CSI)	
CSI_A_CLK_P/N Clock connects to CLKn & CLKp pins of primary camera	
CSI_A_D[1:0]_P/N & CSI_B_D[1:0]_P/N pins connect to up to 4 lanes of primary camera	
CSI_E_CLK_P/N Clock connects to CLKn & CLKp pins of secondary camera	
CSI_E_D0_P/N pins connect to up to secondary camera	
CAM_MCLK connects to primary camera.	
Small Test Points added to CSI_xxx lines near Tegra. Connections from test points to signal very short.	
CAM_MCLK2 (GPIO_PBB0) connects to secondary camera.	
CAM_I2C_SCL/SDA from Tegra connect to Primary & Secondary cameras	
CAM_I2C_SCL/SDA have 1.8k $\Omega$ pull-ups (or values based on section 7.1 of the NXP/Philips I2C-bus spec. & user manual (Version 3)	
CSI_DSI_RDN, CSI_DSI_RUP & AVDD_CSI_DSI connections can be found in Display - DSI section	
If Tegra GPIO used for flash control, one of the GPIO_PBBx pins are used	
Appropriate power filtering/decoupling provided for camera supplies	
Privacy LED included in design if required by OS/provider & powers on when camera is operating (not controlled by SW).	
Audio	
Codec/DAP/I2S	
Tegra I2C_SCL & SDA connect to Codec SCL & SDA pins & pull-up resistors to voltage level of Tegra block I2C pins reside.	
DAP1 pins used for Primary Modem I/F if required	
DAP2 pins used for Codec	
DAP3 pins used for 2nd I2S I/F on Primary Modem (if required)	
DAP4 pins used for Bluetooth (if required)	
DAP[4:1]_SCLK connects to SCLK pin of audio device. (see Pins_EMI_ESD section for related checks)	
DAP[4:1]_FS connects to WS (I2S) or FS/SYNC (PCM) pin of audio device.	
DAP[4:1]_DOUT connects to Data Input pin of audio device.	
SPDIF	
SPDIF_IN connects to TOSLINK optical or other 1.8V/3.3V compatible source	
SPDIF_OUT connects to RCA or TOSLINK optical Connector	
If RCA connector, series 100nF capacitor, series $265\Omega$ resistor, $220\Omega$ pulldown resistor & 100pF capacitor to GND required in path	



Check Item Description	Same/Diff/NA
I2C/SPI/UART	
I2C	
I2C devices on same I2C IF do not have address conflicts (ensure comparisons are done 7-bit to 7-bit format or 8-bit to 8-bit format)	
Level shifters used when required. I2C are of type DD which do not require level shifters to support up to 3.3V devices.	
Pull-up resistors are provided on all I2C I/F segments, including on either side of any level shifters.	
Pull-up resistor values based on reference design or section 7.1 of the NXP/Philips I2C-bus specification & user manual (Version 3)	
PWR/GEN1/GEN2/CAM_I2C _SCL/SDA connect to SCL/SDA pins of devices.	
I2C pull-ups to same rail as block I2C I/F is on, or to rail up to 3.3V, given all devices on bus segment support the higher voltage.	
DDC_SCL/SDA connect to CLK/Data pins of devices. 1.8K pull-ups to +5V_HDMI.	
If I2C6 function used (eDP panel or other), VDDIO_HV is from 2.8-3.3V.	
SPI	
Tegra K1 SPI Clock (SPIx_SCLK) connects to Peripheral CLK pin	
SPI Master Out / Slave In (SPIx_MOSI) connects to Peripheral MOSI pin	
SPI Master In / Slave Out (SPIx_MISO) connect to Peripheral MISO pin	
SPI Chip Selects (SPIx_CSx) connects to Peripheral CS pin	
UART	
UARTx_TXD connects to Peripheral RXD pin of device	
UARTx_RXD connects to Peripheral TXD pin of device	
UARTx_CTS_N connects to Peripheral RTS_N pin of device	
UARTx_RTS_N connects to Peripheral CTS_N pin of device	
Miscellaneous	
THERMP (Temp Sensor)	
GEN1_I2C_SCL/SDA connect to SCLK/SDATA on Thermal Sensor	
THERMD_P/ N connect to a thermal sensor (NCT72/TMP451). 1000pf cap between signal pair. 100 $\Omega$ series resistors	
THERM from Temp. sensor goes to PMU THERM pin with $100k\Omega$ to +2.5V_AON_RTC.	
ALERT from thermal sensor to Tegra GPIO_PI6 pin with $100k\Omega$ to $+1.8V_VDDIO$ .	
JTAG	
JTAG_TMS connects to TMS pin of connector.	
JTAG_TCK connects to TCK pin of connector. 100kΩ GND	
JTAG_TDO connects to TDO pin of connector.	
JTAG_TDI connects to TDI pin of connector.	
JTAG_RTCK connects to RTCK pin of connector.	



Check Item Description	Same/Diff/NA
For normal operation, JTAG_TRST_N is NC or pulled down (recommend external 100K pull-down)	
For Scan test mode, JTAG_TRST_N pulled high (100k $\Omega$ to VDDIO_SYS) or connect to JTAG connector TRST_N pin.	
Strapping	
USB Recovery Mode: GPIO_PI1 is pulled down to GND through resistor no larger than 2.2K $\Omega$ when system powers on	
Normal operation: GPIO_PI1 is pulled up to VDDIO_GMI (Boot from secondary device) with a $10k\Omega$ to $100k\Omega$ resistor	
GPIO_PG[7:4] straps for RAM Code. 100kΩ or stronger pull-ups (to VDDIO_GMI) or pull-downs (to GND). Fewer straps possible if fewer tables required for DRAM/Boot Device.	
GPIO_PG[3:0] Boot Select straps (if straps used for boot select). 100k $\Omega$ pull-up to VDDIO_GMI or 100k $\Omega$ pull-down to GND.	
For eMMC selection using straps, use setting of 1011 on GPIO_PG[3:0] for eMMC x8 BootModeOFF.	
JTAG Access mode: GPIO_PK7 & GPIO_PJ7 have 100k or stronger resistors to GND even if JTAG not supported.	
GPIO_PI0 is pulled to VDDIO_GMI with a 100k $\Omega$ or stronger resistor	
Any Strapping pins used as GPIOs in design will be in correct strap state when SYS_RESET_N goes high. Additionally, GPIO_PIO will be high during/exiting Deep Sleep.	
Pin Selection	
Pinmux completed including GPIO usage (direction, initial state, Ext. PU/PD resistors, Deep Sleep state).	
SFIO usage matches reference platform where possible.	
Each SFIO function assigned to only one pin, even if function selected in Pinmux registers is not used or pin used as GPIO	
GPIO usage matches reference platform where possible.	
EMI/ESD	
Any ESD protection devices used on USB 3.0, DSI, eDP, LVDS, HDMI TMDS, CSI or SDMMC3 (SD Card) are suitable for highest frequency modes supported (has low capacitive load: <1pf recommended).	
Any EMI control devices used on USB 3.0, DSI, eDP, LVDS, HDMI TMDS, CSI or SDMMC3 (SD Card) are suitable for highest frequency modes supported (has low capacitive load: <1pf recommended).	