PAGE	: TITLE
PAGE 1:	COVER PAGE
PAGE 2:	SYSTEM POWER TREE
PAGE 3:	I2C ADDRESS MAP
PAGE 4:	TK1: CH0 MEMORY I/F
PAGE 5:	TK1: CH1 MEMORY I/F
PAGE 6:	DDR3 X16 PAGE 1
PAGE 7:	DDR3 X16 PAGE 2
PAGE 8:	TK1: SDMMC/ULPI/JTAG/KB
PAGE 9:	TK1: CSI/DSI/HDMI/USB
PAGE 10:	TK1: UART/GMI/DAP/SPI
PAGE 11:	TK1: POWER
PAGE 12:	TK1: GND
PAGE 13:	HDMI TYPE A CONN
PAGE 14:	TK1: SATA, PEX, USB 3.0
PAGE 15:	MINI HALF PCIE
PAGE 16:	PEX OPTIONS AND SATA
PAGE 17:	USB PORTS
PAGE 18:	TEMP SENSOR, SERIAL, ID
PAGE 19:	PEX GIGE LAN/PHY
PAGE 20:	AUDIO CODEC
PAGE 21:	AUDIO CONNECTORS
PAGE 22:	JTAG CONN; I2C TRANSLATER
PAGE 23:	EMMC,SPI ROM
PAGE 24:	SWITCHES & STRAPS
PAGE 25:	SD CONN & FRONT PANEL HDR
PAGE 26:	EXP:TOUCH/DISP & GENERAL
PAGE 27:	DC IN
PAGE 28:	+3.3V VR
PAGE 29:	+5V VR
PAGE 30:	LOAD SWITCHES
PAGE 31:	PMIC: LOGIC AND GPIOS
PAGE 32:	PMIC: CNTL, INT SW, LDOS
PAGE 33:	PMIC: DCDC
PAGE 34:	PMIC: TK1 GPU AND CORE
PAGE 35:	VDD_CPU VR
PAGE 36:	REVTSION HISTORY
PAGE 37:	BASENET REPORT
PAGE 38:	BASENET REPORT
PAGE 39:	BASENET REPORT
PAGE 40:	BASENET REPORT
PAGE 41:	BASENET REPORT
PAGE 42:	BASENET REPORT
PAGE 43:	CREF PART REPORT
PAGE 44:	CREF PART REPORT
PAGE 45:	CREF PART REPORT
PAGE 46:	CREF PART REPORT
PAGE 47:	CREF PART REPORT
PAGE 48:	CREF PART REPORT
PAGE 49:	CREF PART REPORT

TK1 Compact Development Module
602-7R375-0000-D00
SCH REV 4.04
04/07/2015
FAB REV D
BOM REV E

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050

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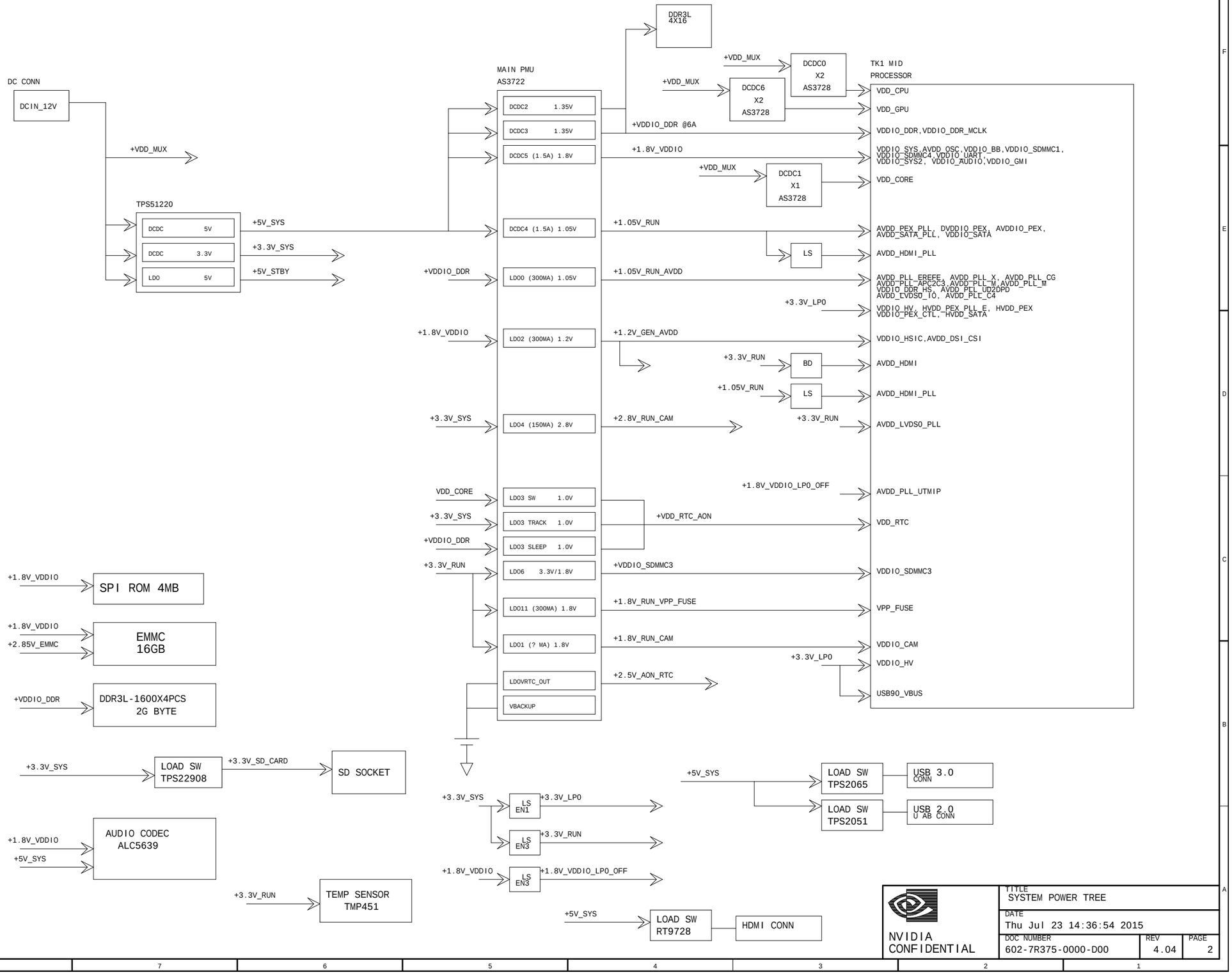
TITLE: COVER PAGE
TK1 Compact Development Module

DATE
Thu Jul 23 14:36:54 2015

DOC NUMBER
602-7R375-0000-D00



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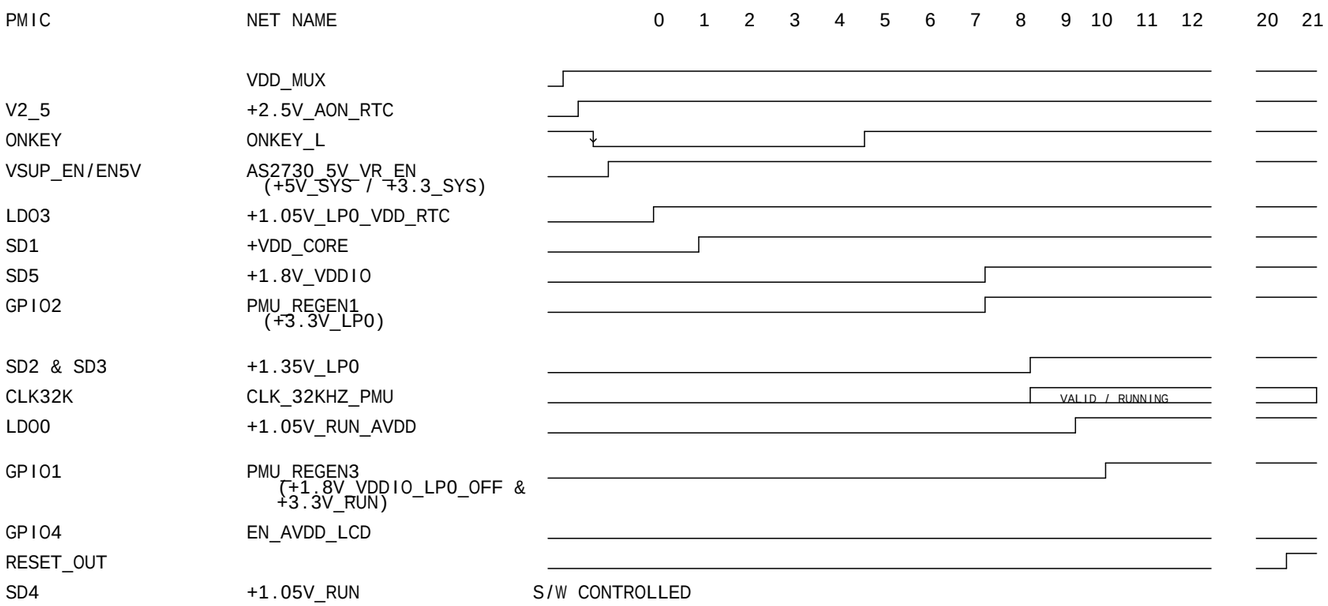
TITLE	SYSTEM POWER TREE
DATE	Thu Jul 23 14:36:54 2015
DOC NUMBER	602-7R375-0000-D00
REV	4.04
PAGE	2

POWER SEQUENCING



I2C ADDRESS MAP

BUS	DEVICE	ADDRESS
GEN1_I2C - 1.8V	AUDIO CODEC	7'H1C, 8'H38
	TEMPERATURE SENSOR	7'H4C, 8'H98
	BOARD ID	7'H56, 8'HAC
	EXPANSION	UNKNOWN
GEN1_I2C - 3.3V	HALF MINI PCIE	UNKNOWN
GEN2_I2C - 3.3V	EXPANSION	UNKNOWN
PWR_I2C - 1.8V	PMIC AS3722	7'H40, 8'H80
	EXPANSION	UNKNOWN
CAM_I2C - 3.3V	EXPANSION	UNKNOWN

Thu Jul 23 14:36:54 2015

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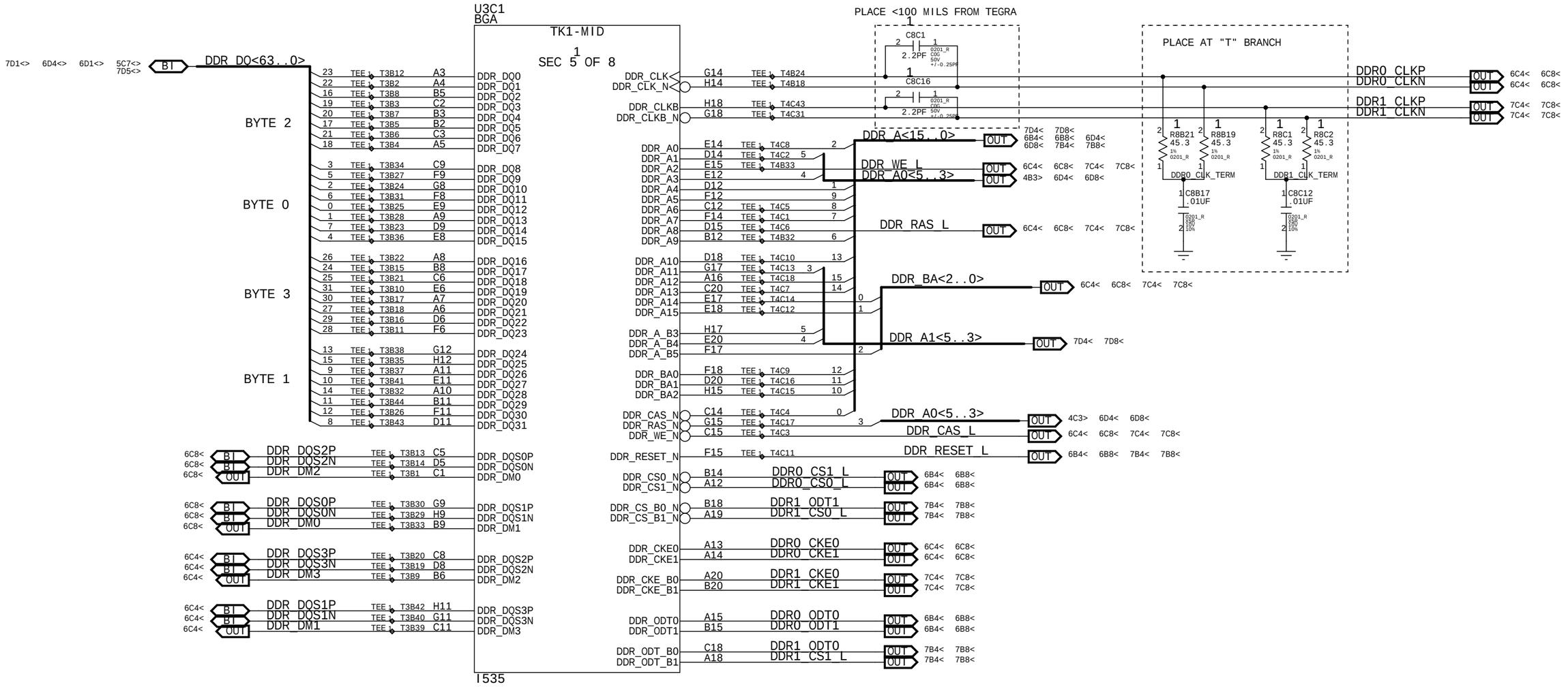
TITLE: I2C ADDRESS MAP

DOC NUMBER: 602-7R375-0000-D00

REV: 4.04

PAGE: 3

DRAM PIN MULTIPLEXING OPTION #14 (DDR3L,4X16, 2 TOP/2 BOTTOM VERTICAL)



TITLE	TK1: CH0 MEMORY I/F
NVIDIA CONFIDENTIAL	
DOC NUMBER	602-7R375-0000-D00
REV	4.04
PAGE	4

Thu Jul 23 14:36:54 2015

DRAM PIN MULTIPLEXING OPTION #14 (DDR3L,4X16, 2 TOP/2 BOTTOM VERTICAL)

U3C1
BGA
TK1-MID
1
SEC 6 OF 8

7D5<> 7D1<> 6D4<> 6D1<> 4D8<> BI DDR_DQ<63..0>

50	TEE	T3C11	G21	DDR_DQ32
51	TEE	T3C8	A21	DDR_DQ33
48	TEE	T3C7	E21	DDR_DQ34
54	TEE	T3C9	F20	DDR_DQ35
52	TEE	T3C2	G20	DDR_DQ36
53	TEE	T3C13	D21	DDR_DQ37
49	TEE	T3C1	B21	DDR_DQ38
55	TEE	T3C12	C21	DDR_DQ39
37	TEE	T3C35	D24	DDR_DQ40
33	TEE	T3C25	C24	DDR_DQ41
38	TEE	T3C36	E27	DDR_DQ42
35	TEE	T3C22	A24	DDR_DQ43
36	TEE	T3C29	E26	DDR_DQ44
32	TEE	T3C26	B26	DDR_DQ45
39	TEE	T3C31	A25	DDR_DQ46
34	TEE	T3C28	A26	DDR_DQ47
62	TEE	T3C20	A22	DDR_DQ48
63	TEE	T3C6	E24	DDR_DQ49
58	TEE	T3C19	A23	DDR_DQ50
60	TEE	T3C3	C23	DDR_DQ51
56	TEE	T3C17	B23	DDR_DQ52
57	TEE	T3C23	G23	DDR_DQ53
61	TEE	T3C14	F24	DDR_DQ54
59	TEE	T3C21	H23	DDR_DQ55
45	TEE	T3C44	D27	DDR_DQ56
44	TEE	T3C34	C29	DDR_DQ57
41	TEE	T3C43	C27	DDR_DQ58
46	TEE	T3C37	A29	DDR_DQ59
40	TEE	T3C38	C31	DDR_DQ60
43	TEE	T3C33	A27	DDR_DQ61
42	TEE	T3C41	C30	DDR_DQ62
47	TEE	T3C39	A28	DDR_DQ63

7C8< BI DDR_DQS6P — TEE T3C5 H21 — DDR_DQS4P
7C8< BI DDR_DQS6N — TEE T3C4 H20 — DDR_DQS4N
7C8< OUT DDR_DM6 — TEE T3C15 F21 — DDR_DM4

7C8< BI DDR_DQS4P — TEE T3C30 C26 — DDR_DQS5P
7C8< BI DDR_DQS4N — TEE T3C27 D26 — DDR_DQS5N
7C8< OUT DDR_DM4 — TEE T3C24 B24 — DDR_DM5

7C4< BI DDR_DQS7P — TEE T3C16 E23 — DDR_DQS6P
7C4< BI DDR_DQS7N — TEE T3C18 D23 — DDR_DQS6N
7C4< OUT DDR_DM7 — TEE T3C10 F23 — DDR_DM6

7C4< BI DDR_DQS5P — TEE T3C42 B30 — DDR_DQS7P
7C4< BI DDR_DQS5N — TEE T3C40 B29 — DDR_DQS7N
7C4< OUT DDR_DM5 — TEE T3C32 B27 — DDR_DM7

32D8< 32B8< 7A8< 6A8< 33B2< 5B3< IN +1.35V_LP0 — R3C2 2 1 34 1% 0201_R — DDR_COMP_PU C17 — DDR_COMP_PU
DDR_COMP_PD D17 — DDR_COMP_PD
R3C1 2 34 1% 0201_R 1

I681

(1.05V)
AVDD_PLL_M K16
AVDD_PLL_APC2C3 B17
VDDIO_DDR_HS A17

(1.35V)
VDDIO_DDR 1 J9
VDDIO_DDR 2 J12
VDDIO_DDR 3 J14
VDDIO_DDR 4 J11
VDDIO_DDR 5 J17
VDDIO_DDR 6 J18
VDDIO_DDR 7 J20
VDDIO_DDR 8 J21
VDDIO_DDR 9 K10
VDDIO_DDR 10 K11
VDDIO_DDR_MCLK J15

+1.05V_RUN_AVDD — TN — 9C2< 9C4< 14C1< 14C7< 32D5>

1 C8C10 0.1UF 0201_R X5R 16V 2 10%
1 C8C11 2.2UF 0402_R X5R 6.3V 2 20%
1 C8C8 0.1UF 0201_R X5R 16V 2 10%
1 C8C7 2.2UF 0402_R X5R 6.3V 2 20%
1 C8C18 0.1UF 0201_R X5R 16V 2 10%
1 C8C20 2.2UF 0402_R X5R 6.3V 2 20%

EMPTY EMPTY EMPTY

1 C8B19 0.1UF 0201_R X5R 16V 2 10%
1 C8C31 0.1UF 0201_R X5R 16V 2 10%
1 C8C28 4.7UF 0402_R X5R 6.3V 2 20%
1 C8C38 4.7UF 0402_R X5R 6.3V 2 20%
1 C8B16 4.7UF 0402_R X5R 6.3V 2 20%
1 C8C36 4.7UF 0402_R X5R 6.3V 2 20%
1 C8B31 4.7UF 0402_R X5R 6.3V 2 20%
1 C8B14 4.7UF 0402_R X5R 6.3V 2 20%
1 C8B21 4.7UF 0402_R X5R 6.3V 2 20%
1 C8B28 4.7UF 0402_R X5R 6.3V 2 20%

ROUTE VDDIO_DDR_MCLK AS 10MIL TRACE W/5X SPACING FROM VREG

+1.35V_LP0_VDDIO_DDR_MCLK_AP

1 C8B30 0.1UF 0201_R X5R 16V 2 10%
PLACE CLOSE TO PIN

1 ISO8C1 10M1L 2

32D8< 6A8< 5A8< 7A8< 32B8< 33B2> IN +1.35V_LP0

Thu Jul 23 14:36:55 2015

NVIDIA CONFIDENTIAL	TITLE: TK1: CH1 MEMORY I/F		
	DOC NUMBER: 602-7R375-0000-D00	REV: 4.04	PAGE: 5

BOTTOM

U7B1
BGA100_2
DDR3_X16
1.35V
1866
256MBIT
HYNIX
1
DDP
FOOTPRINT

CHANNEL 0
RANK 0

TOP

U4B1
BGA100_2
DDR3_X16
1.35V
1866
256MBIT
HYNIX
2
DDP
FOOTPRINT

DDR A<15..0>
DDR A0<5..3>
DDR BA<2..0>
DDR RAS_L
DDR CAS_L
DDR WE_L
DDR0 CLKP
DDR0 CLKN
DDR DQS2P
DDR DQS2N
DDR DQS0P
DDR DQS0N
DDR DM2
DDR DM0
DDR0 CKE0
DDR0 CKE1
DDR0 CS0_L
DDR0 CS1_L
DDR0 ODT0
DDR0 ODT1
DDR RESET_L
VREF_DDR0
DDR ZQ0 U27U1
DDR ZQ1 U27U1
SNN_U27U1_Z3
SNN_U27U1_Z4
SNN_U27U1_Z1
SNN_U27U1_Z2
DDR DQ<63..0>
BYTE 2
BYTE 0
BYTE 3
BYTE 1
DDR DQS3P
DDR DQS3N
DDR DQS1P
DDR DQS1N
DDR DM3
DDR DM1
DDR CKE0
DDR CKE1
DDR CS0_L
DDR CS1_L
DDR ODT0
DDR ODT1
DDR RESET_L
DDR ZQ0 U27U2
DDR ZQ1 U27U2
SNN_U27U2_Z3
SNN_U27U2_Z4
SNN_U27U2_Z1
SNN_U27U2_Z2
R7B2 240
R7B1 240
R4B3 1K
R4B4 1K
R4B2 240
R4B1 240
C7B8 0.1UF
C7B13 0.1UF
C7B4 0.1UF
C7B10 0.1UF
C7B7 4.7UF
C7B5 0.1UF
C7B6 0.1UF
C8B4 4.7UF
C8B6 0.1UF
C7B11 0.1UF
C7B9 0.1UF
C8B5 0.1UF
C4B3 4.7UF
C3B1 0.1UF
C4B1 0.1UF
C7C5 4.7UF
C7C3 0.1UF
C7C6 0.1UF
C4B2 0.1UF
C7B12 0.1UF
+1.35V_LP0
MEM_0A VDDQ
MEM_0A VDD
MEM_0B VDDQ
MEM_0B VDD
A15 USED FOR FUTURE DUAL DIE CONFIG...
I366
I259

Thu Jul 23 14:36:55 2015

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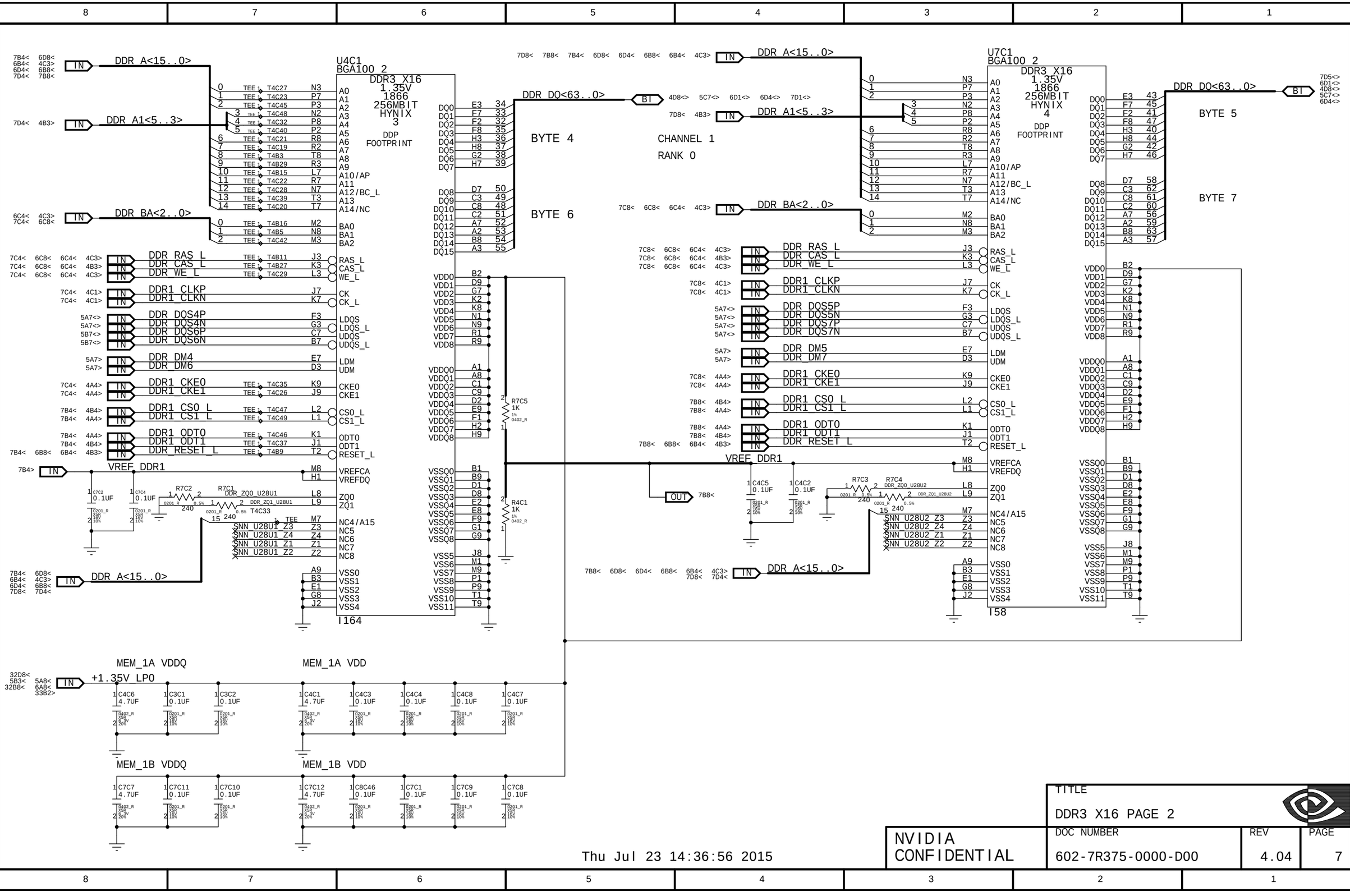
TITLE	DOC NUMBER	REV	PAGE
DDR3 X16 PAGE 1	602-7R375-0000-D00	4.04	6



Thu Jul 23 14:36:56 2015

NVIDIA CONFIDENTIAL	TITLE: DDR3 X16 PAGE 2		
	DOC NUMBER: 602-7R375-0000-D00	REV: 4.04	PAGE: 7

U3C1
BGA

TK1-MID

1

SEC 1 OF 8

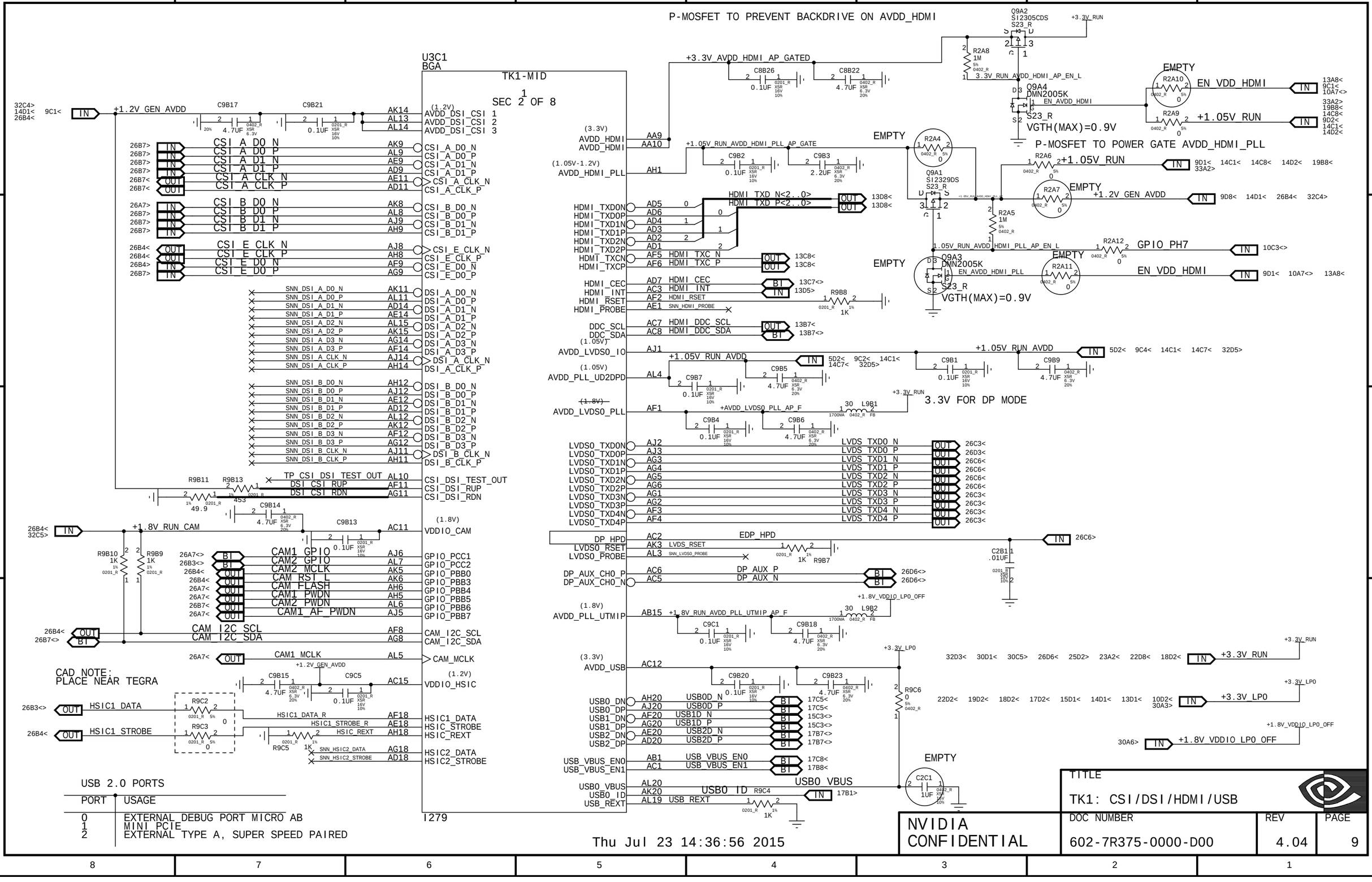
LAYOUT: MATCH SDMMC3_CLK

NOTE: KB_ROW16 IS NOT A TRUE PWM, ONLY ON/OFF

EMPTY

Thu Jul 23 14:36:56 2015

TITLE			
TK1: SDMMC/ULPI/JTAG/KB			
NVIDIA CONFIDENTIAL	DOC NUMBER	REV	PAGE
	602-7R375-0000-D00	4.04	8


P-MOSFET TO PREVENT BACKDRIVE ON AVDD_HDMI
U3C1
BGA
TK1-MID
SEC 2 OF 8
P-MOSFET TO POWER GATE AVDD_HDMI_PLL
CSI A D0 N
CSI A D0 P
CSI A D1 N
CSI A D1 P
CSI A CLK N
CSI A CLK P
CSI B D0 N
CSI B D0 P
CSI B D1 N
CSI B D1 P
CSI E CLK N
CSI E CLK P
CSI E D0 N
CSI E D0 P
CAM1 GPIO
CAM2 GPIO
CAM2 MCLK
CAM RST L
CAM FLASH
CAM1 PWDN
CAM2 PWDN
CAM1 AF PWDN
CAM I2C SCL
CAM I2C SDA
CAM1 MCLK
CAD NOTE:
PLACE NEAR TEGRA
USB 2.0 PORTS
PORT | USAGE
0 EXTERNAL DEBUG PORT MICRO AB
1 MINI PCIE
2 EXTERNAL TYPE A, SUPER SPEED PAIRED
EMPTY
VGTH(MAX)=0.9V
3.3V FOR DP MODE
Thu Jul 23 14:36:56 2015
TITLE
TK1: CSI/DSI/HDMI/USB
NVIDIA CONFIDENTIAL
DOC NUMBER 602-7R375-0000-D00
REV 4.04
PAGE 9

U3C1
BGA
TK1-MID
1
SEC 3 OF 8

(1.8V)
VDDIO_UART U10
C8B23 4.7UF 0402_R X5R 6.3V 20%
C8B18 0.1UF 0201_R X5R 16V 10%

UART2_RXD L9
UART2_TXD M8
UART2_CTS_L M1
UART2_RTS_L P4
26A4> IN UART2_RXD
26A7< OUT UART2_TXD
26A4> IN UART2_CTS_L
26A7< OUT UART2_RTS_L

SNN_UART3_RXD M3
SNN_UART3_TXD M2
SNN_UART3_CTS_L R8
SNN_UART3_RTS_L R9
UART3_RXD
UART3_TXD
UART3_CTS_N
UART3_RTS_N

TP_DAP4_DIN P3
TP_DAP4_DOUT P5
TP_DAP4_FS P1
TP_DAP4_SCLK N1
DAP4_DIN
DAP4_DOUT
DAP4_FS
DAP4_SCLK

26A4< OUT CLK3_OUT P7
SNN_CLK3_REQ M7
R8B12 0 0201_R 5%
CLK3_OUT_R
CLK3_OUT
CLK3_REQ

26B3<> BI GPIO_PU0 R7
26B3<> BI GPIO_PU1 P2
26B3<> BI GPIO_PU2 M10
26A3<> BI GPIO_PU3 P8
26A3<> BI GPIO_PU4 M9
26A3<> BI GPIO_PU5 M4
26A3<> BI GPIO_PU6 M5
GPIO_PU0
GPIO_PU1
GPIO_PU2
GPIO_PU3
GPIO_PU4
GPIO_PU5
GPIO_PU6

+1.8V_VDDIO
R8B10 1K 1% 0201_R
R8B11 1K 1% 0201_R

26A7< 22C4< 20B7< 18D3< 18A6< OUT GEN1_I2C_SCL P6
26D3< GEN1_I2C_SDA M6
22C4<> 20B7<> 18D3<> 18A6<> BI
26D3<> 26A3<>
GEN1_I2C_SCL
GEN1_I2C_SDA

+1.8V_VDDIO
C8C43 4.7UF 0402_R X5R 6.3V 20%
C8C41 0.1UF 0201_R X5R 16V 10%
(1.8V)
VDDIO_AUDIO K31

TP_DAP1_DIN H28
25D7< OUT SATA_LED L28
TP_DAP1_FS J28
TP_DAP1_SCLK P31
DAP1_DIN
DAP1_DOUT
DAP1_FS
DAP1_SCLK

20B7< OUT DAP_MCLK1
R3C6 22 0201_R 5%
DAP_MCLK1_R
DAP_MCLK1 L29
16A5< OUT SATA_PWR_EN_T124 M31
DAP_MCLK1_REQ

20C8< IN DAP2_DIN L30
20C8< OUT DAP2_DOUT J29
20C8<> OUT DAP2_FS R30
DAP2_DIN
DAP2_DOUT
DAP2_FS

20C8<> OUT DAP2_SCLK
R3C4 22 0201_R 5%
DAP2_SCLK_R M29
DAP2_SCLK

13A8< 9D1< 9C1< BI EN_VDD_HDMI AA8
SNN_EN_BAT_SMB AC4
SPDIF_IN
SPDIF_OUT

I208

(2.8V-3.3V)
VDDIO_HV Y10
C9B22 0.1UF 0201_R X5R 16V 10%
C9B24 4.7UF 0402_R X5R 6.3V 20%
+3.3V_LP0

(1.8V)
VDDIO_GMI 1 U9
VDDIO_GMI 2 V10
C8B10 0.1UF 0201_R X5R 16V 10%
C8B12 4.7UF 0402_R X5R 6.3V 20%
+1.8V_VDDIO

18D2< 17D2< 15D1< 30A3< 14D1< 22D2< 13D1< 19D2< 9A2<
32D4< 26A2< 22C7< 25B7< 22B6< 24A2< 21D2< 23A2< 20D2< 22D2< 18D2< 33A2< 8D1<

+3.3V_LP0 IN
+1.8V_VDDIO IN

GPIO_PB0 U4 UART4_RXD IN 18B8> 22D7<
GPIO_PB1 V9 UART4_CTS_L IN 18B8> 22D7<
GPIO_PC7 U1 TP_KBC_IRQ_L
GPIO_PG0 V2 LCD_LR OUT 24D1>
GPIO_PG1 V6 LCD_UD OUT 24D1>
GPIO_PG2 Y7 MODEM_SAR0 BI 24D1>
GPIO_PG3 AA5 GPIO_PG3 BI 24D1>
GPIO_PG4 Y3 SPI4_CS3_L OUT 24B2>
GPIO_PG5 AA3 SPI4_SCK OUT 23A4< 24B2>
GPIO_PG6 Y8 SPI4_MOSI OUT 23A4< 24B2>
GPIO_PG7 V3 SPI4_MISO IN 23A7> 24B2>
STRAPS
GPIO_PH0 Y6 TP_KBL_PWM
GPIO_PH1 U3 LCD_BL_PWM OUT 26C6<
GPIO_PH2 AA4 LCD_BL_EN OUT 26C6<
GPIO_PH3 V8 SNN_GPIO_PH3
GPIO_PH4 R5 CODEC_IRQ_L IN 20B7>
GPIO_PH5 R4 TP_GPIO_PH5
GPIO_PH6 U8 TP_GPIO_PH6
GPIO_PH7 U2 GPIO_PH7 BI 9C1<
GPIO_PI0 Y5 GPIO_PI0 OUT 24C5>
GPIO_PI1 AA6 AP_FORCE_RECOVERY_L IN 24D5>
GPIO_PI2 V1 TP_GPIO_PI2
GPIO_PI3 V7 SPI4_CS0_L OUT 23B7<
GPIO_PI4 Y9 SNN_GPIO_PI4
GPIO_PI5 U7 SNN_GPIO_PI5
GPIO_PI6 R1 TEMP_ALERT_L IN 18A3>
GPIO_PI7 Y4 SNN_GPIO_PI7
GPIO_PJ0 U6 AC_OK_AP_L
GPIO_PJ2 W1 SNN_PG_OC_L
GPIO_PJ7 V4 UART4_TXD OUT 18C7< 22D7>
GPIO_PK0 AA1 TP_GPIO_PK0
GPIO_PK1 R3 TS_SHDN_L OUT 26D3<
GPIO_PK2 Y1 GPIO_PK2 OUT 26D3<
GPIO_PK3 R2 TP_GPIO_PK3
GPIO_PK4 T1 TS_RESET_L OUT 26D3<
GPIO_PK7 V5 UART4_RTS_L OUT 18C7< 24D5>

R3B3 10K 0402_R 1%
+3.3V_LP0
+1.8V_VDDIO
24C5> 22D7>

R2B6 1K 1% 0201_R
R2B8 1K 1% 0201_R
R9B4 1K 1% 0201_R
R9B6 1K 1% 0201_R

GEN2_I2C_SCL Y2 GEN2_I2C_SCL_3.3V
GEN2_I2C_SDA AA2 GEN2_I2C_SDA_3.3V
OUT 26D6<
BI 26D6<>

EMPTY EMPTY EMPTY

SDMMC2_COMP_PU U5 SDMMC2_COMP_PU
SDMMC2_COMP_PD R6 SDMMC2_COMP_PD
EMPTY R8B17 49.9 0201_R 1%
R8B16 49.9 0201_R 1%
+1.8V_VDDIO

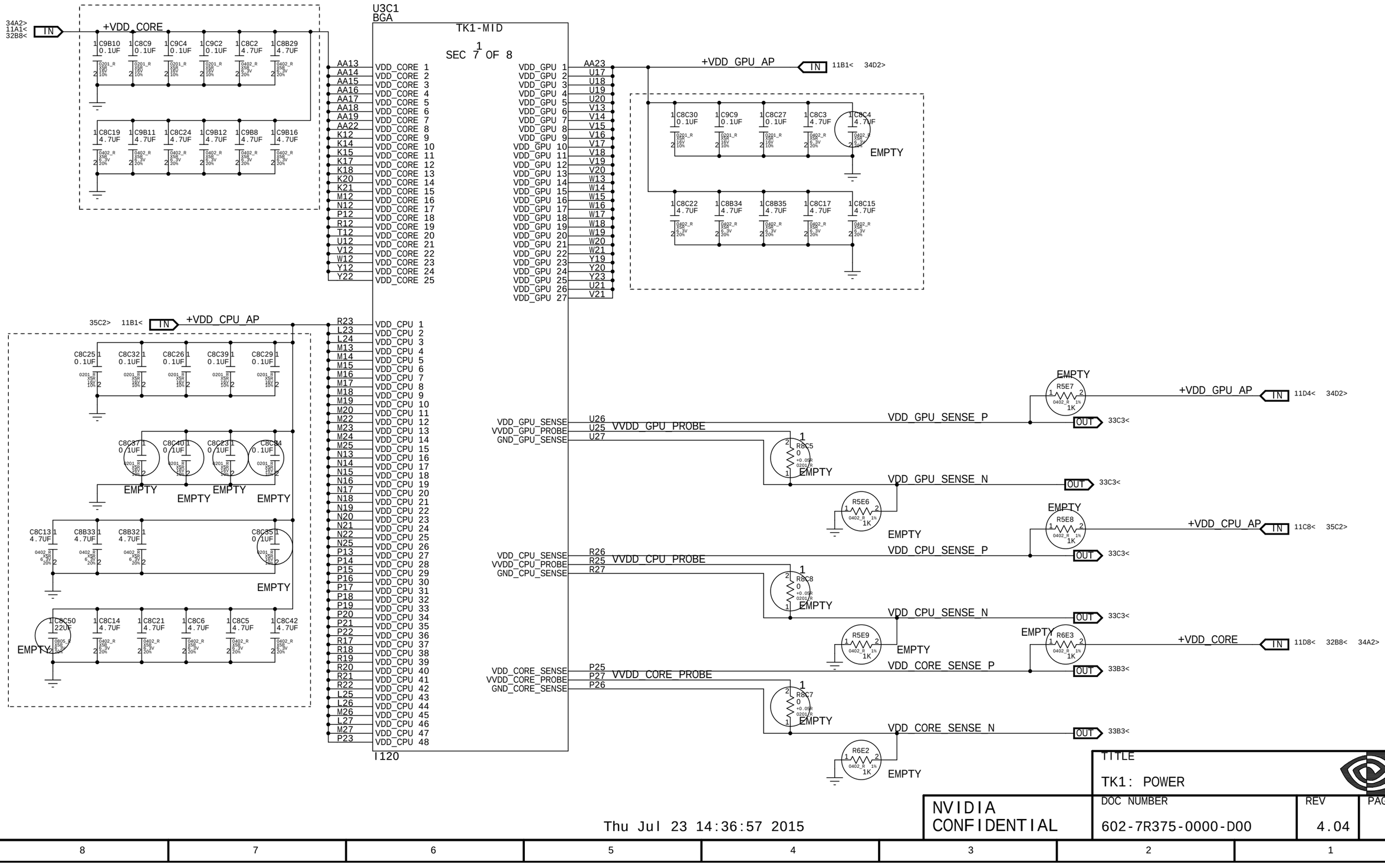
GPIO_X1_AUD P29 BD_ID_STRAP2 IN 24A3>
GPIO_X3_AUD M30 TP_ALS_IRQ_L
GPIO_X4_AUD R28 BD_ID_STRAP3 IN 24A3>
GPIO_X5_AUD R31 SNN_GPS_IRQ_L
GPIO_X6_AUD N31 SNN_COMPASS_DRDY
GPIO_X7_AUD P28 WF_EN
GPIO_W2_AUD M28 SNN_NFC_IRQ_L OUT 15C1<
GPIO_W3_AUD J30 TP_TOUCH_IRQ_L

DVFS_PWM P30 DVFS_PWM BI 33C7<
DVFS_CLK R29 DVFS_CLK OUT 33C7<

SET E_OD PAD = 1 WHEN PU VALUE DIFFERS FROM VDD SOURCE FOR GEN2 I2C

Thu Jul 23 14:36:57 2015

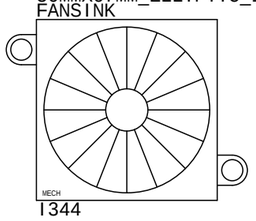
NVIDIA CONFIDENTIAL	TITLE: TK1: UART/GMI/DAP/SPI		
	DOC NUMBER: 602-7R375-0000-D00	REV: 4.04	PAGE: 10



Thu Jul 23 14:36:57 2015

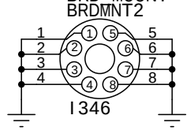
TITLE			
TK1: POWER			
NVIDIA CONFIDENTIAL	DOC NUMBER	REV	PAGE
	602-7R375-0000-D00	4.04	11

HS3C1
HEATSINK
50MMX67MM_ELLIPTIC_12V
FANSINK



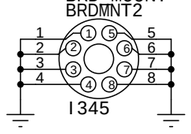
I344

M1A1
BRD_MOUNT
BRDMNT2



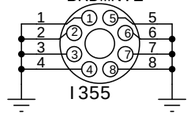
I346

M5E1
BRD_MOUNT
BRDMNT2



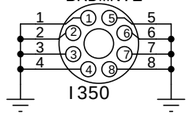
I345

M1E1
BRD_MOUNT
BRDMNT2



I355

M5A1
BRD_MOUNT
BRDMNT2



I350

U3C1
BGA
TK1-MID
1
SEC 8 OF 8

A2	GND 1	GND 21	AE16
AB21	GND 10	GND 22	AE19
L16	GND 100	GND 23	AE22
L17	GND 101	GND 24	AE28
L18	GND 102	GND 25	AE30
L19	GND 103	GND 26	AH2
N2	GND 104	GND 27	AH4
N4	GND 105	GND 28	AH7
N7	GND 106	GND 29	AH10
N10	GND 107	GND 3	AB2
N11	GND 108	GND 30	AH13
N28	GND 109	GND 31	AH16
AB25	GND 11	GND 32	AH19
N30	GND 110	GND 33	AH22
P11	GND 111	GND 34	AH25
R11	GND 112	GND 35	AH28
R13	GND 113	GND 36	AH30
R14	GND 114	GND 37	AK1
R15	GND 115	GND 38	AK4
R16	GND 116	GND 39	AK7
T2	GND 117	GND 4	AB4
T4	GND 118	GND 40	AK10
T7	GND 119	GND 41	AK13
AB28	GND 12	GND 42	AK16
T10	GND 120	GND 43	AK19
T11	GND 121	GND 44	AK22
T13	GND 122	GND 45	AK25
T14	GND 123	GND 46	AK28
T15	GND 124	GND 47	AK31
T16	GND 125	GND 48	AL2
T17	GND 126	GND 49	AL30
T18	GND 127	GND 5	AB7
T19	GND 128	GND 50	B1
T20	GND 129	GND 51	B4
AB30	GND 13	GND 52	B7
T21	GND 130	GND 53	B10
T22	GND 131	GND 54	B13
T25	GND 132	GND 55	B16
T28	GND 133	GND 56	B19
T30	GND 134	GND 57	B22
U11	GND 135	GND 58	B25
U13	GND 136	GND 59	B28
U14	GND 137	GND 6	AB10
U15	GND 138	GND 60	B31
U16	GND 139	GND 61	D2
AC9	GND 14	GND 62	D4
U22	GND 140	GND 63	D7
V11	GND 141	GND 64	D10
V22	GND 142	GND 65	D13
W2	GND 143	GND 66	D16
W4	GND 144	GND 67	D19
W7	GND 145	GND 68	D22
W10	GND 146	GND 69	D25
W11	GND 147	GND 7	AB13
W22	GND 148	GND 70	D28
W25	GND 149	GND 71	D30
AD8	GND 15	GND 72	G2
W28	GND 150	GND 73	G4
W30	GND 151	GND 74	G7
Y13	GND 152	GND 75	G10
Y14	GND 153	GND 76	G13
Y15	GND 154	GND 77	G16
Y16	GND 155	GND 78	G19
Y17	GND 156	GND 79	G22
Y18	GND 157	GND 8	AB16
AK2	GND 158	GND 80	G24
AE8	GND 159	GND 81	G25
AB11	GND 160	GND 82	G28
AB14	GND 161	GND 83	G30
P24	GND 162	GND 84	H8
R24	GND 163	GND 85	H24
T31	GND 164	GND 86	J23
V27	GND 165	GND 87	K2
AE23	GND 166	GND 88	K4
L22	GND 167	GND 89	K7
AE2	GND 16	GND 9	AB19
AE4	GND 17	GND 90	K13
AE7	GND 18	GND 91	AE24
AE10	GND 19	GND 92	K19
A30	GND 2	GND 93	K22
AE13	GND 20	GND 94	AE25
K30	GND 96	GND 95	K28
L13	GND 97		
L14	GND 98		
L15	GND 99		

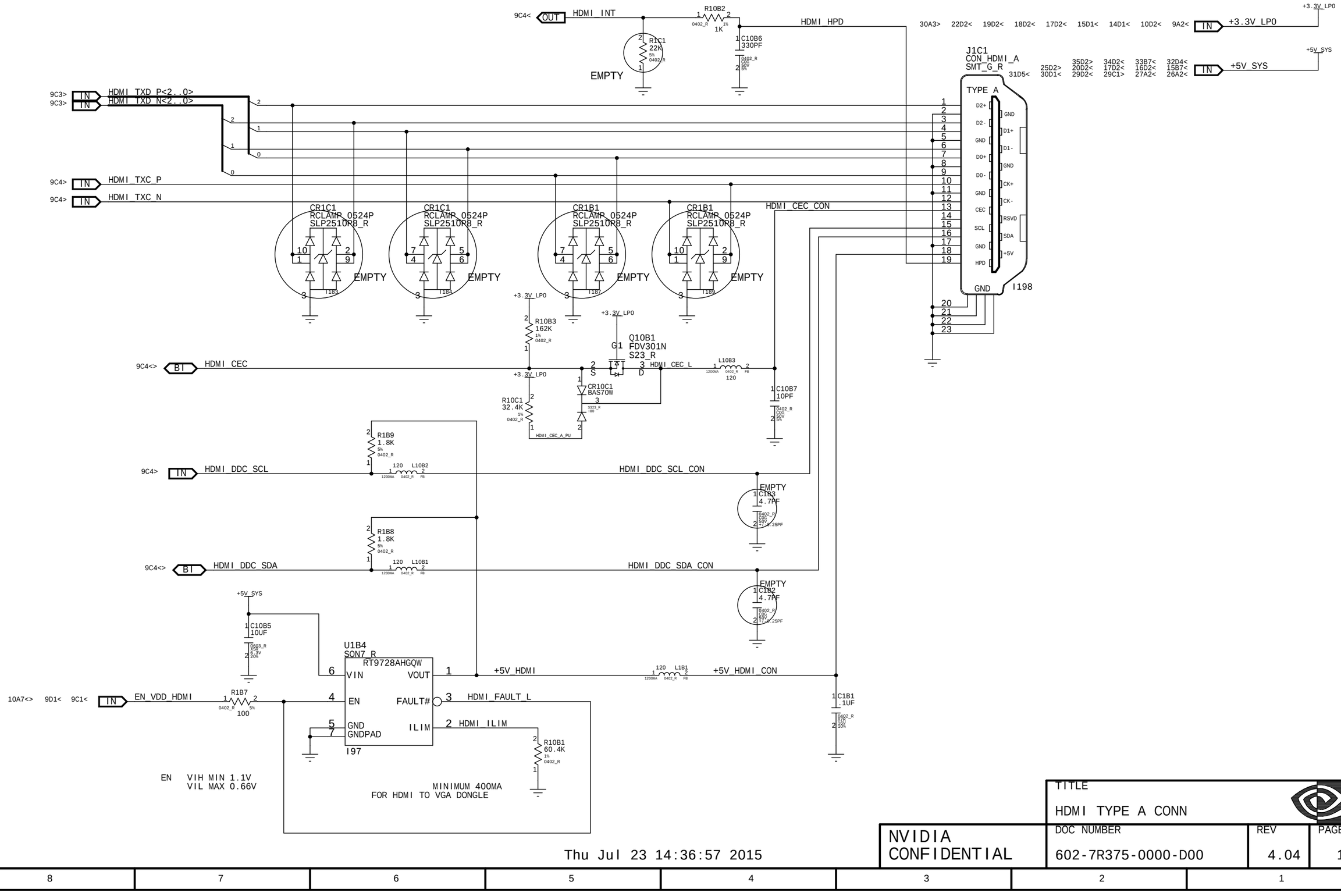
I358

Thu Jul 23 14:36:57 2015

NVIDIA
CONFIDENTIAL

TITLE
TK1: GND

DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.04	12

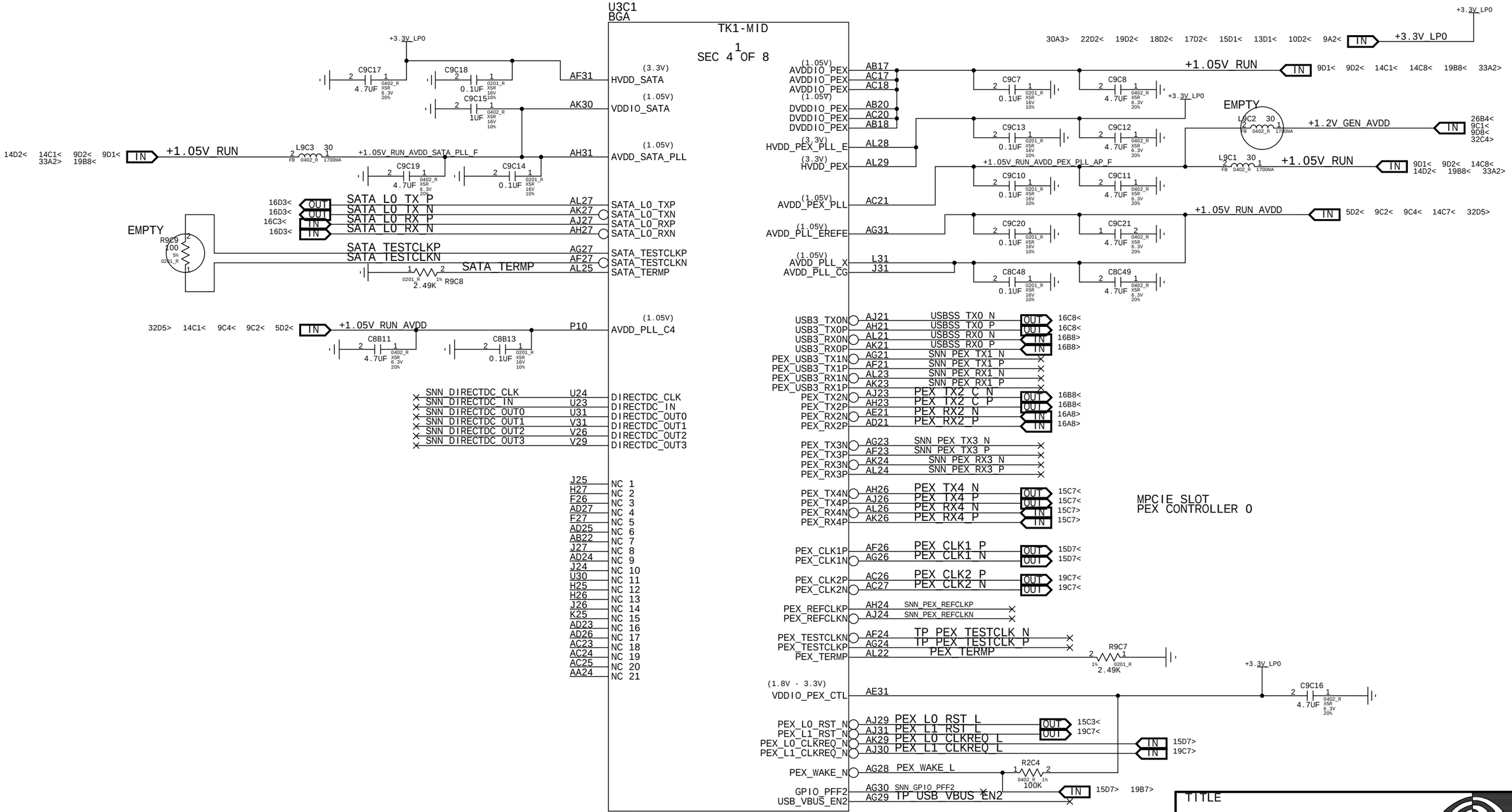


Thu Jul 23 14:36:57 2015

NVIDIA CONFIDENTIAL

TITLE: HDMI TYPE A CONN

DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.04	13

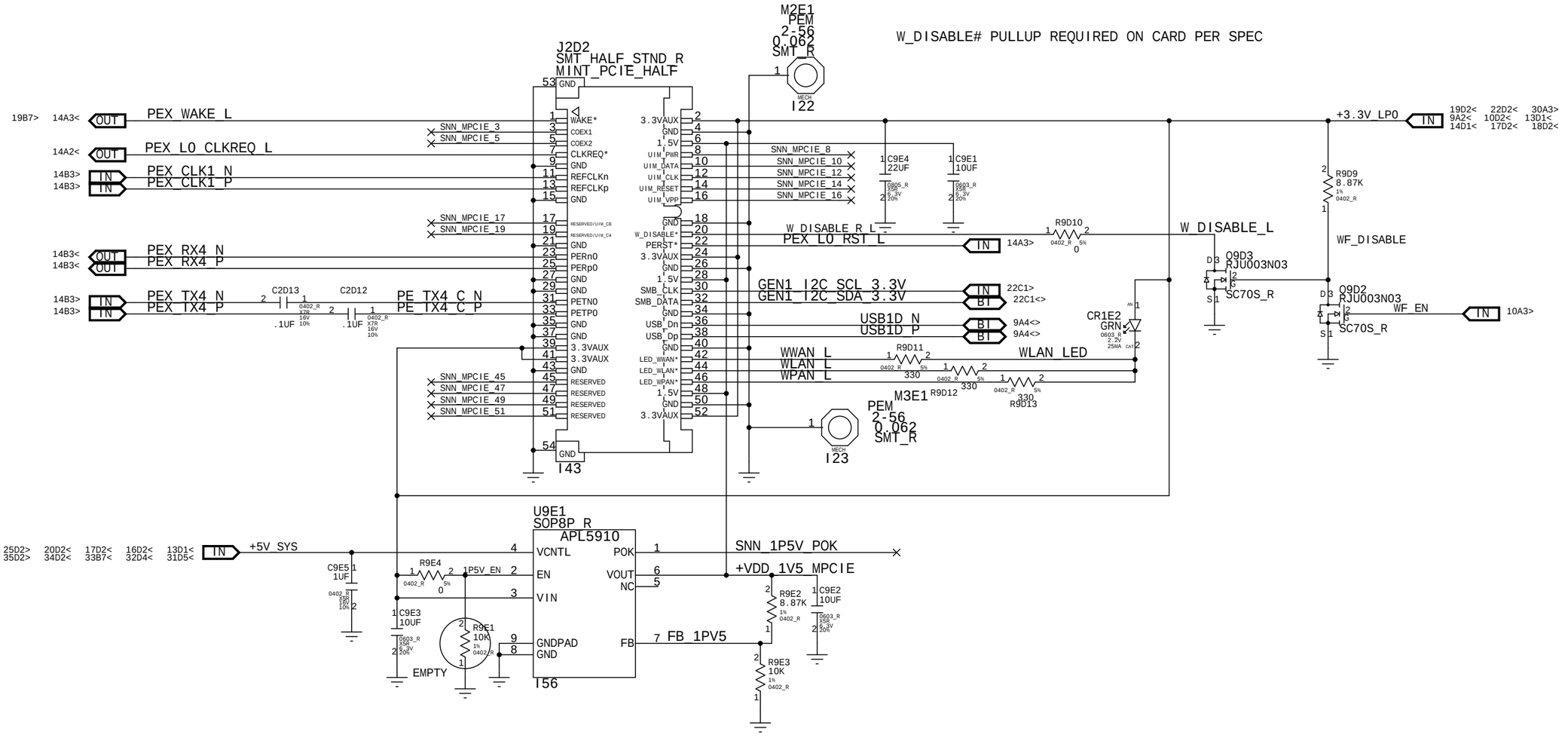


TITLE
TK1: SATA, PEX, USB 3.0

NVIDIA CONFIDENTIAL

DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.04	14

Thu Jul 23 14:36:58 2015



Thu Jul 23 14:36:58 2015

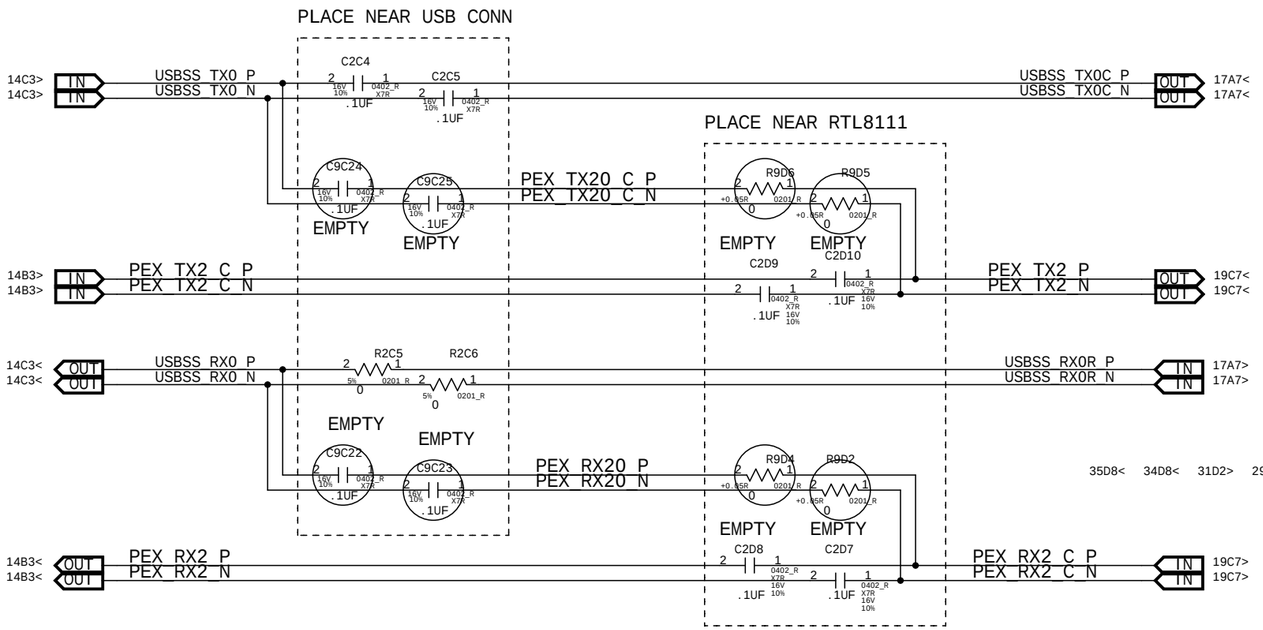
NVIDIA CONFIDENTIAL

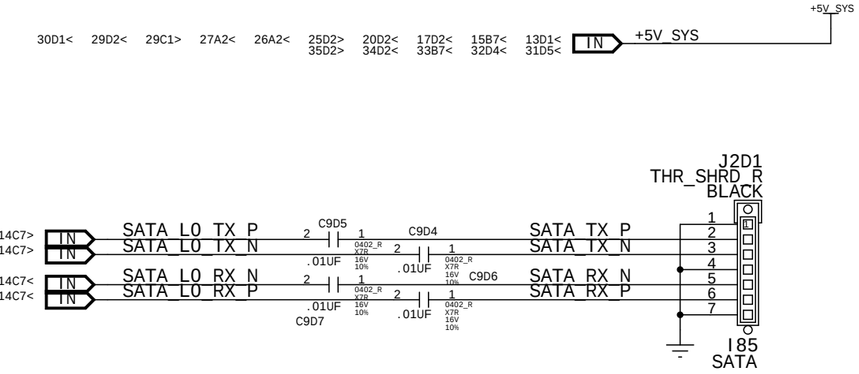
TITLE: MINI HALF PCIE

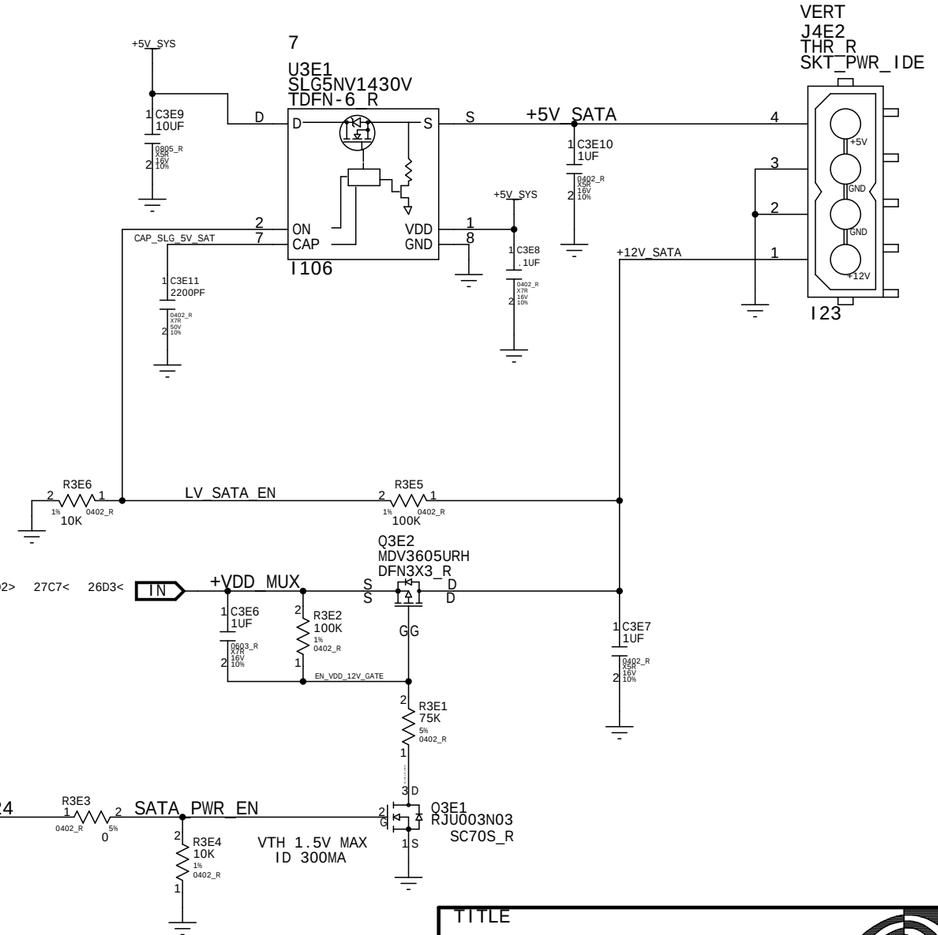
DOC NUMBER: 602-7R375-0000-D00

REV: 4.04

PAGE: 15



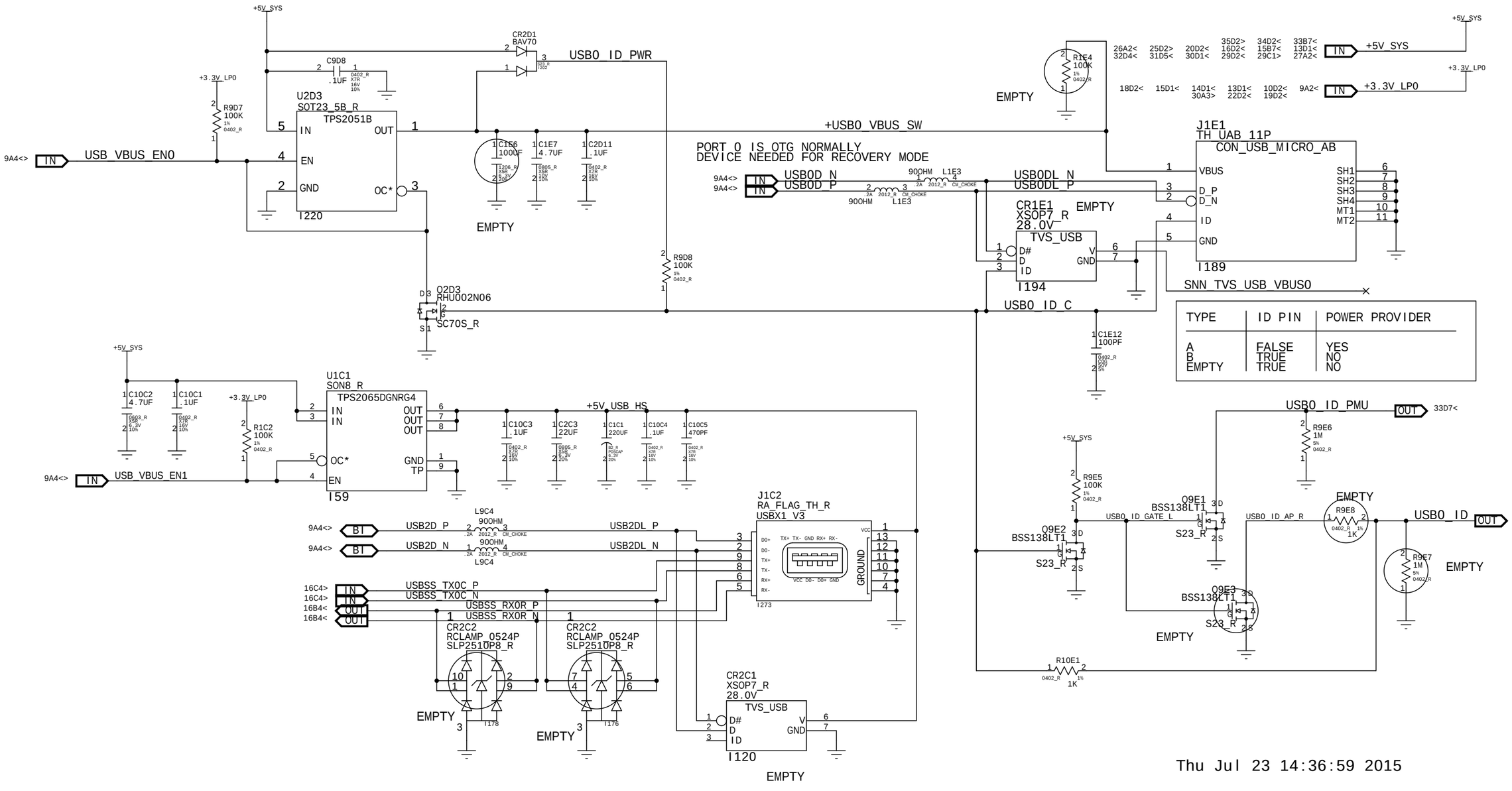




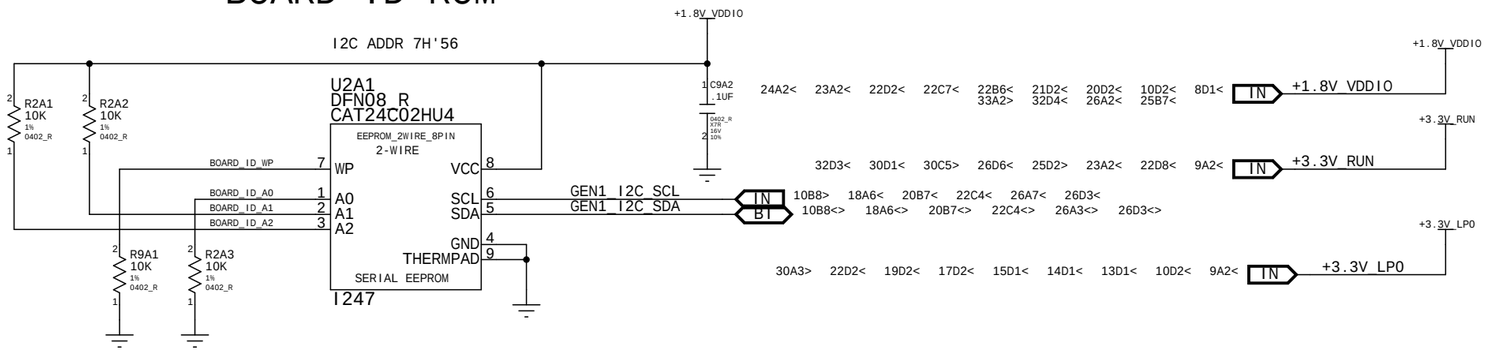
Thu Jul 23 14:36:58 2015

NVIDIA CONFIDENTIAL

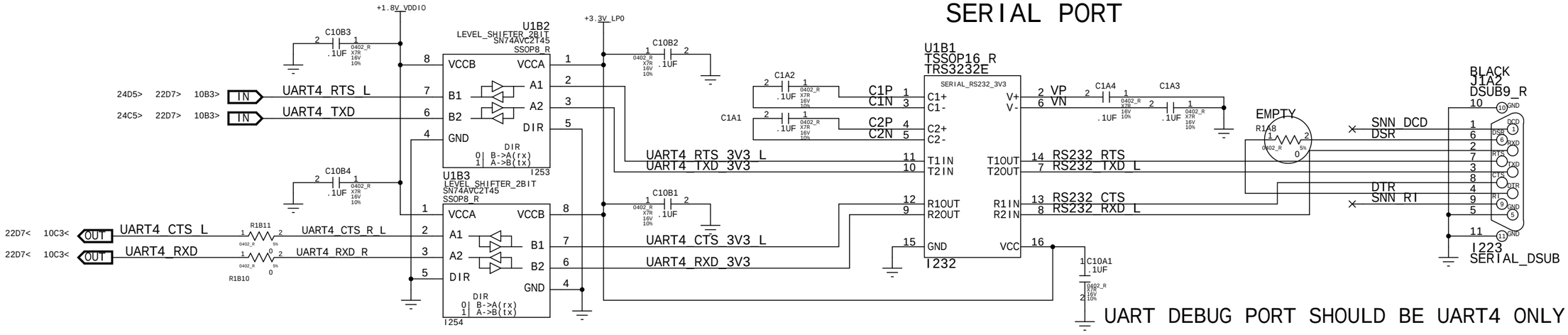
TITLE			
PEX OPTIONS AND SATA			
DOC NUMBER	REV	PAGE	
602-7R375-0000-D00	4.04	16	


+5V_SYS
CR2D1
BAV70
USB0_ID_PWR
C9D8
.1UF
+3.3V_LP0
R9D7
100K
U2D3
SOT23_5B_R
TPS2051B
IN
OUT
EN
GND
OC*
I220
9A4<>
IN
USB_VBUS_EN0
+USB0_VBUS_SW
C1E6
100UF
C1E7
4.7UF
C2D11
.1UF
EMPTY
R1E4
100K
EMPTY
PORT 0 IS OTG NORMALLY
DEVICE NEEDED FOR RECOVERY MODE
USB0D_N
USB0D_P
90OHM
L1E3
CM_CHOKE
USB0DL_N
USB0DL_P
CR1E1
XSOP7_R
28.0V
TVS_USB
D#
D
ID
V
GND
I194
EMPTY
J1E1
TH_UAB_11P
CON_USB_MICRO_AB
VBUS
D_P
D_N
ID
GND
SH1
SH2
SH3
SH4
MT1
MT2
I189
SNN_TVS_USB_VBUS0
R9D8
100K
Q2D3
RHU002N06
SC70S_R
USB0_ID_C
C1E12
100PF
TYPE | ID PIN | POWER PROVIDER
A | FALSE | YES
B | TRUE | NO
EMPTY | TRUE | NO
26A2< 25D2> 20D2< 35D2> 34D2< 33B7<
32D4< 31D5< 30D1< 16D2< 15B7< 13D1< 27A2<
29D2< 29C1>
18D2< 15D1< 14D1< 13D1< 10D2< 9A2<
30A3< 22D2< 19D2<
U1C1
SON8_R
TPS2065DGNRG4
IN
OUT
OC*
GND
TP
EN
I59
C10C2
4.7UF
C10C1
.1UF
R1C2
100K
C10C3
.1UF
C2C3
22UF
C1C1
220UF
C10C4
.1UF
C10C5
470PF
+5V_USB_HS
USB_VBUS_EN1
L9C4
90OHM
USB2D_P
USB2D_N
USB2DL_P
USB2DL_N
J1C2
RA_FLAG_TH_R
USBX1_V3
D0+
D0-
TX+
TX-
RX+
RX-
VCC
GROUND
I273
USBSS_TX0C_P
USBSS_TX0C_N
USBSS_RX0R_P
USBSS_RX0R_N
CR2C2
RCLAMP_0524P
SLP2510P8_R
I178
I176
EMPTY
CR2C1
XSOP7_R
28.0V
TVS_USB
I120
EMPTY
USB0_ID_PMU
OUT
33D7<
R9E6
1M
R9E5
100K
Q9E1
BSS138LT1
Q9E2
BSS138LT1
Q9E3
BSS138LT1
S23_R
USB0_ID_GATE_L
USB0_ID_AP_R
R9E8
1K
EMPTY
USB0_ID
OUT
9A4<
R9E7
1M
EMPTY
R10E1
1K
Thu Jul 23 14:36:59 2015
TITLE
USB PORTS
NVIDIA
CONFIDENTIAL
DOC NUMBER
602-7R375-0000-D00
REV
4.04
PAGE
17

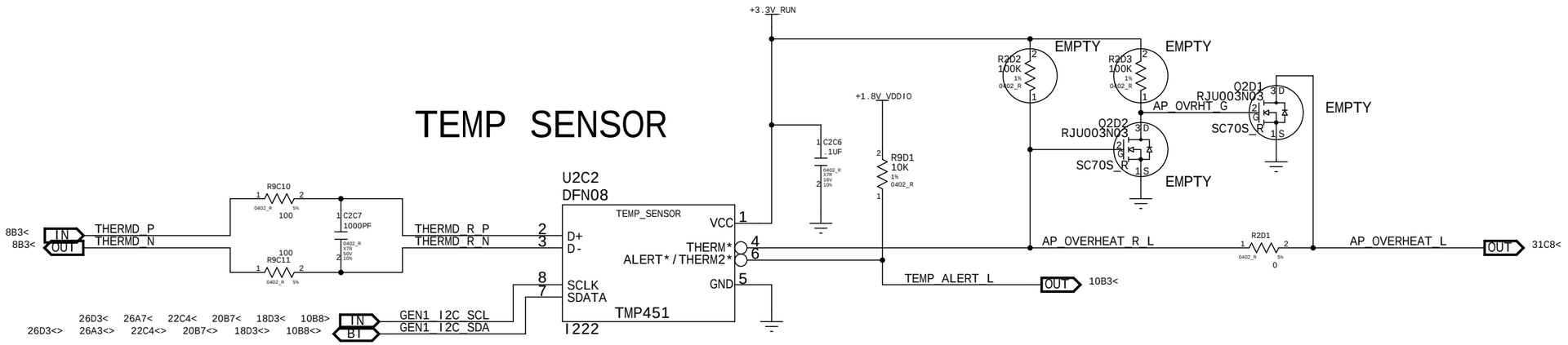
BOARD ID ROM



SERIAL PORT



TEMP SENSOR



Thu Jul 23 14:36:59 2015

NVIDIA CONFIDENTIAL	DOC NUMBER 602-7R375-0000-D00	REV 4.04	PAGE 18

TITLE: TEMP SENSOR, SERIAL, ID

RISE TIME ON 3.3V RAIL MUST BE > 0.5MS

30A3> 22D2< 18D2< 17D2< 15D1< 14D1< 13D1< 10D2< 9A2< IN +3.3V_LPO

+3.3V_LPO

EMPTY

R9D3 10K 1% 0402_R

U2D2
QFN-33_R
RTL8111GS

14B3> IN PEX_CLK2_P
14A3> IN PEX_CLK2_N
14A2< OUT PEX_L1_CLKREQ_L
16B4> IN PEX_TX2_P
16B4> IN PEX_TX2_N
16A4< OUT PEX_RX2_C_P
16A4< OUT PEX_RX2_C_N
14A3> IN PEX_L1_RST_L

15 REFCLK_P
16 REFCLK_N
12 CLKREQB
13 HSIP
14 HSIN
17 HSOP
18 HSON
19 PERSTB

AVDD33 11
AVDD33 32
VDDREG 23
REGOUT 24 +1.05V_LAN_REGOUT_L
AVDD10 3
AVDD10 8
AVDD10 30
DVDD10 22

C1D4 .1UF 0402_R X7R 16V 10%
C1D2 .1UF 0402_R X7R 16V 10%
EMPTY EMPTY
C1D5 4.7UF 0603_R X5R 6.3V 10%
C1D3 4.7UF 0603_R X5R 6.3V 10%
C9D3 .1UF 0402_R X7R 16V 10%
C9D2 4.7UF 0603_R X5R 6.3V 10%

TWO INDUCTOR FOOTPRINTS
FOR AVAILABILITY REASONS

EMPTY
4.7UH L2D1 55MA 2016_R SMD
4.7UH
L2D2 0.7A SMD_R SMD

C2D2 .1UF 0402_R X7R 16V 10%
C2D1 4.7UF 0603_R X5R 6.3V 10%
C10D2 .1UF 0402_R X7R 16V 10%
C10D3 .1UF 0402_R X7R 16V 10%
C10D1 .1UF 0402_R X7R 16V 10%
+1.05V_LAN_REGOUT
C2D4 .1UF 0402_R X7R 16V 10%
C2D6 .1UF 0402_R X5R 16V 10%
C2D5 .1UF 0402_R X7R 16V 10%

BIOS PULL HIGH/LOW ON PIN
TO ISOLATE LEAVE/ENTER DSM

EMPTY
R2C9 100K 1% 0402_R
R2D10 100K 1% 0402_R
LAN_ISOLATE_L 20 ISOLATEB

EMPTY
R9D14 10K 0402_R 1%
30C8< 30A8< 27C4< 31C2< IN PMU_REGEN3
LAN_ISOLATE
Q9D1 MMBT3904
EMPTY
S363_R

33A2> 9D2< 14C1< 14D2< 14C8< 9D1< IN +1.05V_RUN
R2D11 10K 0402_R 1%
LAN_ISO_BASE
Q9D1 MMBT3904
S303_R
EMPTY
21 LANWAKEB

EMPTY

15D7> 14A3< OUT PEX_WAKE_L
R2D8 0 0402_R 5%
PEX0_WAKE_R_L

XTAL_LAN_P 28 CKXTAL1
XTAL_LAN_N 29 CKXTAL2
C2D3 20PF 0402_R C0G 50V 5%
RC49_R 1359
Y2C1 25.000MHZ 30_30PPM
C1D1 20PF 0402_R C0G 50V 5%
33 GND

I404

MDIP0 1 LAN_MDI0_P
MDIN0 2 LAN_MDI0_N
MDIP1 4 LAN_MDI1_P
MDIN1 5 LAN_MDI1_N
MDIP2 6 LAN_MDI2_P
MDIN2 7 LAN_MDI2_N
MDIP3 9 LAN_MDI3_P
MDIN3 10 LAN_MDI3_N
RSET 31 LAN_RSET
R1D1 2.49K 0402_R 1%

LED0 27 LAN_LED0
LED1/GPO 26 LAN_LED1
LED2 25 LAN_LED2
R2D4 240 0402_R 1%
R2D5 240 0402_R 1%
R2D6 510 0402_R 5%
LAN_LED_100
LAN_LED_1000
LAN_LED0_ACT_L

LINK 10 = OFF
LINK 100 = SOLID ORANGE
LINK 1000 = SOLID GREEN
LINK ACT = BLINK YELLOW

J1D1
RJ45_2_R
RJ45_1X1GBIT_MAG_LED

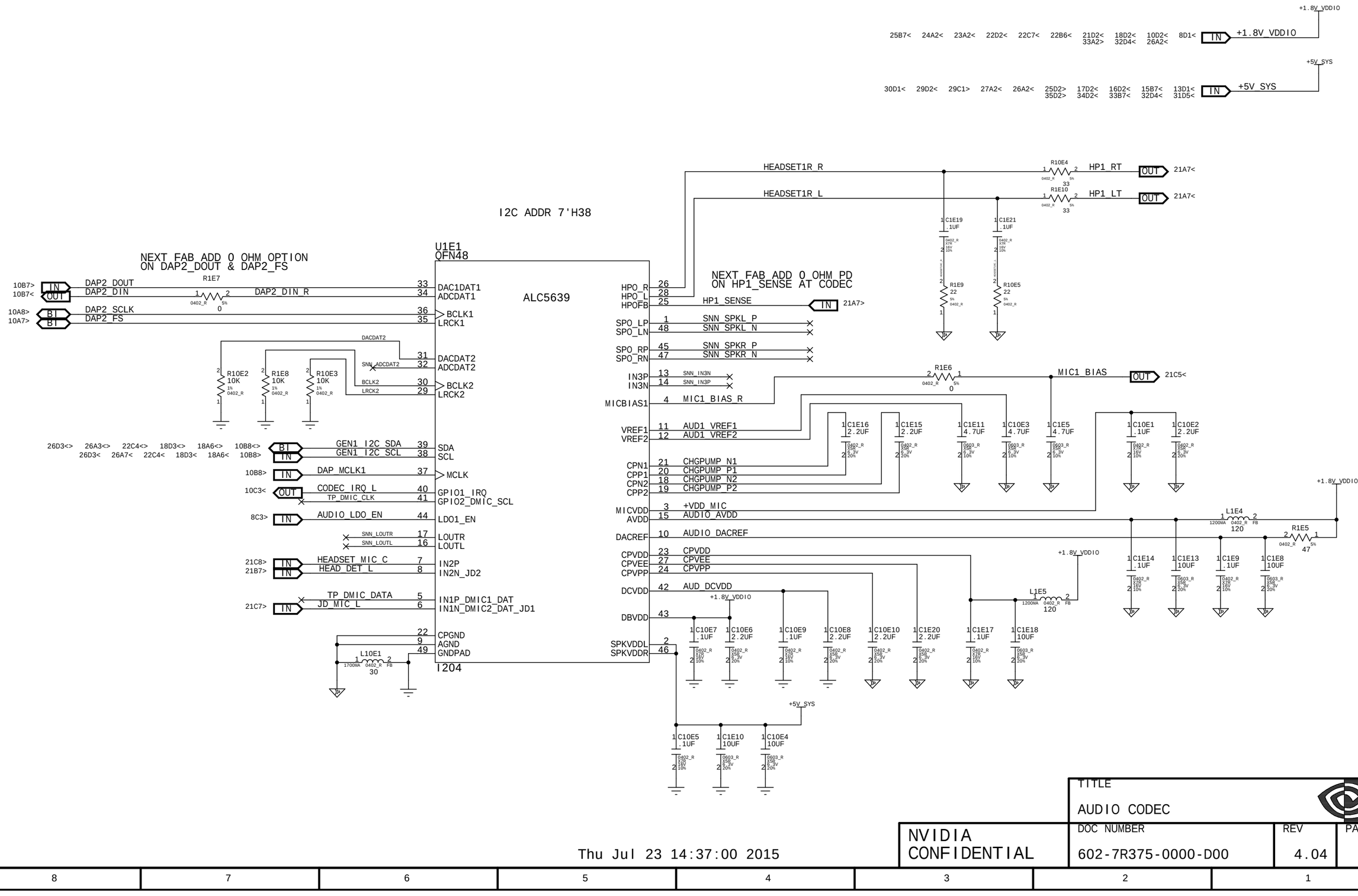
MX0+ 9
MX0- 10
MX1+ 7
MX1- 8
MX2+ 5
MX2- 6
MX3+ 3
MX3- 4
I382 16 14 15 13
(8)TD3- (7)TD3+ (6)TD1- (5)TD2- (4)TD2+ (3)TD1+ (2)TD0- (1)TD0+
ORNG GRN YLW

VCC 2
CH_GND 1
LAN_TRCT1
C1C2 .01UF 0402_R X7R 16V 10%
LAN_CH_GND
R1D2 0 0402_R 5%
GND 11
GND 12
+3.3V_LPO
C1D7 .1UF 0402_R X7R 16V 10%
EMPTY

Thu Jul 23 14:36:59 2015

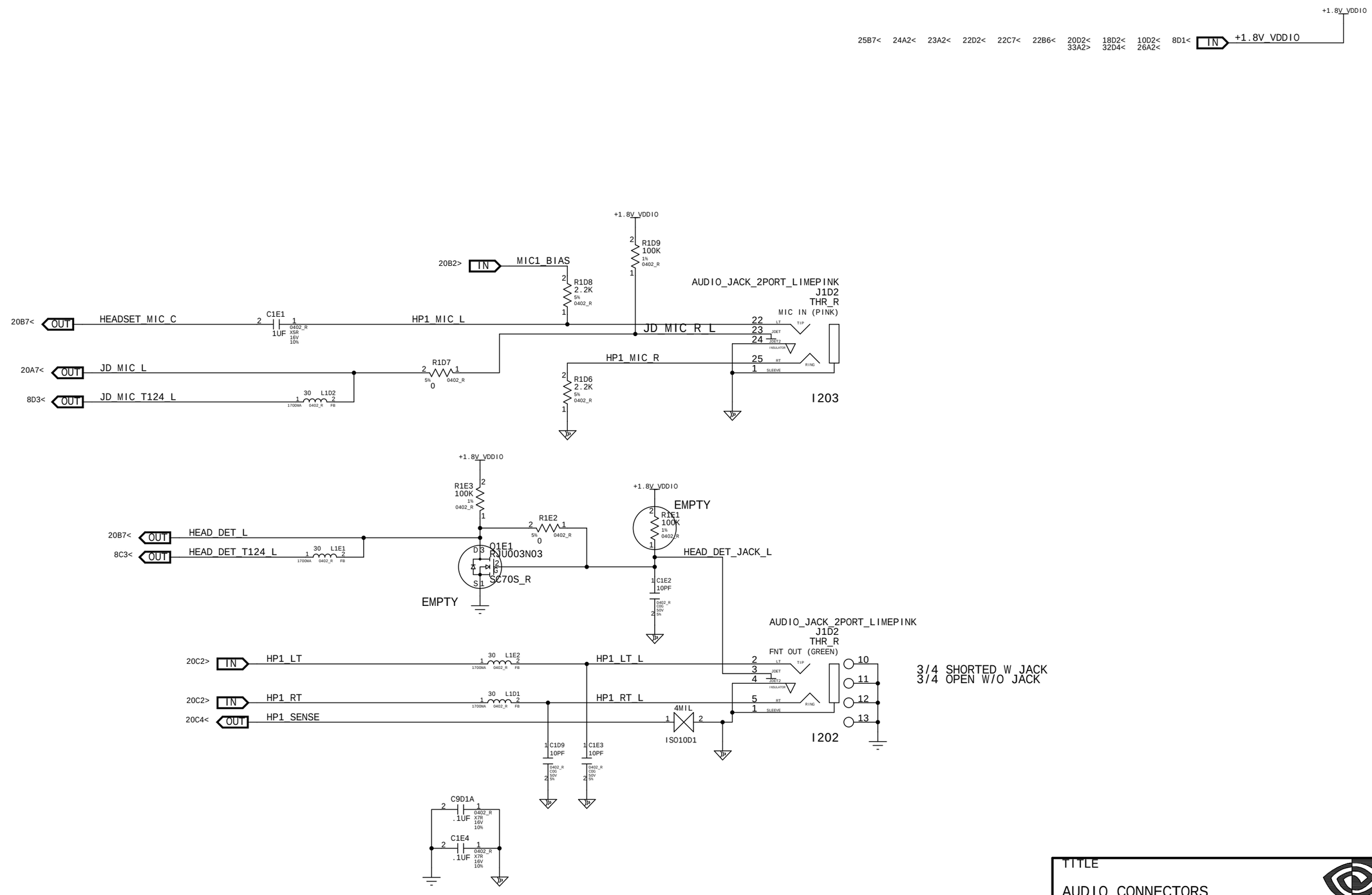
NVIDIA CONFIDENTIAL

TITLE: PEX GIGE LAN/PHY
DOC NUMBER: 602-7R375-0000-D00
REV: 4.04
PAGE: 19



Thu Jul 23 14:37:00 2015

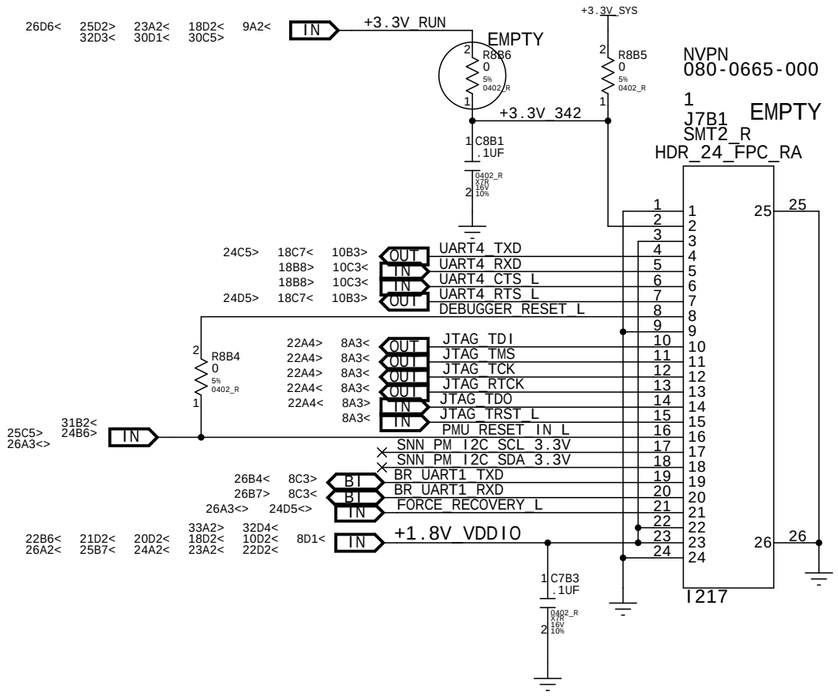
NVIDIA CONFIDENTIAL	TITLE: AUDIO CODEC		
	DOC NUMBER: 602-7R375-0000-D00	REV: 4.04	PAGE: 20



Thu Jul 23 14:37:00 2015

NVIDIA CONFIDENTIAL	DOC NUMBER 602-7R375-0000-D00	REV 4.04	PAGE 21

TITLE
AUDIO CONNECTORS

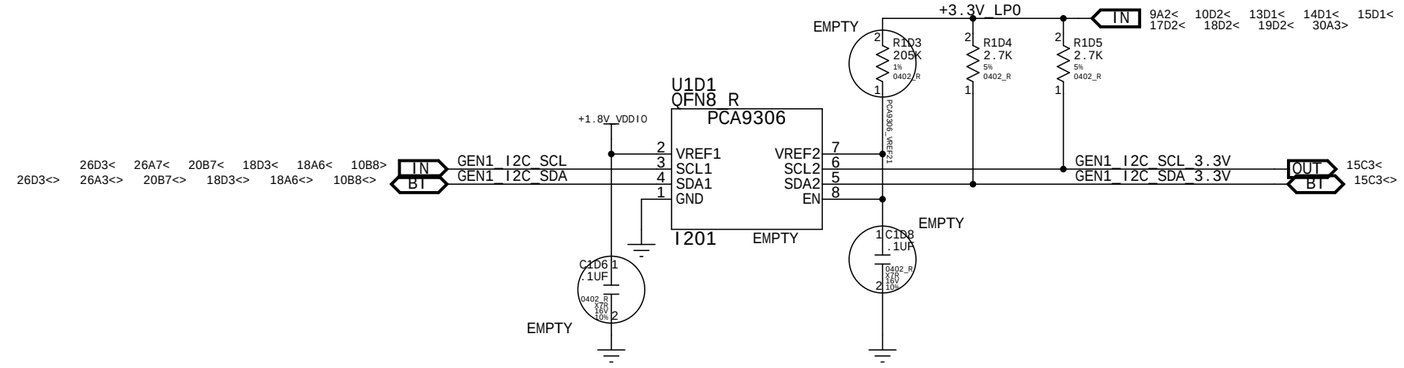


STUFF THIS DEBUG CONN
OR JTAG & DSUB, NOT BOTH

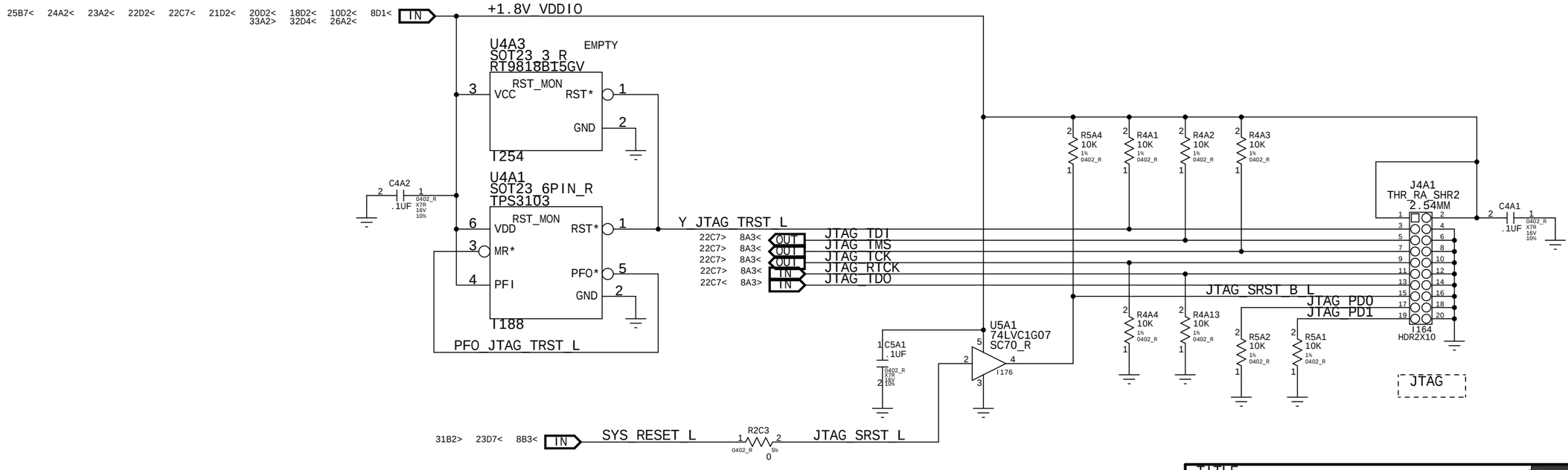
25B7< 24A2< 23A2< 22C7< 22B6< 21D2< 20D2< 18D2< 10D2< 8D1<
33A2> 32D4< 26A2<
IN
+1.8V_VDDIO

32B8< 30D1< 28D2< 28C1> 26D6<
IN
+3.3V_SYS

I2C LEVEL TRANSLATOR



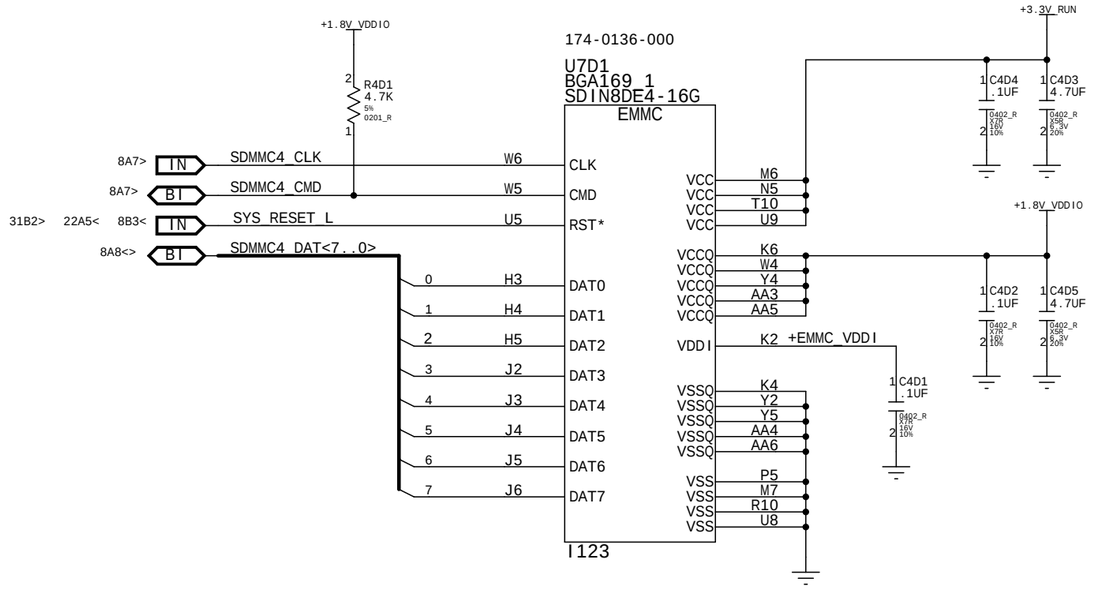
RESET SUPERVISOR ALLOWS EXTERNAL ARM JTAG DEBUGGER TO DETECT POWER CYCLE
DEPOPULATE SUPERVISOR FOR PRODUCTION VERSIONS?



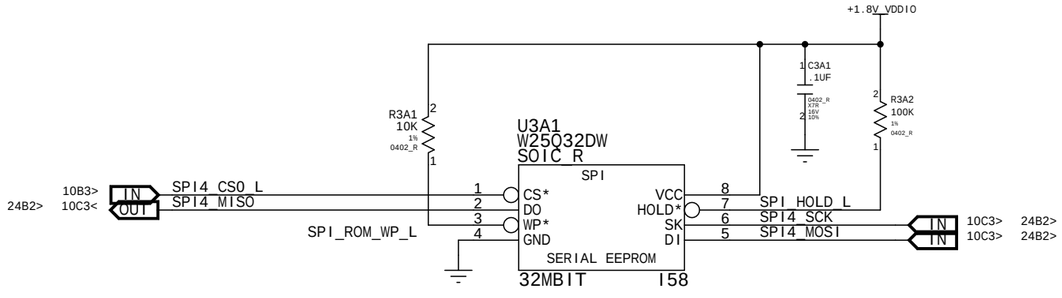
TITLE: JTAG CONN; I2C TRANSLATER			
NVIDIA CONFIDENTIAL	DOC NUMBER: 602-7R375-0000-D00	REV: 4.04	PAGE: 22

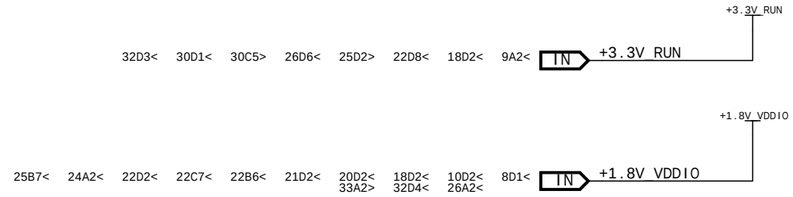
Thu Jul 23 14:37:00 2015

EMMC 4.51



SPI BOOT ROM



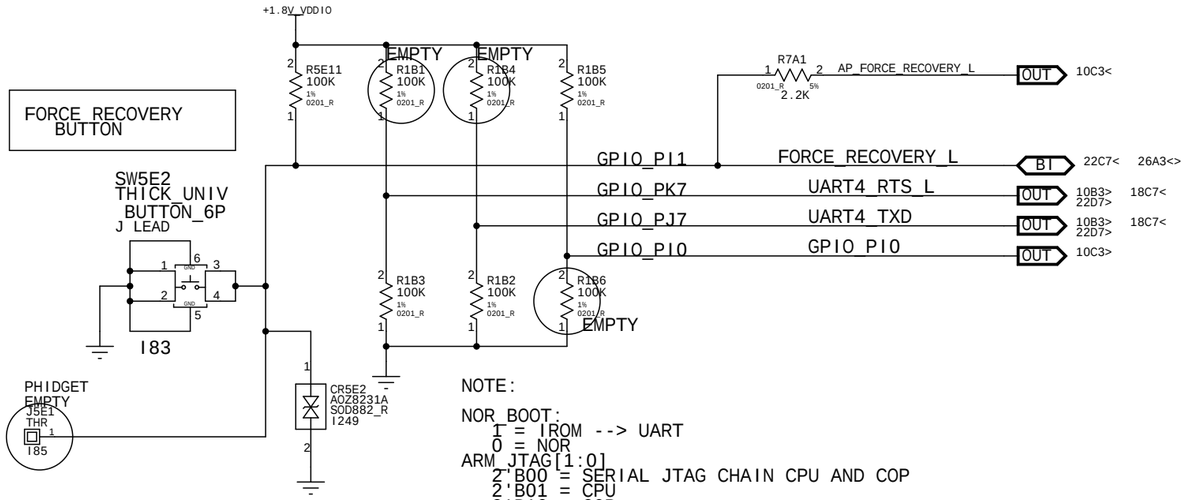


Thu Jul 23 14:37:00 2015

NVIDIA CONFIDENTIAL

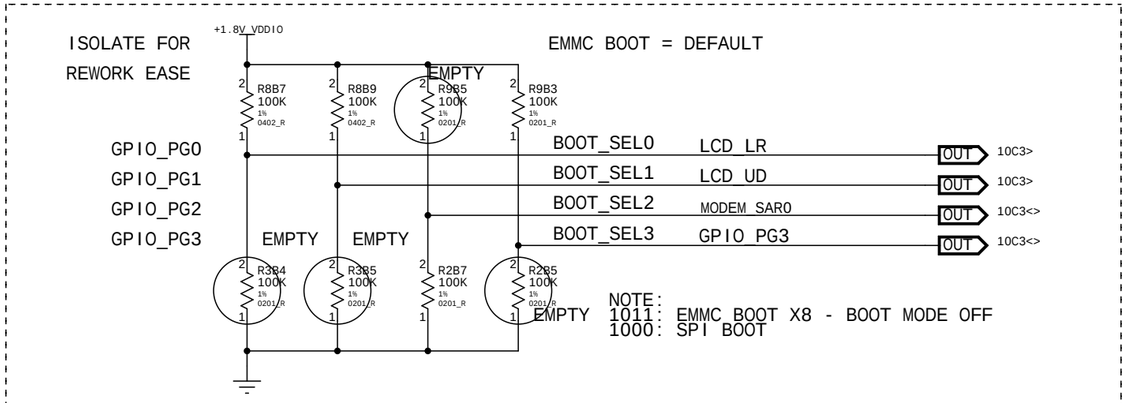
TITLE: EMMC,SPI ROM

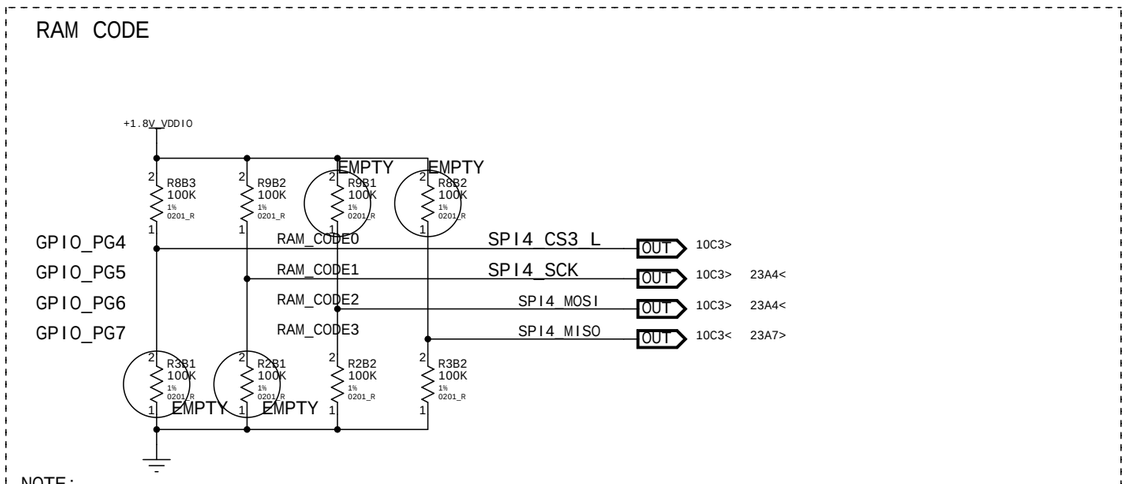
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.04	23

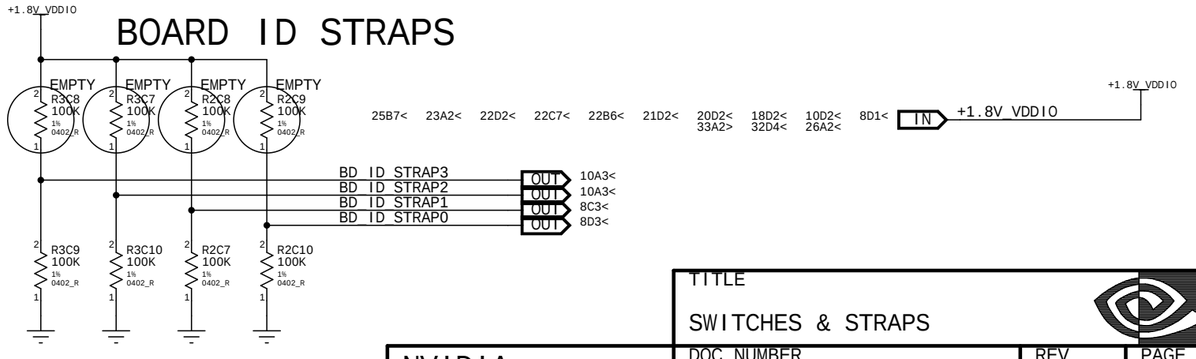


NOTE:

NOR_BOOT:
1 = IROM --> UART
0 = NOR
ARM_JTAG[1:0]
2'B00 = SERIAL JTAG CHAIN CPU AND COP
2'B01 = CPU
2'B10 = COP
2'B11 = SERIAL_ALT







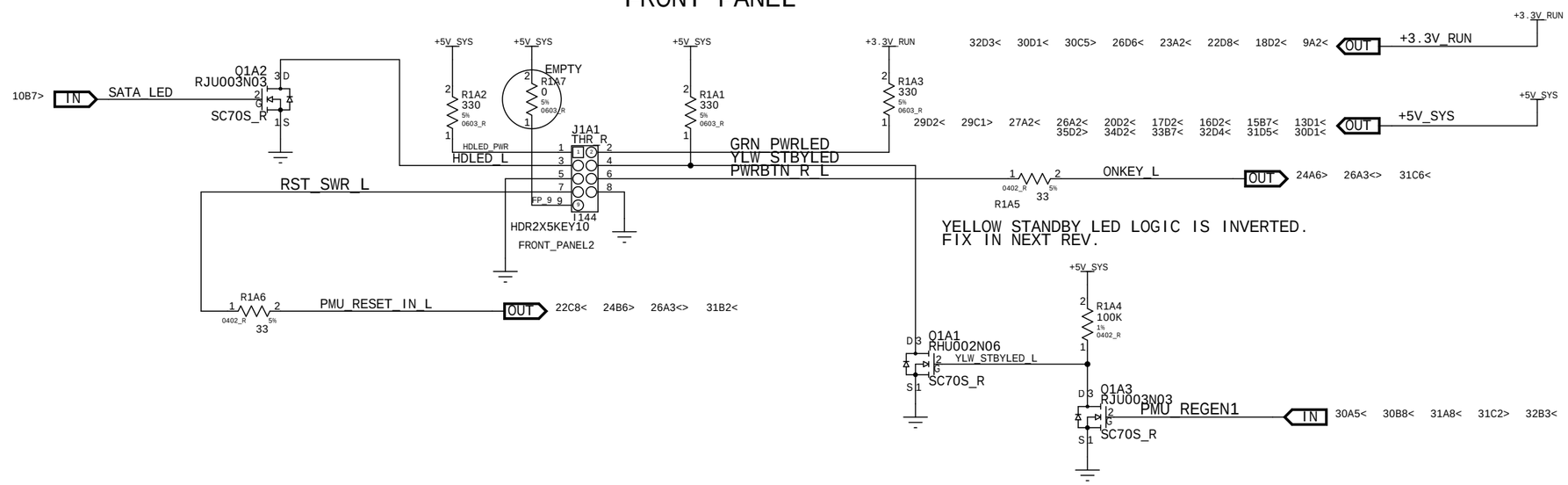
Thu Jul 23 14:37:01 2015

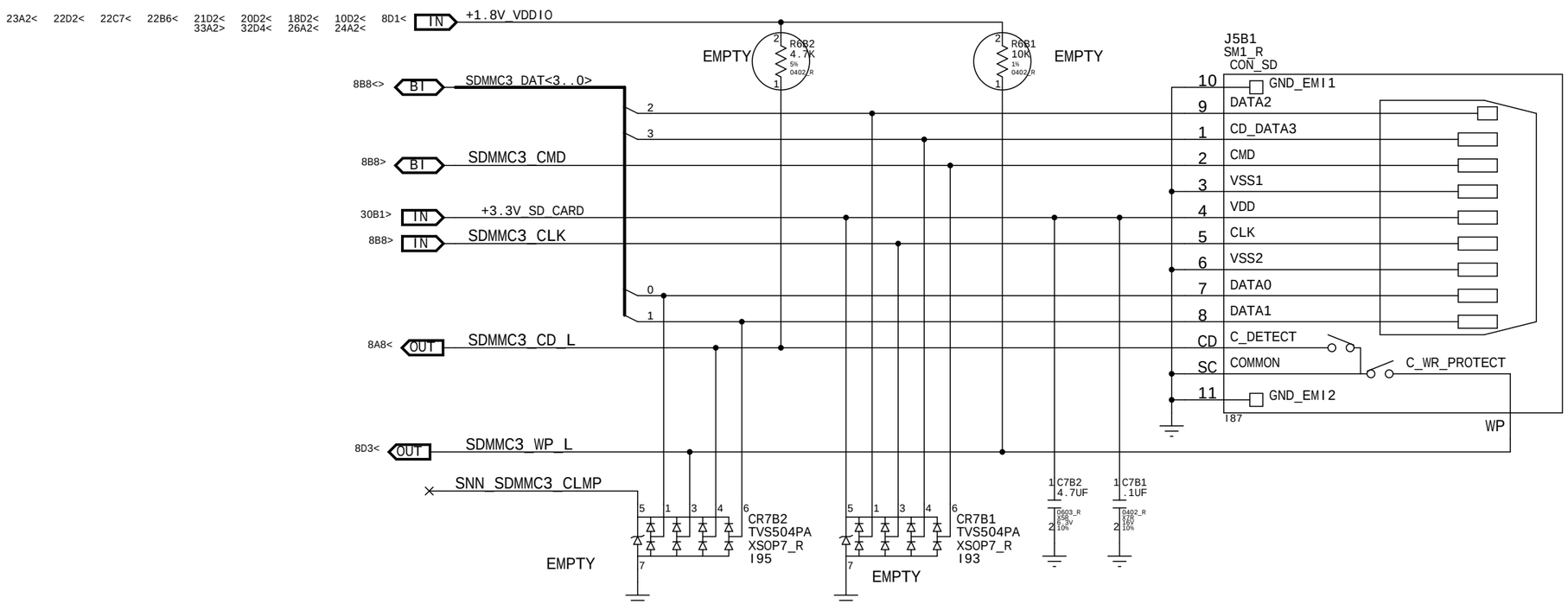
TITLE
SWITCHES & STRAPS

NVIDIA CONFIDENTIAL

DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.04	24

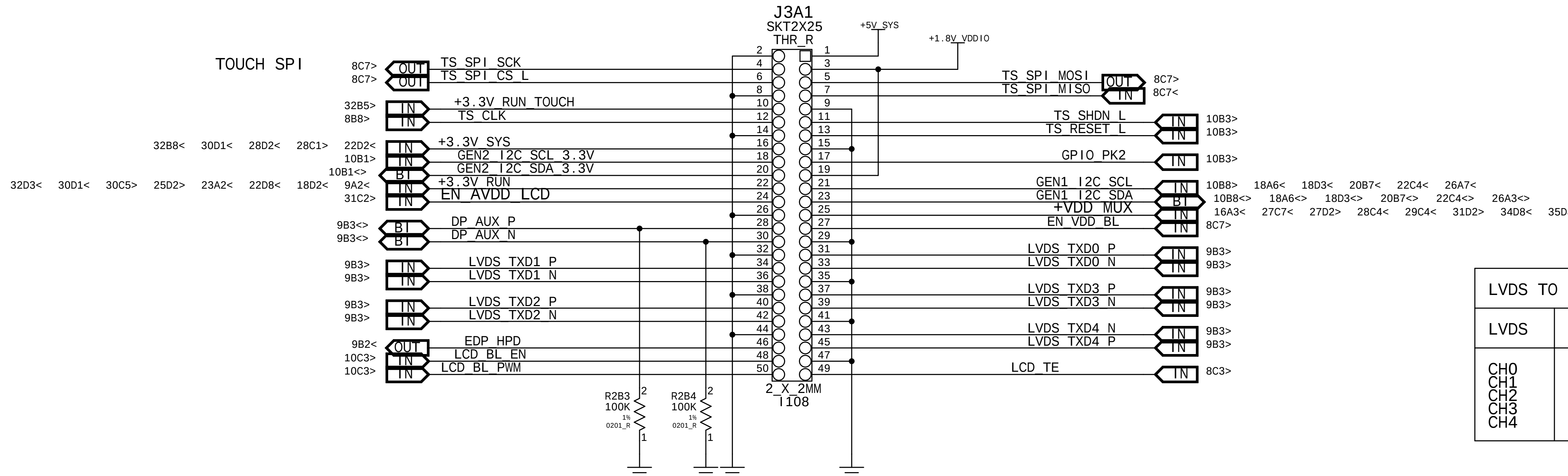
FRONT PANEL





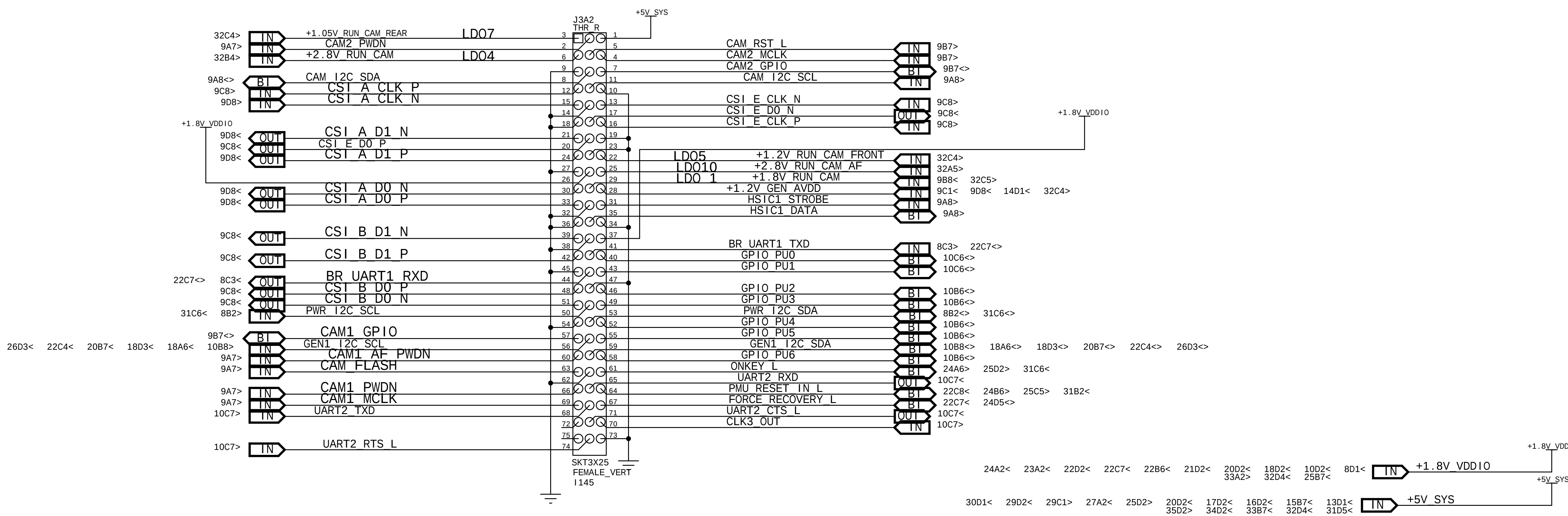
Thu Jul 23 17:09:29 2015

NVIDIA CONFIDENTIAL	TITLE: SD CONN & FRONT PANEL HDR		
	DOC NUMBER: 602-7R375-0000-D00	REV: 4.04	PAGE: 25



LVDS TO EDP MUX	
LVDS	EDP
CH0	CH2
CH1	CH1
CH2	CH0
CH3	---
CH4	CH3

NOTES:
LVDS / EDP MODULES MAY USE +3.3V_RUN
OR +3.3V_RUN GATED BY EN_AVDD_LCD (PMIC GPIO4)



Thu Jul 23 14:37:01 2015

NVIDIA CONFIDENTIAL

TITLE		
EXP:TOUCH/DISP & GENERAL		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.04	26

J5C1
THR_R
PWR_JACK_5P

1480

AC JACK

750-0147-000 FOR 12V_BRICK
030-0364-000 FOR AC POWER CORD

+VDD_ACIN

R5C8 3.9 5% 0603_R
R5C9 20K 1% 0402_R
R5C10 20K 1% 0402_R
R5C11 0.005 1% 1206_R
VDD_AC_SNUB
C5C11 10UF 1206_R 25V 10%

BLEED RESISTORS

+VDD_MUX

C5D5 10UF 1206_R X6S 25V 10%
C5D1 10UF 1206_R X6S 25V 10%
C5D4 10UF 1206_R X6S 25V 10%

OUT 16A3< 26D3< 27C7< 28C4< 29C4< 31D2< 34D8< 35D8<

R4A5 0 5% 0603_R
EMPTY
R4A10 0 5% 0603_R
+5V_SYS
POWER_FAN_SRC

FAN_EN_L
R4A11 2.49K 1% 0402_R
Q4A2 AO3415 S23_R
R4A7 0 5% 0603_R
EMPTY
R4A12 2.49K 1% 0402_R
POWER_FAN

FAN_EN_DR
Q4A1 RJU003N03 SC70S_R

SNN_FAN_TACH
J4A2 4PIN_FAN_R
FAN HEADER
T501

NOTE: KB_ROW16 IS NOT
A TRUE PWM, ONLY ON/OFF

31C2> 30C8< 30A8< 19B8< IN PMU_REGEN3
R4A8 0 5% 0402_R
FAN_EN_GATE

8C3> IN FAN_PWM
R4A9 0 5% 0402_R
EMPTY

VREF2 IOUT=100UA

U5C1
U_SWREG_TPS51220
QFN32

35D8< 34D8< 31D2< 29C4< 28C4< 27D2< 26D3< 16A3< IN +VDD_MUX
C5C3 1UF 0805_R X5R 25V 10%

2/2
VIN 23
VREF2 13
+2V_STBY OUT 28B7< 29B7<
C5B2 .22UF 0402_R X5R 10V 10%
AGND0

VREF5 W/V5SW=5V IOUT(MIN)=200MA
VREF5 W/V5SW=5V IOUT(MAX)=400MA

RF[KOHM]=(1X10E+5)/FSW[KHZ]
FSW~500[KHZ]

TPS51220A_RF 3 RF
R5C4 200K 1% 0402_R
AGND0

VREG5 29 +5V_STBY OUT 27A7< 28C8<
C6C5 10UF 0805_R X5R 16V 10%

28C8< 27B4> 27A8< IN +3.3V_AON
OVP_ENABLED
D-CAP MODE
R5B1 0 5% 0402_R

TPS51220A_FUNC 11 FUNC
OVP_ENABLED
CURRENT MODE
R6B3 0 5% 0402_R
EMPTY
AGND0

VREG3 22 +3.3V_AON OUT 27A8< 27B8< 28C8<
C6C3 2.2UF 0603_R X5R 10V 10%

VREF3 IOUT(MIN)=10MA
VREF3 IOUT(MAX)=20MA

28C8< 27B4> IN +5V_STBY
VOCL_LOW_VOLTAGE
DISCHARGE ENABLE
R6B4 0 5% 0402_R

TPS51220A_TRIP 14 TRIP
VOCL_ULTRA_LOW_VOLTAGE
DISCHARGE ENABLE
R5B2 0 5% 0402_R
EMPTY

27B8< 27B4> 28C8< IN +3.3V_AON
R5B5 0 5% 0402_R
+VRTC_LDO_OUT EN PU OPTION??

AGND0 TPS51220A_REG_EN 12 REG_EN

29B8< 28B8< 31B6> IN AS3720_5V_VR_EN
R6B7 0 5% 0402_R
EMPTY

ISO6C1 10MIL
AGND0

GND 28

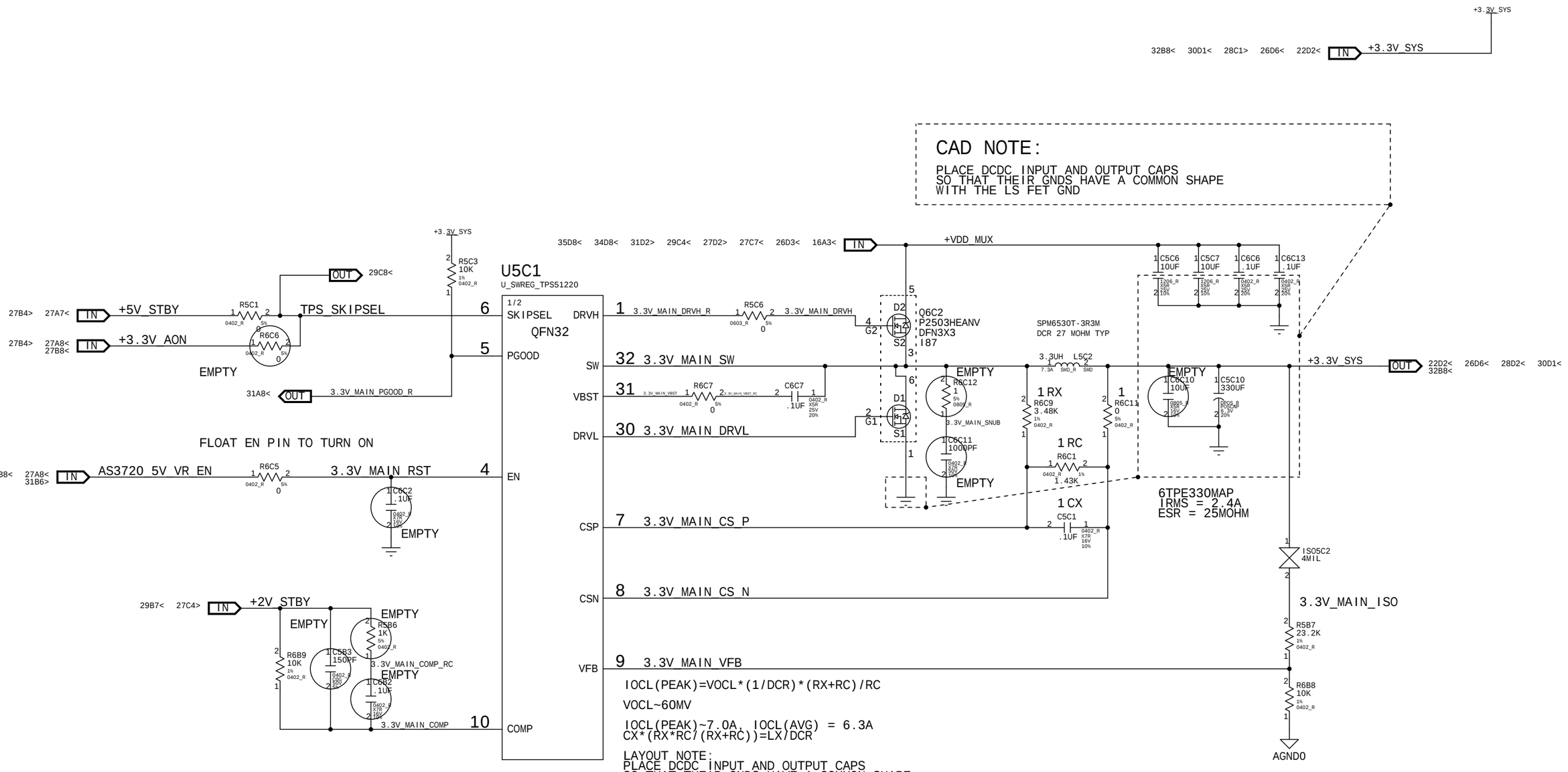
+5V_SYS
2 V5SW
C6C4 .1UF 0402_R X7R 16V 10%

GND_PAD 33
AGND0

30D1< 29D2< 29C1> 26A2< 25D2> 20D2< 35D2> 17D2< 34D2< 16D2< 33B7< 15B7< 32D4< 13D1< 31D5< IN +5V_SYS
+5V_SYS

Thu Jul 23 14:37:02 2015

NVIDIA CONFIDENTIAL	TITLE: DC IN	REV: 4.04	PAGE: 27
	DOC NUMBER: 602-7R375-0000-D00		



Thu Jul 23 14:37:02 2015

NVIDIA CONFIDENTIAL	DOC NUMBER: 602-7R375-0000-D00	REV: 4.04	PAGE: 28

TITLE: +3.3V VR

+5V_SYS

30D1< 29C1> 27A2< 26A2< 25D2> 20D2< 35D2> 17D2< 34D2> 16D2< 33B7< 15B7< 32D4< 13D1< 31D5< IN +5V_SYS

IOCL(PEAK)=VOCL*(1/DCR)*(RX+RC)/RC

VOCL~60MV

IOCL(PEAK)~9.8A
CX*(RX*RC/(RX+RC))=LX/DCR

LAYOUT NOTE:
PLACE DCDC INPUT AND OUTPUT CAPS
SO THAT THEIR GNDS HAVE A COMMON SHAPE
WITH THE LS FET GND

35D8< 34D8< 31D2> 28C4< 27D2> 27C7< 26D3< 16A3< IN +VDD_MUX

1 C5C4 10UF 1206_R X5R 25V 10%
1 C5C5 10UF 1206_R X5R 25V 10%
1 C6C8 .1UF 0402_R X5R 25V 20%
1 C6C12 .1UF 0402_R X5R 25V 20%

SPM6530T-3R3M
DCR 27MOHM TYP

CAD NOTE:

PLACE DCDC INPUT AND OUTPUT CAPS
SO THAT THEIR GNDS HAVE A COMMON SHAPE
WITH THE LS FET GND

+5V_SYS

EMPTY
R5C2 100K 1% 0402_R

28C7> IN TPS SKIPSEL → 19 SKIPSEL

5V_MAIN_PGOOD_R → 20 PGOOD

U5C1
U_SWREG_TPS51220
1/2
QFN32

24 DRVH — 5V_MAIN_DRVH_R — R5C5 0603_R 0 5% — 5V_MAIN_DRVH → D2 Q6C1 P2503HEANV DFN3X3 I227 (G2, S2)

25 SW — 5V_MAIN_SW → 3 → 3.3UH L5C1 7.3A SMD_R SMD → +5V_SYS → OUT

26 VBST — 5V_MAIN_VBST — R5C7 0402_R 0 5% — 5V_MAIN_VBST_RC — C5C8 .1UF 0402_R X5R 25V 20% → D1 (G1)

27 DRVL — 5V_MAIN_DRVL → 1 → EMPTY R6C3 1K 5% 0805_R → 5V_MAIN_SNUB → EMPTY 1C6C1 .1UF 0402_R X7R 16V 10%

EMPTY
R6C8 3.48K 1% 0402_R → RX
R6C10 0 5% 0402_R
EMPTY 1C6C9 10UF 0805_R X5R 16V 20%
1C5C9 330UF POSCAP 6.3V 20%

RC
R6C2 1.43K 0402_R 1%

CX
C5C2 .1UF 0402_R X7R 16V 10%

6TPE330MAP
IRMS = 2.4A
ESR = 25MOHM

FLOAT EN PIN TO TURN ON

28B8< 27A8< 31B6> IN AS3720_5V_VR_EN — R6C4 0 0402_R 5% — 5V_MAIN_RST → 21 EN

18 CSP — 5V_MAIN_CS_P

17 CSN — 5V_MAIN_CS_N

16 VFB — 5V_MAIN_VFB

28B7< 27C4> IN +2V_STBY

EMPTY
R6B5 10K 1% 0402_R
1C5B1 150PF 0402_R X5R 50V 10%
EMPTY R5B4 1K 5% 0402_R → 5V_MAIN_COMP_RC
EMPTY 1C6B1 .1UF 0402_R X7R 16V 10%

5V_MAIN_COMP → 15 COMP

ISO5C1 4MIL
5V_MAIN_ISO
R5B3 40.2K 1% 0402_R
R6B6 10K 1% 0402_R
AGND0

33B7< 29D2< 20D2< 13D1< 16D2< 26A2< 31D5< 35D2< 34D2< 30D1< 25D2< 15B7< 17D2< 27A2< 32D4<

RGV[KOHM]=200XIOUT(MAX)*IOUTMAX*VOUT/IOCL(PEAK*VDROOPMV

IOCL(PEAK)=VOCL*(1/DCR)*(RX+RC)/RC

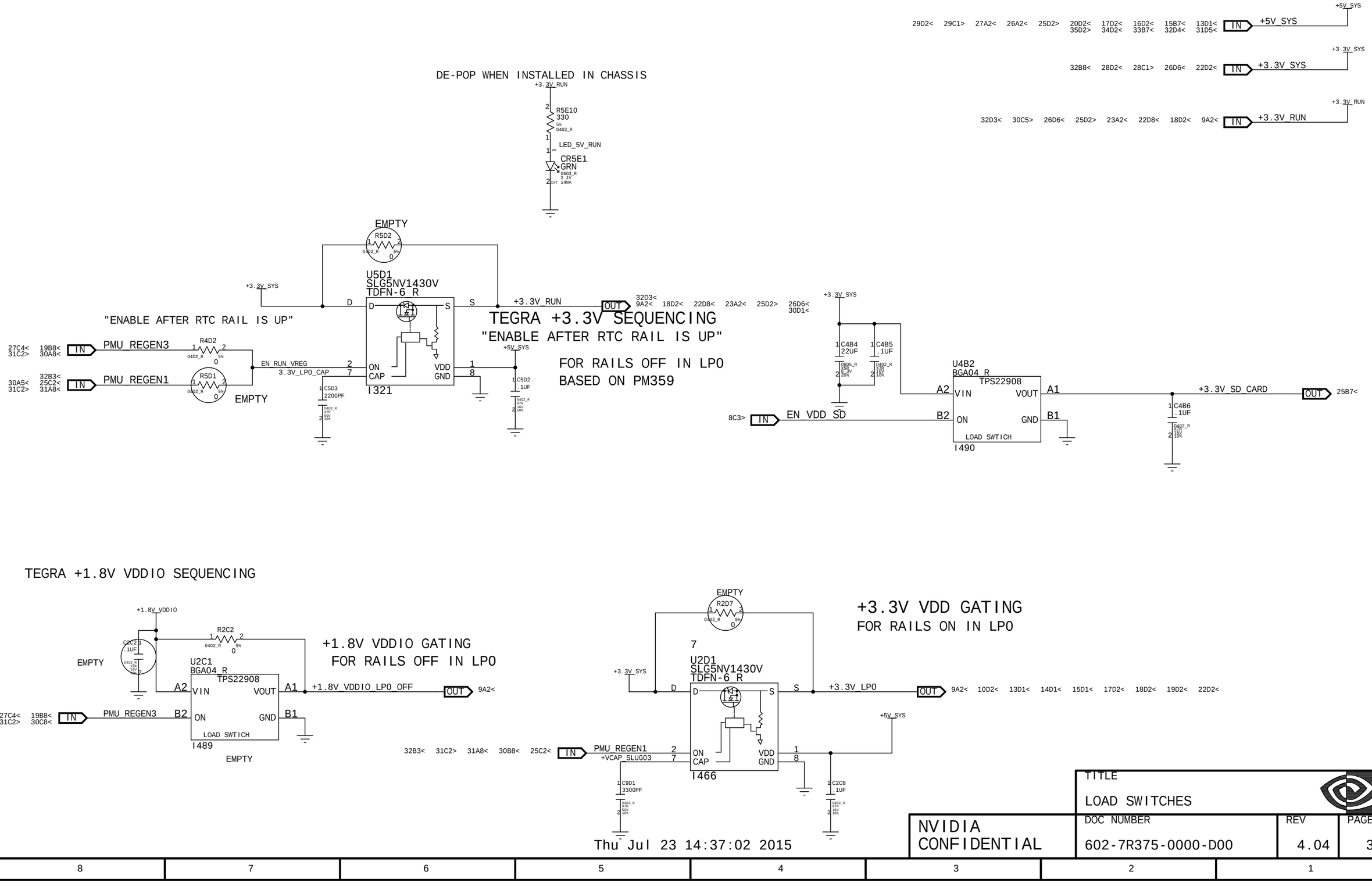
VOCL~60MV

IOCL(PEAK)~7.0A, IOCL(AVG) = 6.2A
CX*(RX*RC/(RX+RC))=LX/DCR

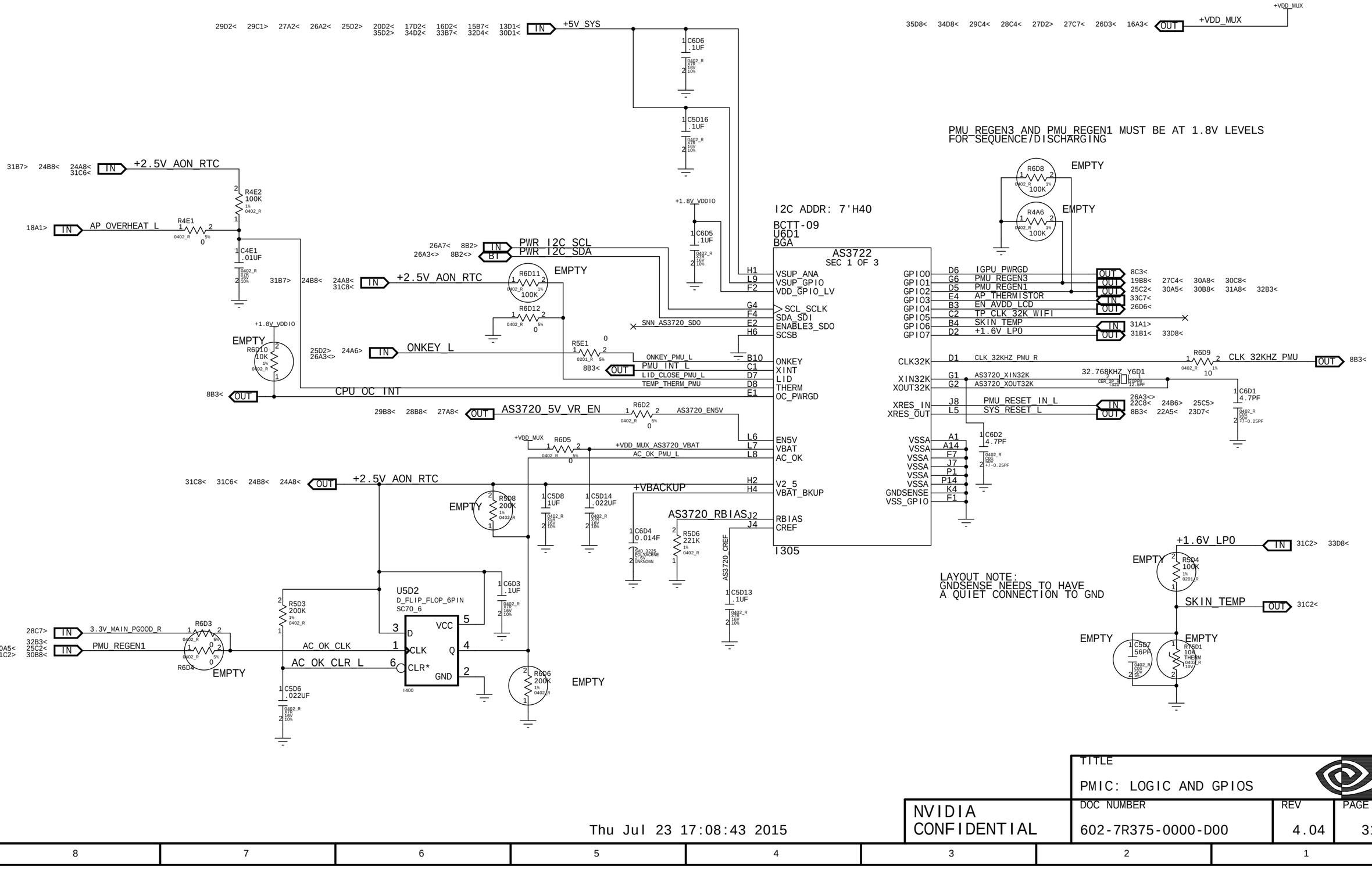
LAYOUT NOTE:
PLACE DCDC INPUT AND OUTPUT CAPS
SO THAT THEIR GNDS HAVE A COMMON SHAPE
WITH THE LS FET GND

Thu Jul 23 14:37:02 2015

TITLE			
+5V VR			
NVIDIA CONFIDENTIAL	DOC NUMBER	REV	PAGE
	602-7R375-0000-D00	4.04	29



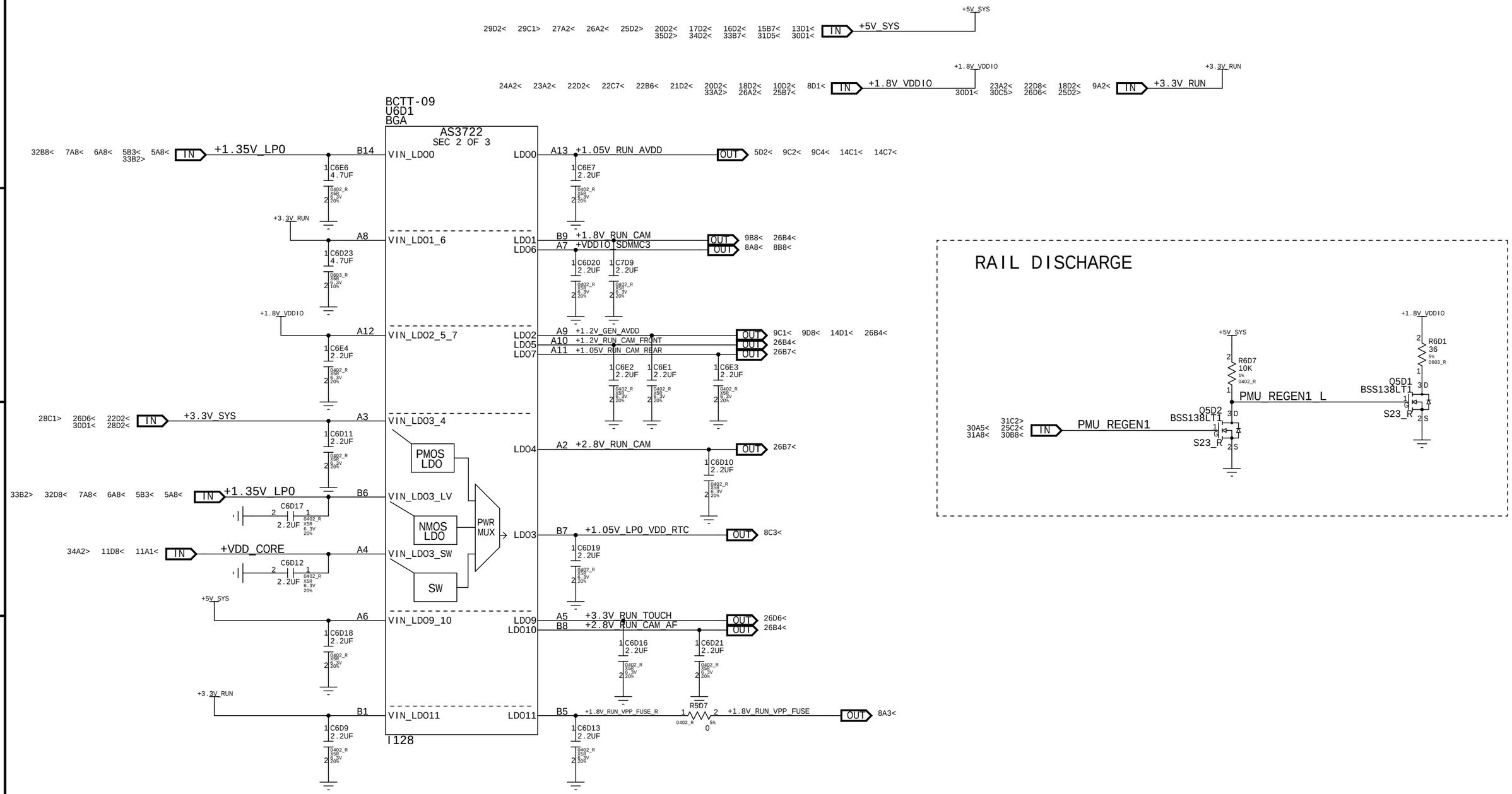
TITLE			
LOAD SWITCHES			
NVIDIA CONFIDENTIAL	DOC NUMBER 602-7R375-0000-D00	REV 4.04	PAGE 30



Thu Jul 23 17:08:43 2015

NVIDIA CONFIDENTIAL	DOC NUMBER: 602-7R375-0000-D00	REV: 4.04	PAGE: 31

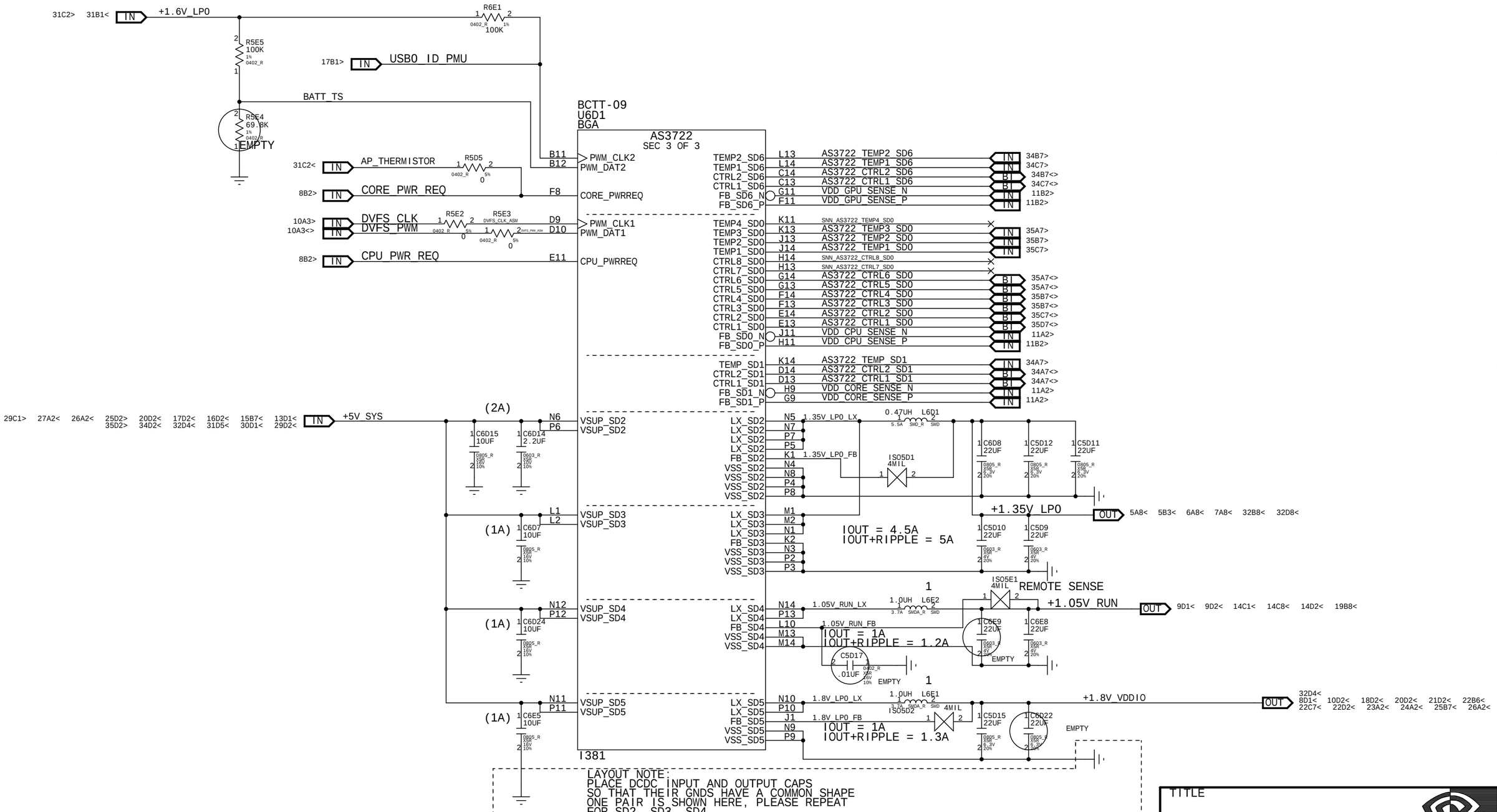
TITLE: PMIC: LOGIC AND GPIOS



Thu Jul 23 14:37:03 2015

NVIDIA CONFIDENTIAL	DOC NUMBER 602-7R375-0000-D00	REV 4.04	PAGE 32

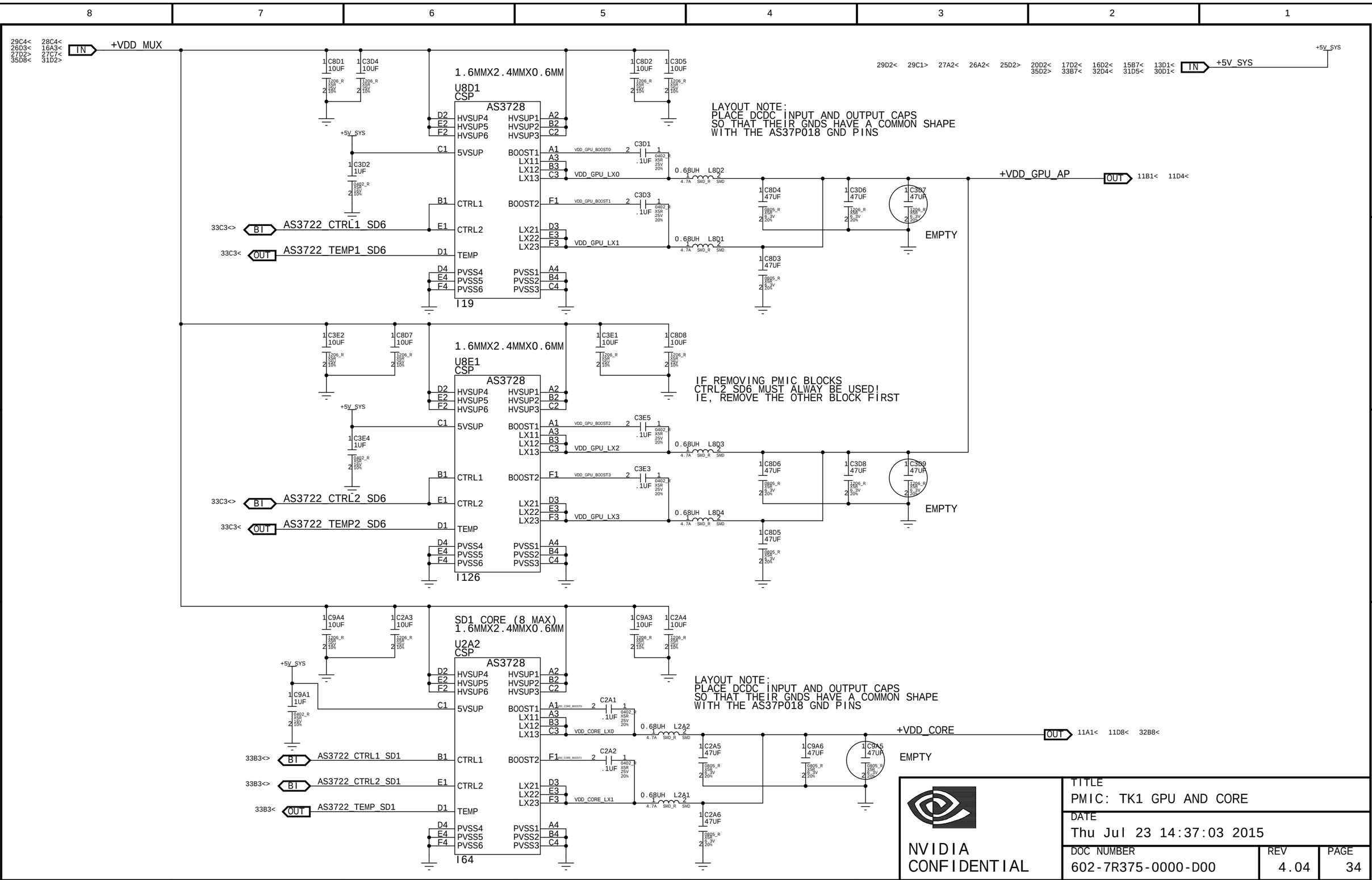
TITLE
PMIC: CNTL, INT SW, LDOS



Thu Jul 23 14:37:03 2015

NVIDIA CONFIDENTIAL	DOC NUMBER: 602-7R375-0000-D00	REV: 4.04	PAGE: 33

TITLE: PMIC: DCDC


+VDD_MUX
+5V_SYS
1.6MMX2.4MMX0.6MM
U8D1
CSP
AS3728
I19
LAYOUT NOTE:
PLACE DCDC INPUT AND OUTPUT CAPS
SO THAT THEIR GNDS HAVE A COMMON SHAPE
WITH THE AS37P018 GND PINS
+VDD_GPU_AP
EMPTY
AS3722_CTRL1_SD6
AS3722_TEMP1_SD6
1.6MMX2.4MMX0.6MM
U8E1
CSP
I126
IF REMOVING PMIC BLOCKS
CTRL2_SD6 MUST ALWAY BE USED!
IE, REMOVE THE OTHER BLOCK FIRST
AS3722_CTRL2_SD6
AS3722_TEMP2_SD6
SD1 CORE (8 MAX)
1.6MMX2.4MMX0.6MM
U2A2
CSP
I64
LAYOUT NOTE:
PLACE DCDC INPUT AND OUTPUT CAPS
SO THAT THEIR GNDS HAVE A COMMON SHAPE
WITH THE AS37P018 GND PINS
+VDD_CORE
EMPTY
AS3722_CTRL1_SD1
AS3722_CTRL2_SD1
AS3722_TEMP_SD1
NVIDIA
CONFIDENTIAL
TITLE
PMIC: TK1 GPU AND CORE
DATE
Thu Jul 23 14:37:03 2015
DOC NUMBER
602-7R375-0000-D00
REV
4.04
PAGE
34

27D2> 27C7< 26D3< 16A3<
34D8< 31D2> 29C4< 28C4<

IN +VDD_MUX

U7D2 CSP AS3728 I144

U7E1 CSP AS3728 I153

U7D3 CSP AS3728 I190

33C3<> BI AS3722_CTRL1_SDO
33C3<> BI AS3722_CTRL2_SDO
33C3< OUT AS3722_TEMP1_SDO
33C3<> BI AS3722_CTRL3_SDO
33C3<> BI AS3722_CTRL4_SDO
33C3< OUT AS3722_TEMP2_SDO
33C3<> BI AS3722_CTRL5_SDO
33C3<> BI AS3722_CTRL6_SDO
33C3< OUT AS3722_TEMP3_SDO

+5V_SYS

VDD_CPU_LX1 VDD_CPU_LX2 VDD_CPU_LX3 VDD_CPU_LX4 VDD_CPU_LX5 VDD_CPU_LX6

L7D2 L7D3 L7E1 L7E2 L7D4 L7D1 0.68UH 4.7A SMD_R SMD

EMPTY

LAYOUT NOTE:
PLACE DCDC INPUT AND OUTPUT CAPS
SO THAT THEIR GNDS HAVE A COMMON SHAPE
WITH THE AS3728 GND PINS

34D2< 26A2< 25D2> 20D2< 17D2< 16D2< 15B7< 13D1< OUT +5V_SYS +5V_SYS

+VDD_CPU_AP OUT 11B1< 11C8<

CAN EMPTY TWO PHASES FOR COST SAVINGS

NVIDIA CONFIDENTIAL

TITLE		
VDD_CPU VR		
DATE		
Thu Jul 23 17:11:40 2015		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.04	35

REVISION HISTORY

REVISION 1.00

BOM REVISION D

- RELEASED FAB A

REVISION 1.01

BOM REVISION E

- RELEASED FAB A
- UPDATE I2C MAP (P3)
- STUFF USB_VBUS_EN(0:1) PULLUPS (P17)
- STUFF USB0_VBUS RESISTOR TO 3.3V (P9)
- UPDATE EOL_HDMI CONN (P13)
- CHANGE R5C10 TO 5 MOHM FOR COST SAVINGS (P27)
- CHANGE R3E5 -> 100K OHM; SATA POWER DIVIDER (P16)
- CHANGE DFF CLEAR (P31)
- CHANGE PMIC TO OTP TYPE 9 (P31-33)
- EMPTY C4B2, EXCESS BYPASS FOR 3.3V SD CARD (P30)
- CHANGE SLEW RATE CAP C9D1 TO 3.3NF (P30)
- EMPTY 3.3V RESISTORS ON GEN2 I2C, STUFF 1.8V (P10)
- EMPTY R2D6 & R2D8, ADD R2D7 FOR LAN ISOLATEB (P19)
- BYPASS & EMPTY LOAD SWITCH U2C1 (P30)

REVISION 2.00

BOM REVISION B

- CHANGE RC ON DFF W/ CLOCK OPTIONS (P28,31)
- WIRE GPIO_PK2 TO EXPANSION HDR (P10, P26)
- WIRE +5V_SYS TO R2A5 (P25)
- RESIZE 0 OHM BYPASS RESISTORS TO 0402 (P30)
- CHANGE GEN2 I2C PULLUPS TO +3.3V_LP0 (P10)
- RESIZE FAN RESISTORS (P27)
- REWIRE ISOLATEB ON LAN (P19)
- DIRECT WIRE VDD_GPIO_LV TO +1.8V_VDDIO (P31)
- REPLACE POWER FETS ON 3.3V SWITCHER (P28)
- REPLACE SD_CARD_SWITCH (P30)
- EMPTY USB ESD PROTECTION (P17)
- EMPTY SD ESD PROTECTION (P25)
- ADD BLEED RESISTORS ON DC INPUT (P27)
- SIMPLIFY FEEDBACK, DROP BLEED RESISTORS (P11)
- TUNE +5V_SYS & +3V3_SYS FOR 3.3UH INDUCTORS (P27-29)
- ADD DEBUG CONNECTOR (P22)
- ADD TEMP SENSOR BUFFERING OPTIONS (P18)
- RELEASED FAB B

REVISION 3.00

BOM REVISION A

- MODIFY EXPANSION HEADER (P11,P26)
- STUFF FRONT PANEL HEADER (P25)
- CHANGE AUDIO HEADER TO LIME/PINK (P21)
- RELEASED FAB C

REVISION 4.00

- REWIRE ONKEY TO KB_COL0 FET (P24)
- REMOVE LED DIODE (P25)
- UART4 INPUTS STUFFING OPTIONS (P24)
- ADD EMI CAP (P21)
- ADD EMI CAP ON VDD MUX (P29)
- REPLACE EOL SNUBBERS (P24)
- ADD PMU_REGEN3 OPTION FOR LAN (P21)
- RELEASED FAB D

REVISION 4.01

- COSMETIC COMMENT CLEANUP (MULTIPLE PAGES)
- REPLACE Q4E2 (P24)
- RELEASE BOM B FAB D

REVISION 4.02

- ADJUST SEQUENCE ON SD5 (P2)
- ADD FRONT PANEL NOTE - YELLOW STDBY LED (P25)
- REPLACE Q9A1, Q9A2 - AVAILABILITY (P9)
- REPLACE J1A1 - AVAILABILITY (P25)
- RELEASE BOM E FAB D

REVISION 4.03

- ADDED NOTE OF DDR3L PIN MUXING TABLES (P4,5)
  THAT KB_ROW16 IS NOT A TRUE PWM (P4, 5, 8, AND 27)
  UPDATE TK1 SYMBOL

REVISION 4.04

- UPDATE TK1 SYMBOL AVDD_OSC,VDDIO_SYS,VDDIO_BB,VDDIO_SDMMC1&4,VDDIO_AUDIO,VDDIO_UART,VDDIO_CAM AND VDDIO_GMI TO SUPPORT 1.8V ONLY,VDDIO_DDR 1.35V SUPPORT ONLY

Thu Jul 23 14:37:04 2015

NVIDIA CONFIDENTIAL

TITLE			
REVISION HISTORY			
DOC NUMBER	REV	PAGE	
602-7R375-0000-D00	4.04	36	

Title: Basenet Report
Design: beaver_t124_fabd
Date: Jul 23 17:18:06 2015

Base nets and synonyms for beaver_t124_lib.BEAVER_T124_FABD(@beaver_t124_lib.beaver_t124_fabd(sch_1))

Base Signal	Location([Zone][dir])
+1.2V_GEN_AVDD	9C1< 9D8< 14D1< 26B4< 32C4>
+1.2V_RUN_CAM_FRONT	26B4< 32C4>
+1.05V_LAN_REGOUT	19B3
+1.05V_LAN_REGOUT_L	19C4
+1.05V_LP0_VDD_RTC	8C3< 32B5>
+1.05V_RUN	9D1< 9D2< 14C1< 14C8< 14D2< 19B8< 33A2>
+1.05V_RUN_AVDD	5D2< 9C2< 9C4< 14C1< 14C7< 32D5>
+1.05V_RUN_AVDD_HDMI_PLL_AP	9C3
+1.05V_RUN_AVDD_HDMI_PLL_AP_GATE	9D5
+1.05V_RUN_AVDD_PEX_PLL_AP_F	14C3
+1.05V_RUN_AVDD_SATA_PLL_F	14C7
+1.05V_RUN_CAM_REAR	26B7< 32C4>
+1.6V_LP0	31B1< 31C2> 33D8<
+1.8V_LP0_AVDD_OSC_AP_F	8A4
+1.8V_RUN_AVDD_PLL_UTMIP_AP_F	9A5
+1.8V_RUN_CAM	9B8< 26B4< 32C5>
+1.8V_RUN_VPP_FUSE	8A3< 32A4>
+1.8V_RUN_VPP_FUSE_R	32A5
+1.8V_VDDIO	8D1< 10D2< 18D2< 20D2< 21D2< 22B6< 22C7< 22D2< 23A2< 24A2< 25B7< 26A2< 32D4< 33A2>
+1.8V_VDDIO_LP0_OFF	9A2< 30A6>
+1.35V_LP0	5A8< 5B3< 6A8< 7A8< 32B8< 32D8< 33B2>
+1.35V_LP0_VDDIO_DDR_MCLK_AP	5B3
+2.5V_AON_RTC	24A8< 24B8< 31B7> 31C6< 31C8<
+2.8V_RUN_CAM	26B7< 32B4>
+2.8V_RUN_CAM_AF	26B4< 32A5>
+2V_STBY	27C4> 28B7< 29B7<
+3.3V_342	22D7
+3.3V_AON	27A8< 27B4> 27B8< 28C8<
+3.3V_AVDD_HDMI_AP_GATED	9D5
+3.3V_LP0	9A3 10B2 10D3 13B5 13C5 13C5 14A2 14D2 14D6 17B7 17D7 18C6 19A2 19D6 9A2< 10D2< 13D1< 14D1< 15D1< 17D2< 18D2< 19D2< 22D2< 30A3> 9A3 10B2 10D3 13B5 13C5 13C5 14A2
	14D2 14D6 17B7 17D7 18C6 19A2 19D6 9A2< 10D2< 13D1< 14D1< 15D1< 17D2< 18D2< 19D2< 22D2< 30A3>
+3.3V_LP0	9A3 10B2 10D3 13B5 13C5 13C5 14A2 14D2 14D6 17B7 17D7 18C6 19A2 19D6 9A2< 10D2< 13D1< 14D1< 15D1< 17D2< 18D2< 19D2< 22D2< 30A3>
+3.3V_RUN	9A2< 18D2< 22D8< 23A2< 25D2> 26D6< 30C5> 30D1< 32D3< 9B3 9D2 18B4 23D4 25D4 30D5 32A7 32C7
	9A2< 18D2< 22D8< 23A2< 25D2> 26D6< 30C5> 30D1< 32D3< 9B3 9D2 18B4 23D4 25D4 30D5 32A7 32C7
+3.3V_RUN	9A2< 18D2< 22D8< 23A2< 25D2> 26D6< 30C5> 30D1< 32D3< 9B3 9D2 18B4 23D4 25D4 30D5 32A7 32C7
	9A2< 18D2< 22D8< 23A2< 25D2> 26D6< 30C5> 30D1< 32D3< 9B3 9D2 18B4 23D4 25D4 30D5 32A7 32C7
+3.3V_RUN_TOUCH	26D6< 32B5>
+3.3V_SD_CARD	25B7< 30B1>
+3.3V_SYS	22D2< 26D6< 28C1> 28D2< 30D1< 32B8<
+5V_HDMI	13A5
+5V_HDMI_CON	13A4
+5V_SATA	16C2
+5V_STBY	27A7< 27B4> 28C8<
+5V_SYS	13D1< 15B7< 16D2< 17D2< 20D2< 25D2> 26A2< 27A2< 29C1> 29D2< 30D1< 31D5< 32D4< 33B7< 34D2< 35D2>
+5V_USB_HS	17B5
+12V_SATA	16B2
+AVDD_LVDS0_PLL_AP_F	9B4
+EMMC_VDDI	23C4
+USB0_VBUS_SW	17C4
+VBACKUP	31B5
+VCAP_SLUGO3	30A5
+VDDIO_SDMMC3	8A8< 8B8< 32C5>
+VDD_1V5_MPCIE	15B4
+VDD_ACIN	27D5
+VDD_CORE	11A1< 11D8< 32B8< 34A2>
+VDD_CPU_AP	11B1< 11C8< 35C2>
+VDD_GPU_AP	11B1< 11D4< 34D2>
+VDD_MIC	20B4
+VDD_MUX	31B5 16A3< 26D3< 27C7< 27D2> 28C4< 29C4< 31D2> 34D8< 35D8<
	31B5 16A3< 26D3< 27C7< 27D2> 28C4< 29C4< 31D2> 34D8< 35D8<
+VDD_MUX	31B5 16A3< 26D3< 27C7< 27D2> 28C4< 29C4< 31D2> 34D8< 35D8<
	31B5 16A3< 26D3< 27C7< 27D2> 28C4< 29C4< 31D2> 34D8< 35D8<
+VDD_MUX_AS3720_VBAT	31B5
1.05V_RUN_AVDD_HDMI_PLL_AP_EN_L	9C3
1.05V_RUN_FB	33A4
1.05V_RUN_LX	33A4
1.8V_LP0_FB	33A4
1.8V_LP0_LX	33A4
1.35V_LP0_FB	33B4
1.35V_LP0_LX	33B4
1P5V_EN	15B5
3.3V_LP0_CAP	30B7
3.3V_MAIN_COMP	28A7
3.3V_MAIN_COMP_RC	28B7
3.3V_MAIN_CS_N	28B5
3.3V_MAIN_CS_P	28B5
3.3V_MAIN_DRVH	28C5
3.3V_MAIN_DRVH_R	28C5
3.3V_MAIN_DRVL	28C5
3.3V_MAIN_ISO	28B2
3.3V_MAIN_PGOOD_R	28C7> 31A8<
3.3V_MAIN_RST	28B7
3.3V_MAIN_SNUB	28C4
3.3V_MAIN_SW	28C5
3.3V_MAIN_VBST	28C5
3.3V_MAIN_VBST_RC	28C5
3.3V_MAIN_VFB	28B5
3.3V_RUN_AVDD_HDMI_AP_EN_L	9D3
5V_MAIN_COMP	29A7
5V_MAIN_COMP_RC	29A7
5V_MAIN_CS_N	29B5
5V_MAIN_CS_P	29B5
5V_MAIN_DRVH	29C5
5V_MAIN_DRVH_R	29C5
5V_MAIN_DRVL	29B5
5V_MAIN_ISO	29B2
5V_MAIN_PGOOD_R	29C7
5V_MAIN_RST	29B7
5V_MAIN_SNUB	29B4
5V_MAIN_SW	29C5
5V_MAIN_VBST	29B5
5V_MAIN_VBST_RC	29B5
5V_MAIN_VFB	29A5
AC_OK_AP_L	10B4
AC_OK_CLK	31A7
AC_OK_CLR_L	31A7
AC_OK_PMU_L	31B5
AP_FORCE_RECOVERY_L	10C3< 24D5>
AP_OVERHEAT_L	18A1> 31C8<

<->

TITLE
?

NVIDIA CONFIDENTIAL

DOC NUMBER 602-7R375-0000-D00 | REV 4.04 | PAGE 37

AP_OVERHEAT_R_L	18A3
AP_OVRHT_G	18A3
AP_THERMISTOR	31C2< 33C7<
AS3720_5V_VR_EN	27A8< 28B8< 29B8< 31B6>
AS3720_CREF	31A4
AS3720_EN5V	31B5
AS3720_RBIAS	31B5
AS3720_XIN32K	31B3
AS3720_XOUT32K	31B3
AS3722_CTRL1_SD0	33C3<> 35D7<>
AS3722_CTRL1_SD1	33B3<> 34A7<>
AS3722_CTRL1_SD6	33C3<> 34C7<>
AS3722_CTRL2_SD0	33C3<> 35C7<>
AS3722_CTRL2_SD1	33B3<> 34A7<>
AS3722_CTRL2_SD6	33C3<> 34B7<>
AS3722_CTRL3_SD0	33C3<> 35B7<>
AS3722_CTRL4_SD0	33C3<> 35B7<>
AS3722_CTRL5_SD0	33C3<> 35A7<>
AS3722_CTRL6_SD0	33C3<> 35A7<>
AS3722_TEMP1_SD0	33C3< 35C7>
AS3722_TEMP1_SD6	33C3< 34C7>
AS3722_TEMP2_SD0	33C3< 35B7>
AS3722_TEMP2_SD6	33C3< 34B7>
AS3722_TEMP3_SD0	33C3< 35A7>
AS3722_TEMP_SD1	33B3< 34A7>
AUD1_VREF1	20B4
AUD1_VREF2	20B4
AUDIO_AVDD	20B4
AUDIO_DACREF	20B4
AUDIO_GND	20A1 20A1 20A2 20A2 20A3 20A3 20A3 20A3 20A6 20B2 20B2 20B2 20B3 20B3 20C3 20C3 21A4 21A5 21A5 21A5 21B4 21B5 21C4
AUDIO_LDO_EN	8C3> 20B7<
AUD_DCVDD	20A4
BATT_TS	33D7
BCLK2	20B6
BD_ID_STRAP0	8D3< 24A3>
BD_ID_STRAP1	8C3< 24A3>
BD_ID_STRAP2	10A3< 24A3>
BD_ID_STRAP3	10A3< 24A3>
BOARD_ID_A0	18D5
BOARD_ID_A1	18D5
BOARD_ID_A2	18D5
BOARD_ID_WP	18D5
BR_UART1_RXD	8C3< 22C7<> 26B7>
BR_UART1_TXD	8C3> 22C7<> 26B4<
C1N	18C4
C1P	18C4
C2N	18C4
C2P	18C4
CAM1_AF_PWDN	9A7> 26A7<
CAM1_GPIO	9B7<> 26A7<>
CAM1_MCLK	9A7> 26A7<
CAM1_PWDN	9A7> 26A7<

CAM2_GPIO	9B7<> 26B3<>
CAM2_MCLK	9B7> 26B4<
CAM2_PWDN	9A7> 26B7<
CAM_FLASH	9A7> 26A7<
CAM_I2C_SCL	9A8> 26B4<
CAM_I2C_SDA	9A8<> 26B7<>
CAM_RST_L	9B7> 26B4<
CAP_SLG_5V_SAT	16B3
CHGPUMP_N1	20B4
CHGPUMP_N2	20B4
CHGPUMP_P1	20B4
CHGPUMP_P2	20B4
CLK3_OUT	10C7> 26A4<
CLK3_OUT_R	10C6
CLK_32KHZ_PMU	8B3< 31B1>
CLK_32KHZ_PMU_R	31B3
CODEC_IRQ_L	10C3< 20B7>
CORE_PWR_REQ	8B2> 33C7<
CPU_OC_INT	8B3< 31B7>
CPU_PWR_REQ	8B2> 33C7<
CPVDD	20B4
CPVEE	20B4
CPVPP	20B4
CSI_A_CLK_N	9D8> 26B7<
CSI_A_CLK_P	9C8> 26B7<
CSI_A_D0_N	9D8< 26B7>
CSI_A_D0_P	9D8< 26B7>
CSI_A_D1_N	9D8< 26B7>
CSI_A_D1_P	9D8< 26B7>
CSI_B_D0_N	9C8< 26A7>
CSI_B_D0_P	9C8< 26B7>
CSI_B_D1_N	9C8< 26B7>
CSI_B_D1_P	9C8< 26B7>
CSI_E_CLK_N	9C8> 26B4<
CSI_E_CLK_P	9C8> 26B4<
CSI_E_D0_N	9C8< 26B4>
CSI_E_D0_P	9C8< 26B7>
DACDAT2	20C6
DAP2_DIN	10B7< 20C8>
DAP2_DIN_R	20C7
DAP2_DOUT	10B7> 20C8<
DAP2_FS	10A7> 20C8<>
DAP2_SCLK	10A8> 20C8<>
DAP2_SCLK_R	10A6
DAP_MCLK1	10B8> 20B7<
DAP_MCLK1_R	10B6
DDR0_CKE0	4B4> 6C4< 6C8<
DDR0_CKE1	4B4> 6C4< 6C8<
DDR0_CLKN	4D1> 6C4< 6C8<
DDR0_CLKP	4D1> 6C4< 6C8<
DDR0_CLK_TERM	4C3
DDR0_CS0_L	4B4> 6B4< 6B8<
DDR0_CS1_L	4B4> 6B4< 6B8<
DDR0_ODT0	4A4> 6B4< 6B8<
DDR0_ODT1	4A4> 6B4< 6B8<

DDR1_CKE0	4A4> 7C4< 7C8<
DDR1_CKE1	4A4> 7C4< 7C8<
DDR1_CLKN	4C1> 7C4< 7C8<
DDR1_CLKP	4C1> 7C4< 7C8<
DDR1_CLK_TERM	4C2
DDR1_CS0_L	4B4> 7B4< 7B8<
DDR1_CS1_L	4A4> 7B4< 7B8<
DDR1_ODT0	4A4> 7B4< 7B8<
DDR1_ODT1	4B4> 7B4< 7B8<
DDR_A0<5..3>	4B3> 4C3> 6D4< 6D8<
DDR_A1<5..3>	4B3> 7D4< 7D8<
DDR_A<15..0>	4C3> 6B4< 6B8< 6D4< 6D8< 7B4< 7B8< 7D4< 7D8<
DDR_BA<2..0>	4C3> 6C4< 6C8< 7C4< 7C8<
DDR_CAS_L	4B3> 6C4< 6C8< 7C4< 7C8<
DDR_COMP_PD	5A6
DDR_COMP_PU	5A6
DDR_DM0	4B7> 6C8<
DDR_DM1	4A7> 6C4<
DDR_DM2	4B7> 6C8<
DDR_DM3	4A7> 6C4<
DDR_DM4	5A7> 7C8<
DDR_DM5	5A7> 7C4<
DDR_DM6	5A7> 7C8<
DDR_DM7	5A7> 7C4<
DDR_DQ<63..0>	4D8<> 5C7<> 6D1<> 6D4<> 7D1<> 7D5<>
DDR_DQS0N	4B7<> 6C8<
DDR_DQS0P	4B7<> 6C8<
DDR_DQS1N	4A7<> 6C4<
DDR_DQS1P	4A7<> 6C4<
DDR_DQS2N	4B7<> 6C8<
DDR_DQS2P	4B7<> 6C8<
DDR_DQS3N	4B7<> 6C4<
DDR_DQS3P	4B7<> 6C4<
DDR_DQS4N	5A7<> 7C8<
DDR_DQS4P	5A7<> 7C8<
DDR_DQS5N	5A7<> 7C4<
DDR_DQS5P	5A7<> 7C4<
DDR_DQS6N	5B7<> 7C8<
DDR_DQS6P	5B7<> 7C8<
DDR_DQS7N	5A7<> 7C4<
DDR_DQS7P	5A7<> 7C4<
DDR_RAS_L	4C3> 6C4< 6C8< 7C4< 7C8<
DDR_RESET_L	4B3> 6B4< 6B8< 7B4< 7B8<
DDR_WE_L	4C3> 6C4< 6C8< 7C4< 7C8<
DDR_ZQ0_U27U1	6B7
DDR_ZQ0_U27U2	6B3
DDR_ZQ0_U28U1	7B7
DDR_ZQ0_U28U2	7B3

<->

TITLE

?

NVIDIA CONFIDENTIAL

DOC NUMBER 602-7R375-0000-D00

REV 4.04

PAGE 38

```
DDR_ZQ1_U27U1       6B7
DDR_ZQ1_U27U2       6B3
DDR_ZQ1_U28U1       7B7
DDR_ZQ1_U28U2       7B3
DEBUGGER_RESET_L    22C7
DP_AUX_N            9B3<> 26D6<>
DP_AUX_P            9B3<> 26D6<>
DSI_CSI_RDN         9B7
DSI_CSI_RUP         9B7
DSR                 18C2
DTR                 18B2
DVFS_CLK            10A3> 33C7<
DVFS_CLK_ASM        33C6
DVFS_PWM            10A3<> 33C7<
DVFS_PWM_ASM        33C6
EDP_HPD             9B2< 26C6>
EN_AVDD_HDMI        9D2
EN_AVDD_HDMI_PLL    9C3
EN_AVDD_LCD         26D6< 31C2>
EN_RUN_VREG         30C7
EN_VDD_12V_DRAIN    16A2
EN_VDD_12V_GATE     16A3
EN_VDD_BL           8C7> 26D3<
EN_VDD_HDMI         9C1< 9D1< 10A7<> 13A8<
EN_VDD_SD           8C3> 30B4<
FAN_EN_DR           27C3
FAN_EN_GATE         27C3
FAN_EN_L            27D3
FAN_PWM             8C3> 27C4<
FB_1PV5             15B5
FORCE_RECOVERY_L    22C7< 24D5<> 26A3<>
FP_9                25D5
GEN1_I2C_SCL        10B8> 18A6< 18D3< 20B7< 22C4< 26A7<
                    26D3<
GEN1_I2C_SCL_3.3V   15C3< 22C1>
GEN1_I2C_SDA        10B8<> 18A6<> 18D3<> 20B7<> 22C4<>
                    26A3<> 26D3<>
GEN1_I2C_SDA_3.3V   15C3<> 22C1<>
GEN2_I2C_SCL_3.3V   10B1> 26D6<
GEN2_I2C_SDA_3.3V   10B1<> 26D6<>
GND                 4C2 4C3 5A6 5B4 5B4 5C4 5C4 5D4 6A2
                    6A3 6A6 6A7 6A7 6A7 6A8 6A8 6B4 6B4
                    6B5 6B8 6B8 7A2 7A3 7A6 7A7 7A7 7A7
                    7A8 7A8 7B4 7B4 7B6 7B8 7B8 8A3 8A3
                    8A4 8A4 8A4 8A4 8A6 8A7 8A7 8A7 8B3
                    8B7 8B7 8B7 8C4 8C6 8C7 8D3 8D3 8D4
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                    10B6 10B7 10D3 10D3 10D3 10D3 10D6
                    10D7 11A4 11A4 11A8 11A8 11B4 11B8
                    11B8 11C4 11C4 11C8 11D8 12A3 12A4
                    12A6 12A6 12A6 12A7 12B6 12B6 12B6
                    12B7 13A4 13A4 13A5 13A7 13A7 13B4
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```
13B4 13C3 13C4 13C5 13C6 13C7 13D4
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14C6 14C7 14D2 14D3 14D6 14D6 14D7
15B4 15B4 15B4 15B5 15B5 15B5 15B6
15B6 15C2 15C2 15C3 15C4 16A2 16A2
16A3 16B1 16B2 16B2 16B2 16B3 16B4
16C1 16C3 17A1 17A2 17A4 17A4 17A5
17A6 17B2 17B2 17B3 17B3 17B5 17B5
17B5 17B5 17B6 17B6 17B7 17B8 17C1
17C3 17C5 17C6 17C6 17C6 17C7 17D3
17D6 18A2 18A3 18A4 18A4 18B2 18B3
18B4 18B5 18B6 18B6 18B7 18C3 18C4
18C5 18C5 18C5 18C7 18D3 19A1 19A2
19A2 19A3 19A5 19A6 19A6 19B3 19B3
19B4 19B4 19B4 19B4 19B4 19B4 19B6
19B6 19C3 19C4 19C4 19C4 19C4 19C4
20A4 20A4 20A4 20A4 20A4 20A4 20A5
20A6 20B7 20B7 20B7 21A3 21A6 21B5
22A1 22A1 22A2 22A2 22A2 22A3 22A3
22A4 22A5 22B5 22B6 22B7 22C2 22C3
22C3 22C6 22C6 22D7 23A5 23B4 23C4
23C4 23C4 23C4 23D4 23D4 24A4 24A4
24A4 24A4 24A6 24A6 24A7 24A8 24A8
24B4 24B7 24B7 24B8 24C4 24C7 24C7
24C8 25A4 25A4 25A4 25A5 25A6 25C3
25C4 25C5 25D5 25D6 26A5 26A5 26C5
26C5 26C5 26C5 27A4 27A5 27A6 27B5
27C2 27C3 27C5 27C6 27D3 27D3 27D3
27D4 27D4 27D6 28B4 28B4 28B7 28C2
28C2 29B2 29B4 29B4 29C3 30A4 30A4
30A5 30A7 30A8 30B2 30B2 30B4 30B6
30B6 30B7 30C5 31A2 31A4 31A5 31A5
31A5 31A6 31A6 31A7 31B1 31B3 31B3
31B5 31B5 31C3 31C4 31C4 31C5 31C6
31C7 31D5 32A5 32A5 32A6 32A7 32A7
32B1 32B2 32B5 32B5 32B5 32B5 32B6
32B7 32B7 32B7 32C5 32C6 32C6 32C7
32C7 32C7 33A3 33A3 33A4 33A6 33A6
33B3 33B3 33B6 33B6 33B6 33C7 34A3
34A4 34A5 34A5 34A6 34A7 34A7 34B3
34B4 34B5 34B6 34B6 34C3 34C4 34C5
34C5 34C6 34C7 34D5 34D6 34D7 35A4
35A5 35A5 35A6 35A7 35A7 35B2 35B4
35B5 35B6 35B7 35C4 35C5 35C5 35C6
35C7 35D5 35D7 35D7
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```
GPIO_PG3            10C3<> 24D1>
GPIO_PH7            9C1< 10C3<>
GPIO_PI0            10C3> 24C5>
GPIO_PK2            10B3> 26D3<
GPIO_PU0            10C6<> 26B3<>
GPIO_PU1            10C6<> 26B3<>
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GPIO_PU3            10B6<> 26A3<>
GPIO_PU4            10B6<> 26A3<>
GPIO_PU5            10B6<> 26A3<>
GPIO_PU6            10B6<> 26A3<>
GPIO_PV0            8C7
GPIO_PV1            8C7
GRN_PWRLED          25D4
HDLED_L             25D5
HDLED_PWR           25D5
HDMI_CEC            9C4<> 13C7<>
HDMI_CEC_A_PU       13B5
HDMI_CEC_CON        13C4
HDMI_CEC_L          13C5
HDMI_DDC_SCL        9C4> 13B7<
HDMI_DDC_SCL_CON    13B5
HDMI_DDC_SDA        9C4<> 13B7<>
HDMI_DDC_SDA_CON    13B5
HDMI_FAULT_L        13A6
HDMI_HPD            13D4
HDMI_ILIM           13A6
HDMI_INT            9C4< 13D5>
HDMI_RSET           9C5
HDMI_TXC_N          9C4> 13C8<
HDMI_TXC_P          9C4> 13C8<
HDMI_TXD_N<2..0>    9C3> 13D8<
HDMI_TXD_P<2..0>    9C3> 13D8<
HEADSET1RC_L        20C3
HEADSET1RC_R        20C3
HEADSET1R_L         20C4
HEADSET1R_R         20C4
HEADSET_MIC_C       20B7< 21C8>
HEAD_DET_JACK_L     21B4
HEAD_DET_L          20B7< 21B7>
HEAD_DET_T124_L     8C3< 21B7>
HP1_LT              20C2> 21A7<
HP1_LT_L            21A5
HP1_MIC_L           21C6
HP1_MIC_R           21C5
HP1_RT              20C2> 21A7<
HP1_RT_L            21A5
HP1_SENSE           20C4< 21A7>
HSIC1_DATA          9A8> 26B3<>
HSIC1_DATA_R        9A7
HSIC1_STROBE        9A8> 26B4<
HSIC1_STROBE_R      9A7
HSIC_REXT           9A7
IGPU_PWRGD          8C3< 31C2>
JD_MIC_L            20A7< 21C7>
JD_MIC_R_L          21C4
JD_MIC_T124_L       8D3< 21C7>
JTAG_PD0            22A2
```

<->

TITLE

?

NVIDIA CONFIDENTIAL

DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.04	39

JTAG_PD1	22A2
JTAG_RTCK	8A3< 22A4< 22C7>
JTAG_SRST_B_L	22A2
JTAG_SRST_L	22A4
JTAG_TCK	8A3< 22A4> 22C7>
JTAG_TDI	8A3< 22A4> 22C7>
JTAG_TDO	8A3> 22A4< 22C7<
JTAG_TMS	8A3< 22A4> 22C7>
JTAG_TRST_L	8A3< 22C7<
KB_COL0_AP	8D3< 24A5>
KB_COL0_GATE	24A6
LAN_CH_GND	19A1
LAN_ISOLATE	19B7
LAN_ISOLATE_L	19B6
LAN_ISO_BASE	19B7
LAN_LED0	19A4
LAN_LED0_ACT_L	19A3
LAN_LED1	19A4
LAN_LED2	19A4
LAN_LED_100	19A3
LAN_LED_1000	19A3
LAN_MDI0_N	19B4
LAN_MDI0_P	19B4
LAN_MDI1_N	19A4
LAN_MDI1_P	19A4
LAN_MDI2_N	19A4
LAN_MDI2_P	19A4
LAN_MDI3_N	19A4
LAN_MDI3_P	19A4
LAN_RSET	19A4
LAN_TRCT1	19B1
LCD_BL_EN	10C3> 26C6<
LCD_BL_PWM	10C3> 26C6<
LCD_LR	10C3> 24D1>
LCD_TE	8C3> 26C3<
LCD_UD	10C3> 24D1>
LED_5V_RUN	30D5
LID_CLOSED_L	8C4
LID_CLOSE_PMU_L	31B5
LRCK2	20B6
LVDS_RSET	9B5
LVDS_TXD0_N	9B3> 26C3<
LVDS_TXD0_P	9B3> 26D3<
LVDS_TXD1_N	9B3> 26C6<
LVDS_TXD1_P	9B3> 26C6<
LVDS_TXD2_N	9B3> 26C6<
LVDS_TXD2_P	9B3> 26C6<
LVDS_TXD3_N	9B3> 26C3<
LVDS_TXD3_P	9B3> 26C3<
LVDS_TXD4_N	9B3> 26C3<
LVDS_TXD4_P	9B3> 26C3<
LV_SATA_EN	16B3
MIC1_BIAS	20B2> 21C5<
MIC1_BIAS_R	20B4
MODEM_SAR0	10C3<> 24D1>

ONKEY_L	24A6> 25D2> 26A3<> 31C6<
ONKEY_PMU_L	31B5
PCA9306_VREF21	22C2
PEX0_WAKE_R_L	19B6
PEX_CLK1_N	14B3> 15D7<
PEX_CLK1_P	14B3> 15D7<
PEX_CLK2_N	14A3> 19C7<
PEX_CLK2_P	14B3> 19C7<
PEX_GIGE_PRSNT_L	8D7
PEX_L0_CLKREQ_L	14A2< 15D7>
PEX_L0_RST_L	14A3> 15C3<
PEX_L1_CLKREQ_L	14A2< 19C7>
PEX_L1_RST_L	14A3> 19C7<
PEX_MINI_PRSNT_L	8D7
PEX_RX2_C_N	16A4< 19C7>
PEX_RX2_C_P	16A4< 19C7>
PEX_RX2_N	14B3< 16A8>
PEX_RX2_P	14B3< 16A8>
PEX_RX4_N	14B3< 15C7>
PEX_RX4_P	14B3< 15C7>
PEX_RX20_N	16A7
PEX_RX20_P	16A7
PEX_TERMP	14A3
PEX_TX2_C_N	14B3> 16B8<
PEX_TX2_C_P	14B3> 16B8<
PEX_TX2_N	16B4> 19C7<
PEX_TX2_P	16B4> 19C7<
PEX_TX4_N	14B3> 15C7<
PEX_TX4_P	14B3> 15C7<
PEX_TX20_C_N	16B7
PEX_TX20_C_P	16B7
PEX_WAKE_L	14A3< 15D7> 19B7>
PE_TX4_C_N	15C6
PE_TX4_C_P	15C6
PFO_JTAG_TRST_L	22A6
PMU_INT_L	8B3< 31B5>
PMU_REGEN1	25C2< 30A5< 30B8< 31A8< 31C2> 32B3<
PMU_REGEN1_L	32B2
PMU_REGEN3	19B8< 27C4< 30A8< 30C8< 31C2>
PMU_RESET_IN_L	22C8< 24B6> 25C5> 26A3<> 31B2<
POWER_FAN	27C2
POWER_FAN_SRC	27D2
PWRBTN_R_L	25D4
PWR_I2C_SCL	8B2> 26A7< 31C6<
PWR_I2C_SDA	8B2<> 26A3<> 31C6<>
RS232_CTS	18B3
RS232_RTS	18C3
RS232_RXD_L	18B3
RS232_TXD_L	18C3
RST_SWR_L	25D6
SATA_L0_RX_N	14C7< 16D3<
SATA_L0_RX_P	14C7< 16C3<
SATA_L0_TX_N	14C7> 16D3<
SATA_L0_TX_P	14C7> 16D3<
SATA_LED	10B7> 25D7<

SATA_PWR_EN	16A3
SATA_PWR_EN_T124	10B7> 16A5<
SATA_RX_N	16D2
SATA_RX_P	16C2
SATA_TERMP	14C6
SATA_TESTCLKN	14C7
SATA_TESTCLKP	14C7
SATA_TX_N	16D2
SATA_TX_P	16D2
SDMMC1_COMP_PD	8B6
SDMMC1_COMP_PU	8B6
SDMMC2_COMP_PD	10B4
SDMMC2_COMP_PU	10B4
SDMMC3_CD_L	8A8< 25A7>
SDMMC3_CLK	8B8> 25B7<
SDMMC3_CLK_LB_IN	8A7
SDMMC3_CLK_LB_OUT	8A7
SDMMC3_CMD	8B8> 25B7<>
SDMMC3_COMP_PD	8A6
SDMMC3_COMP_PU	8A6
SDMMC3_DAT<3..0>	8B8<> 25B7<>
SDMMC3_WP_L	8D3< 25A7>
SDMMC4_CLK	8A7> 23D7<
SDMMC4_CMD	8A7> 23D7<>
SDMMC4_COMP_PD	8A6
SDMMC4_COMP_PU	8A6
SDMMC4_DAT<7..0>	8A8<> 23C7<>
SKIN_TEMP	31A1> 31C2<
SNN_1P5V_POK	15B4
SNN_ADCDAT2	20C6
SNN_AS3720_SDO	31C5
SNN_AS3722_CTRL7_SD0	33C4
SNN_AS3722_CTRL8_SD0	33C4
SNN_AS3722_TEMP4_SD0	33C4
SNN_CAMERA_SHUTTER	8B7
SNN_CLK3_REQ	10C6
SNN_COMPASS_DRDY	10A4
SNN_DAP3_SCLK	8C7
SNN_DCD	18C2
SNN_DGPU_3P3_EN	8C7
SNN_DGPU_PWRGD	8C4
SNN_DGPU_VDD_EN	8C7
SNN_DIRECTDC_CLK	14B6
SNN_DIRECTDC_IN	14B6
SNN_DIRECTDC_OUT0	14B6
SNN_DIRECTDC_OUT1	14B6
SNN_DIRECTDC_OUT2	14B6
SNN_DIRECTDC_OUT3	14B6
SNN_DSI_A_CLK_N	9C7

<->

TITLE

?

NVIDIA CONFIDENTIAL

DOC NUMBER 602-7R375-0000-D00 | REV 4.04 | PAGE 40

SNN_DSI_A_CLK_P	9C7
SNN_DSI_A_D0_N	9C7
SNN_DSI_A_D0_P	9C7
SNN_DSI_A_D1_N	9C7
SNN_DSI_A_D1_P	9C7
SNN_DSI_A_D2_N	9C7
SNN_DSI_A_D2_P	9C7
SNN_DSI_A_D3_N	9C7
SNN_DSI_A_D3_P	9C7
SNN_DSI_B_CLK_N	9B7
SNN_DSI_B_CLK_P	9B7
SNN_DSI_B_D0_N	9B7
SNN_DSI_B_D0_P	9B7
SNN_DSI_B_D1_N	9B7
SNN_DSI_B_D1_P	9B7
SNN_DSI_B_D2_N	9B7
SNN_DSI_B_D2_P	9B7
SNN_DSI_B_D3_N	9B7
SNN_DSI_B_D3_P	9B7
SNN_EN_BAT_SMB	10A6
SNN_FAN_TACH	27C2
SNN_GPIO_PFF2	14A4
SNN_GPIO_PH3	10C4
SNN_GPIO_PI4	10B4
SNN_GPIO_PI5	10B4
SNN_GPIO_PI7	10B4
SNN_GPS_IRQ_L	10A4
SNN_GPU_PWR_REQ	8C4
SNN_HDMI_PROBE	9C5
SNN_HSIC2_DATA	9A7
SNN_HSIC2_STROBE	9A7
SNN_IN3N	20B4
SNN_IN3P	20B4
SNN_JACK_RING	27D6
SNN_KB_COL1	8D4
SNN_KB_COL2	8D4
SNN_KB_COL6	8D4
SNN_KB_COL7	8D4
SNN_KB_ROW8	8C4
SNN_KB_ROW11	8C4
SNN_KB_ROW12	8C4
SNN_LOUTL	20B6
SNN_LOUTR	20B6
SNN_LVDS0_PROBE	9B5
SNN_MPCIE_3	15D6
SNN_MPCIE_5	15D6
SNN_MPCIE_8	15D4
SNN_MPCIE_10	15D4
SNN_MPCIE_12	15D4
SNN_MPCIE_14	15D4
SNN_MPCIE_16	15C4
SNN_MPCIE_17	15C6
SNN_MPCIE_19	15C6
SNN_MPCIE_45	15C6
SNN_MPCIE_47	15C6

SNN_MPCIE_49	15C6
SNN_MPCIE_51	15C6
SNN_NFC_IRQ_L	10A4
SNN_NFC_PROG	8C4
SNN_OWR	8B4
SNN_PEX_REFCLKN	14A4
SNN_PEX_REFCLKP	14A4
SNN_PEX_RX1_N	14B3
SNN_PEX_RX1_P	14B3
SNN_PEX_RX3_N	14B3
SNN_PEX_RX3_P	14B3
SNN_PEX_TX1_N	14B3
SNN_PEX_TX1_P	14B3
SNN_PEX_TX3_N	14B4
SNN_PEX_TX3_P	14B4
SNN_PG_OC_L	10B4
SNN_PM_I2C_SCL_3.3V	22C7
SNN_PM_I2C_SDA_3.3V	22C7
SNN_RI	18B2
SNN_SDMMC1_CLK	8B7
SNN_SDMMC1_CMD	8B7
SNN_SDMMC1_DAT<3..0>	8B7
SNN_SDMMC3_CLMP	25A7
SNN_SPKL_N	20C4
SNN_SPKL_P	20C4
SNN_SPKR_N	20C4
SNN_SPKR_P	20C4
SNN_SYS_CLK_REQ	8C4
SNN_TVS_USB_VBUS0	17C2
SNN_U27U1_Z1	6B7
SNN_U27U1_Z2	6B7
SNN_U27U1_Z3	6B7
SNN_U27U1_Z4	6B7
SNN_U27U2_Z1	6B3
SNN_U27U2_Z2	6B3
SNN_U27U2_Z3	6B3
SNN_U27U2_Z4	6B3
SNN_U28U1_Z1	7B7
SNN_U28U1_Z2	7B7
SNN_U28U1_Z3	7B7
SNN_U28U1_Z4	7B7
SNN_U28U2_Z1	7B3
SNN_U28U2_Z2	7B3
SNN_U28U2_Z3	7B3
SNN_U28U2_Z4	7B3
SNN_UART3_CTS_L	10C7
SNN_UART3_RTS_L	10C7
SNN_UART3_RXD	10C7
SNN_UART3_TXD	10C7
SNN_ULPI_DATA4	8D7
SNN_ULPI_DATA5	8D7
SNN_ULPI_DATA6	8C7
SNN_ULPI_DATA7	8C7
SNN_WF_RST_L	8B6
SPI4_CS0_L	10B3> 23B7<

SPI4_CS3_L	10C3> 24B2>
SPI4_MISO	10C3< 23A7> 24B2>
SPI4_MOSI	10C3> 23A4< 24B2>
SPI4_SCK	10C3> 23A4< 24B2>
SPI_HOLD_L	23A4
SPI_ROM_WP_L	23A6
SYS_RESET_L	8B3< 22A5< 23D7< 31B2>
TEMP_ALERT_L	10B3< 18A3>
TEMP_THERM_PMU	31B5
TEST_MODE_EN	8A4
THERMD_N	8B3< 18A7>
THERMD_P	8B3< 18A7<
THERMD_R_N	18A6
THERMD_R_P	18A6
TPS51220A_FUNC	27B7
TPS51220A_REG_EN	27A6
TPS51220A_RF	27B6
TPS51220A_TRIP	27A7
TPS_SKIPSEL	28C7> 29C8<
TP_ALS_IRQ_L	10A4
TP_AP_WP_L	8C4
TP_CLK_32K_WIFI	31C3
TP_CSI_DSI_TEST_OUT	9B7
TP_DAP1_DIN	10B7
TP_DAP1_FS	10B7
TP_DAP1_SCLK	10B7
TP_DAP4_DIN	10C7
TP_DAP4_DOUT	10C7
TP_DAP4_FS	10C7
TP_DAP4_SCLK	10C7
TP_DMIC_CLK	20B6
TP_DMIC_DATA	20A6
TP_GPIO_PH5	10C4
TP_GPIO_PH6	10C4
TP_GPIO_PI2	10B3
TP_GPIO_PK0	10B4
TP_GPIO_PK3	10B4
TP_KBC_IRQ_L	10C4
TP_KBL_PWM	10C4
TP_PEX_TESTCLK_N	14A4
TP_PEX_TESTCLK_P	14A4
TP_RESET_OUT_L	8B4
TP_TOUCH_IRQ_L	10A4
TP_ULPI_DATA1	8D7
TP_ULPI_DATA2	8D7
TP_USB_VBUS_EN2	14A4
TS_CLK	8B8> 26D6<
TS_RESET_L	10B3> 26D3<
TS_SHDN_L	10B3> 26D3<

<->

TITLE

?

NVIDIA CONFIDENTIAL

DOC NUMBER 602-7R375-0000-D00 | REV 4.04 | PAGE 41

TS_SPI_CS_L	8C7> 26D6>
TS_SPI_MISO	8C7< 26D3<
TS_SPI_MOSI	8C7> 26D3>
TS_SPI_SCK	8C7> 26D6>
UART2_CTS_L	10C7< 26A4>
UART2_RTS_L	10C7> 26A7<
UART2_RXD	10C7< 26A4>
UART2_TXD	10C7> 26A7<
UART4_CTS_3V3_L	18B5
UART4_CTS_L	10C3< 18B8> 22D7<
UART4_CTS_R_L	18B7
UART4_RTS_3V3_L	18C5
UART4_RTS_L	10B3> 18C7< 22D7> 24D5>
UART4_RXD	10C3< 18B8> 22D7<
UART4_RXD_3V3	18B5
UART4_RXD_R	18B7
UART4_TXD	10B3> 18C7< 22D7> 24C5>
UART4_TXD_3V3	18C5
USB0DL_N	17C3
USB0DL_P	17C3
USB0D_N	9A4<> 17C5<
USB0D_P	9A4<> 17C5<
USB0_ID	9A4< 17B1>
USB0_ID_AP_R	17B2
USB0_ID_C	17C3
USB0_ID_GATE_L	17B3
USB0_ID_PMU	17B1> 33D7<
USB0_ID_PWR	17D5
USB0_VBUS	9A4
USB1D_N	9A4<> 15C3<>
USB1D_P	9A4<> 15C3<>
USB2DL_N	17B5
USB2DL_P	17B5
USB2D_N	9A4<> 17B7<>
USB2D_P	9A4<> 17B7<>
USBSS_RX0R_N	16B4< 17A7>
USBSS_RX0R_P	16B4< 17A7>
USBSS_RX0_N	14C3< 16B8>
USBSS_RX0_P	14C3< 16B8>
USBSS_TX0C_N	16C4> 17A7<
USBSS_TX0C_P	16C4> 17A7<
USBSS_TX0_N	14C3> 16C8<
USBSS_TX0_P	14C3> 16C8<
USB_REXT	9A5
USB_VBUS_EN0	9A4<> 17C8<
USB_VBUS_EN1	9A4<> 17B8<
VDD_AC_SNUB	27D5
VDD_CORE_BOOST0	34A5
VDD_CORE_BOOST1	34A5
VDD_CORE_LX0	34A5
VDD_CORE_LX1	34A5
VDD_CORE_SENSE_N	11A2> 33B3<
VDD_CORE_SENSE_P	11A2> 33B3<
VDD_CPU_BOOST1	35D5
VDD_CPU_BOOST2	35D5
VDD_CPU_BOOST3	35B5
VDD_CPU_BOOST4	35B5
VDD_CPU_BOOST5	35A5
VDD_CPU_BOOST6	35A5
VDD_CPU_LX1	35D5
VDD_CPU_LX2	35C5
VDD_CPU_LX3	35B5
VDD_CPU_LX4	35B5
VDD_CPU_LX5	35A5
VDD_CPU_LX6	35A5
VDD_CPU_SENSE_N	11A2> 33C3<
VDD_CPU_SENSE_P	11B2> 33C3<
VDD_GPU_BOOST0	34D5
VDD_GPU_BOOST1	34D5
VDD_GPU_BOOST2	34B5
VDD_GPU_BOOST3	34B5
VDD_GPU_LX0	34D5
VDD_GPU_LX1	34C5
VDD_GPU_LX2	34B5
VDD_GPU_LX3	34B5
VDD_GPU_SENSE_N	11B2> 33C3<
VDD_GPU_SENSE_P	11B2> 33C3<
VN	18C3
VP	18C3
VREF_DDR0	6B5> 6B8<
VREF_DDR1	7B4> 7B8<
VVDD_CORE_PROBE	11A5
VVDD_CPU_PROBE	11A5
VVDD_GPU_PROBE	11B5
WF_DISABLE	15C2
WF_EN	10A3> 15C1<
WLAN_L	15C4
WLAN_LED	15C3
WPAN_L	15C4
WWAN_L	15C4
W_DISABLE_L	15C2
W_DISABLE_R_L	15C4
XTAL_IN	8A4
XTAL_LAN_N	19A6
XTAL_LAN_P	19A6
XTAL_OUT	8A4
YLW_STBYLED	25D4
YLW_STBYLED_L	25C4
Y_JTAG_TRST_L	22A5

<->

TITLE

?

NVIDIA CONFIDENTIAL

DOC NUMBER 602-7R375-0000-D00

REV 4.04

PAGE 42

Title: Cref Part Report
Design: beaver_t124_fabd
Date: Jul 23 17:18:06 2015

C1A1	CAP_0402_R	[18C5]
C1A2	CAP_0402_R	[18C5]
C1A3	CAP_0402_R	[18C3]
C1A4	CAP_0402_R	[18C3]
C1B1	CAP_0402_R	[13A4]
C1B2	CAP_0402_R	[13A4]
C1B3	CAP_0402_R	[13B4]
C1C1	CAPP_B2_R	[17B5]
C1C2	CAP_0402_R	[19B1]
C1D1	CAP_0402_R	[19A6]
C1D2	CAP_0402_R	[19C4]
C1D3	CAP_0603_R	[19C3]
C1D4	CAP_0402_R	[19C4]
C1D5	CAP_0603_R	[19C4]
C1D6	CAP_0402_R	[22C3]
C1D7	CAP_0402_R	[19A2]
C1D8	CAP_0402_R	[22C2]
C1D9	CAP_0402_R	[21A5]
C1E1	CAP_0402_R	[21C6]
C1E2	CAP_0402_R	[21B4]
C1E3	CAP_0402_R	[21A5]
C1E4	CAP_0402_R	[21A5]
C1E5	CAP_0603_R	[20B2]
C1E6	CAP_1206_R	[17C6]
C1E7	CAP_0805_R	[17C6]
C1E8	CAP_0603_R	[20B1]
C1E9	CAP_0402_R	[20B1]
C1E10	CAP_0603_R	[20A4]
C1E11	CAP_0603_R	[20B3]
C1E12	CAP_0402_R	[17B3]
C1E13	CAP_0603_R	[20B2]
C1E14	CAP_0402_R	[20B2]
C1E15	CAP_0402_R	[20B3]
C1E16	CAP_0402_R	[20B4]
C1E17	CAP_0402_R	[20A3]
C1E18	CAP_0603_R	[20A3]
C1E19	CAP_0402_R	[20C3]
C1E20	CAP_0402_R	[20A3]
C1E21	CAP_0402_R	[20C3]
C2A1	CAP_0402_R	[34A5]
C2A2	CAP_0402_R	[34A5]
C2A3	CAP_1206_R	[34A6]
C2A4	CAP_1206_R	[34A5]
C2A5	CAP_0805_R	[34A4]
C2A6	CAP_0805_R	[34A4]
C2B1	CAP_0201_R	[9B3]
C2C1	CAP_0402_R	[9A3]
C2C2	CAP_0402_R	[30A8]
C2C3	CAP_0805_R	[17B5]
C2C4	CAP_0402_R	[16C7]
C2C5	CAP_0402_R	[16C7]
C2C6	CAP_0402_R	[18A4]
C2C7	CAP_0402_R	[18A6]
C2C8	CAP_0402_R	[30A4]
C2D1	CAP_0603_R	[19B3]
C2D2	CAP_0402_R	[19B3]
C2D3	CAP_0402_R	[19A6]
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C2D6	CAP_0402_R	[19B4]
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C2D8	CAP_0402_R	[16A6]
C2D9	CAP_0402_R	[16B6]
C2D10	CAP_0402_R	[16B6]
C2D11	CAP_0402_R	[17C5]
C2D12	CAP_0402_R	[15C6]
C2D13	CAP_0402_R	[15C6]
C3A1	CAP_0402_R	[23B4]
C3B1	CAP_0201_R	[6A8]
C3C1	CAP_0201_R	[7A8]
C3C2	CAP_0201_R	[7A7]
C3D1	CAP_0402_R	[34D5]
C3D2	CAP_0402_R	[34D6]
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C3D4	CAP_1206_R	[34D6]
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C3D7	CAP_1206_R	[34D3]
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C3D9	CAP_1206_R	[34B3]
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C3E2	CAP_1206_R	[34C7]
C3E3	CAP_0402_R	[34B5]
C3E4	CAP_0402_R	[34B6]
C3E5	CAP_0402_R	[34B5]
C3E6	CAP_0603_R	[16A3]
C3E7	CAP_0402_R	[16A2]
C3E8	CAP_0402_R	[16B2]
C3E9	CAP_0805_R	[16C3]
C3E10	CAP_0402_R	[16C2]
C3E11	CAP_0402_R	[16B3]
C4A1	CAP_0402_R	[22B1]
C4A2	CAP_0402_R	[22B6]
C4B1	CAP_0201_R	[6A7]
C4B2	CAP_0201_R	[6A6]
C4B3	CAP_0402_R	[6A8]
C4B4	CAP_0805_R	[30C4]
C4B5	CAP_0402_R	[30C3]
C4B6	CAP_0402_R	[30B2]
C4C1	CAP_0402_R	[7A7]
C4C2	CAP_0201_R	[7B4]
C4C3	CAP_0201_R	[7A6]
C4C4	CAP_0201_R	[7A6]
C4C5	CAP_0201_R	[7B4]
C4C6	CAP_0402_R	[7A8]
C4C7	CAP_0201_R	[7A6]
C4C8	CAP_0201_R	[7A6]
C4D1	CAP_0402_R	[23C4]
C4D2	CAP_0402_R	[23C4]
C4D3	CAP_0402_R	[23D4]
C4D4	CAP_0402_R	[23D4]
C4D5	CAP_0402_R	[23C4]
C4D6	CAP_1206_R	[35B4]
C4D7	CAP_1206_R	[35C4]
C4D8	CAP_1206_R	[35D5]
C4D9	CAP_1206_R	[35A5]
C4D10	CAP_1206_R	[35C3]
C4D11	CAP_1206_R	[35C3]
C4D12	CAP_0402_R	[35A5]
C4D13	CAP_0402_R	[35D5]
C4D14	CAP_0402_R	[35A7]
C4D15	CAP_0402_R	[35D7]
C4D16	CAP_0402_R	[35A5]
C4D17	CAP_0402_R	[35D5]
C4D18	CAP_1206_R	[35C2]
C4D19	CAP_1206_R	[35C3]
C4D20	CAP_1206_R	[35A7]
C4D21	CAP_1206_R	[35D7]
C4E1	CAP_0402_R	[31C7]
C4E2	CAP_1206_R	[35C7]
C4E3	CAP_1206_R	[35C5]
C4E4	CAP_0402_R	[35B5]
C4E5	CAP_0402_R	[35B7]
C4E6	CAP_0402_R	[35B5]
C4E7	CAP_0402_R	[24A7]
C5A1	CAP_0402_R	[22A4]
C5B1	CAP_0402_R	[29A7]
C5B2	CAP_0402_R	[27C5]
C5B3	CAP_0402_R	[28B7]
C5C1	CAP_0402_R	[28B3]
C5C2	CAP_0402_R	[29B3]
C5C3	CAP_0805_R	[27C6]
C5C4	CAP_1206_R	[29C4]
C5C5	CAP_1206_R	[29C3]
C5C6	CAP_1206_R	[28C3]
C5C7	CAP_1206_R	[28C3]
C5C8	CAP_0402_R	[29B4]
C5C9	CAPP_DPOS_R	[29B2]

C5C10	CAPP_DPOS_R	[28C2]
C5C11	CAP_1206_R	[27D5]
C5D1	CAP_1206_R	[27D3]
C5D2	CAP_0402_R	[30B6]
C5D3	CAP_0402_R	[30B7]
C5D4	CAP_1206_R	[27D3]
C5D5	CAP_1206_R	[27D3]
C5D6	CAP_0402_R	[31A7]
C5D7	CAP_0402_R	[31A2]
C5D8	CAP_0402_R	[31B5]
C5D9	CAP_0603_R	[33B3]
C5D10	CAP_0603_R	[33B3]
C5D11	CAP_0805_R	[33B3]
C5D12	CAP_0805_R	[33B3]
C5D13	CAP_0402_R	[31A4]
C5D14	CAP_0402_R	[31B5]
C5D15	CAP_0805_R	[33A3]
C5D16	CAP_0402_R	[31D5]
C5D17	CAP_0402_R	[33A4]
C5E1	CAP_0402_R	[24B7]
C6B1	CAP_0402_R	[29A7]
C6B2	CAP_0402_R	[28A7]
C6C1	CAP_0402_R	[29B4]
C6C2	CAP_0402_R	[28B7]
C6C3	CAP_0603_R	[27B5]
C6C4	CAP_0402_R	[27A6]
C6C5	CAP_0805_R	[27B5]
C6C6	CAP_0402_R	[28C2]
C6C7	CAP_0402_R	[28C5]
C6C8	CAP_0402_R	[29C3]
C6C9	CAP_0805_R	[29B3]
C6C10	CAP_0805_R	[28C3]
C6C11	CAP_0402_R	[28B4]
C6C12	CAP_0402_R	[29C3]
C6C13	CAP_0402_R	[28C2]
C6D1	CAP_0402_R	[31B1]
C6D2	CAP_0402_R	[31B3]
C6D3	CAP_0402_R	[31A6]
C6D4	CAPP_SMD_3225	[31B5]
C6D5	CAP_0402_R	[31C4]
C6D6	CAP_0402_R	[31D5]
C6D7	CAP_0805_R	[33B6]
C6D8	CAP_0805_R	[33B3]
C6D9	CAP_0402_R	[32A7]
C6D10	CAP_0402_R	[32B5]
C6D11	CAP_0402_R	[32B7]
C6D12	CAP_0402_R	[32B7]
C6D13	CAP_0402_R	[32A6]
C6D14	CAP_0603_R	[33B6]
C6D15	CAP_0805_R	[33B6]
C6D16	CAP_0402_R	[32A5]
C6D17	CAP_0402_R	[32B7]
C6D18	CAP_0402_R	[32A7]
C6D19	CAP_0402_R	[32B6]
C6D20	CAP_0402_R	[32C6]
C6D21	CAP_0402_R	[32A5]
C6D22	CAP_0805_R	[33A3]
C6D23	CAP_0603_R	[32C7]
C6D24	CAP_0805_R	[33A6]
C6E1	CAP_0402_R	[32C5]
C6E2	CAP_0402_R	[32C5]
C6E3	CAP_0402_R	[32C5]
C6E4	CAP_0402_R	[32C7]
C6E5	CAP_0805_R	[33A6]
C6E6	CAP_0402_R	[32C7]
C6E7	CAP_0402_R	[32C6]
C6E8	CAP_0603_R	[33A3]
C6E9	CAP_0603_R	[33A3]
C7B1	CAP_0402_R	[25A4]
C7B2	CAP_0603_R	[25A4]
C7B3	CAP_0402_R	[22C7]
C7B4	CAP_0201_R	[6B4]
C7B5	CAP_0201_R	[6A8]
C7B6	CAP_0201_R	[6A7]
C7B7	CAP_0402_R	[6A8]
C7B8	CAP_0201_R	[6B8]
C7B9	CAP_0201_R	[6A6]
C7B10	CAP_0201_R	[6B4]
C7B11	CAP_0201_R	[6A6]
C7B12	CAP_0201_R	[6A6]
C7B13	CAP_0201_R	[6B8]
C7C1	CAP_0201_R	[7A6]
C7C2	CAP_0201_R	[7B8]
C7C3	CAP_0201_R	[6A6]
C7C4	CAP_0201_R	[7B8]
C7C5	CAP_0402_R	[6A7]
C7C6	CAP_0201_R	[6A6]
C7C7	CAP_0402_R	[7A8]
C7C8	CAP_0201_R	[7A6]
C7C9	CAP_0201_R	[7A6]
C7C10	CAP_0201_R	[7A7]
C7C11	CAP_0201_R	[7A8]
C7C12	CAP_0402_R	[7A7]
C7D1	CAP_0805_R	[35B4]
C7D2	CAP_0805_R	[35A4]
C7D3	CAP_1206_R	[35D5]
C7D4	CAP_1206_R	[35A5]
C7D5	CAP_0805_R	[35C4]
C7D6	CAP_0805_R	[35B4]
C7D7	CAP_1206_R	[35D7]
C7D8	CAP_1206_R	[35A7]
C7D9	CAP_0402_R	[32C5]
C7E1	CAP_0805_R	[35C4]
C7E2	CAP_0805_R	[35A4]
C7E3	CAP_1206_R	[35A4]
C7E4	CAP_1206_R	[35C5]
C7E5	CAP_1206_R	[35C7]
C8B1	CAP_0402_R	[22D7]
C8B2	CAP_0402_R	[8A4]
C8B3	CAP_0402_R	[8A4]
C8B4	CAP_0402_R	[6A7]
C8B5	CAP_0201_R	[6A6]
C8B6	CAP_0201_R	[6A6]
C8B7	CAP_0201_R	[8B7]
C8B8	CAP_0402_R	[8B7]
C8B9	CAP_0402_R	[8A4]
C8B10	CAP_0201_R	[10D3]
C8B11	CAP_0402_R	[14C6]
C8B12	CAP_0402_R	[10D3]
C8B13	CAP_0201_R	[14C6]
C8B14	CAP_0402_R	[5C2]
C8B15	CAP_0402_R	[8C7]
C8B16	CAP_0402_R	[5C3]
C8B17	CAP_0201_R	[4C3]
C8B18	CAP_0201_R	[10D6]
C8B19	CAP_0201_R	[5C4]
C8B20	CAP_0402_R	[8D4]
C8B21	CAP_0402_R	[5C2]
C8B22	CAP_0402_R	[9D4]
C8B23	CAP_0402_R	[10D6]
C8B24	CAP_0201_R	[8D4]
C8B25	CAP_0201_R	[8C6]
C8B26	CAP_0201_R	[9D4]
C8B27	CAP_0201_R	[8A4]
C8B28	CAP_0402_R	[5C2]
C8B29	CAP_0402_R	[11D7]
C8B30	CAP_0201_R	[5B4]
C8B31	CAP_0402_R	[5C2]
C8B32	CAP_0402_R	[11B8]
C8B33	CAP_0402_R	[11B8]
C8B34	CAP_0402_R	[11C4]
C8B35	CAP_0402_R	[11C4]
C8C1	CAP_0201_R	[4D4]
C8C2	CAP_0402_R	[11D7]
C8C3	CAP_0402_R	[11D4]
C8C4	CAP_0402_R	[11D4]
C8C5	CAP_0402_R	[11A7]
C8C6	CAP_0402_R	[11A7]
C8C7	CAP_0402_R	[5D4]
C8C8	CAP_0201_R	[5D4]
C8C9	CAP_0201_R	[11D8]
C8C10	CAP_0201_R	[5D4]
C8C11	CAP_0402_R	[5D4]

C8C12	CAP_0201_R	[4C2]
C8C13	CAP_0402_R	[11B8]
C8C14	CAP_0402_R	[11A8]
C8C15	CAP_0402_R	[11C4]
C8C16	CAP_0201_R	[4C4]
C8C17	CAP_0402_R	[11C4]
C8C18	CAP_0201_R	[5C4]
C8C19	CAP_0402_R	[11C8]
C8C20	CAP_0402_R	[5C4]
C8C21	CAP_0402_R	[11A8]
C8C22	CAP_0402_R	[11C5]
C8C23	CAP_0201_R	[11B7]
C8C24	CAP_0402_R	[11C8]
C8C25	CAP_0201_R	[11B8]
C8C26	CAP_0201_R	[11B7]
C8C27	CAP_0201_R	[11D4]
C8C28	CAP_0402_R	[5C3]
C8C29	CAP_0201_R	[11B7]
C8C30	CAP_0201_R	[11D5]
C8C31	CAP_0201_R	[5C4]
C8C32	CAP_0201_R	[11B8]
C8C33	CAP_0201_R	[8D4]
C8C34	CAP_0201_R	[11B7]
C8C35	CAP_0201_R	[11B7]
C8C36	CAP_0402_R	[5C3]
C8C37	CAP_0201_R	[11B8]
C8C38	CAP_0402_R	[5C3]
C8C39	CAP_0201_R	[11B7]
C8C40	CAP_0201_R	[11B7]
C8C41	CAP_0201_R	[10B6]
C8C42	CAP_0402_R	[11A7]
C8C43	CAP_0402_R	[10B6]
C8C44	CAP_0201_R	[8A6]
C8C45	CAP_0402_R	[8A7]
C8C46	CAP_0201_R	[7A6]
C8C47	CAP_0402_R	[8D4]
C8C48	CAP_0201_R	[14C3]
C8C49	CAP_0402_R	[14C3]
C8C50	CAP_0805_R	[11A8]
C8D1	CAP_1206_R	[34D7]
C8D2	CAP_1206_R	[34D5]
C8D3	CAP_0805_R	[34C4]
C8D4	CAP_0805_R	[34D4]
C8D5	CAP_0805_R	[34B4]
C8D6	CAP_0805_R	[34B4]
C8D7	CAP_1206_R	[34C6]
C8D8	CAP_1206_R	[34C5]
C9A1	CAP_0402_R	[34A7]
C9A2	CAP_0402_R	[18D3]
C9A3	CAP_1206_R	[34A5]
C9A4	CAP_1206_R	[34A7]
C9A5	CAP_0805_R	[34A3]
C9A6	CAP_0805_R	[34A4]
C9B1	CAP_0201_R	[9C3]
C9B2	CAP_0201_R	[9D4]
C9B3	CAP_0402_R	[9D4]
C9B4	CAP_0201_R	[9B4]
C9B5	CAP_0402_R	[9C4]
C9B6	CAP_0402_R	[9B4]
C9B7	CAP_0201_R	[9B4]
C9B8	CAP_0402_R	[11C7]
C9B9	CAP_0402_R	[9C2]
C9B10	CAP_0201_R	[11D8]
C9B11	CAP_0402_R	[11C8]
C9B12	CAP_0402_R	[11C7]
C9B13	CAP_0201_R	[9B7]
C9B14	CAP_0402_R	[9B7]
C9B15	CAP_0402_R	[9A7]
C9B16	CAP_0402_R	[11C7]
C9B17	CAP_0402_R	[9D7]
C9B18	CAP_0402_R	[9A4]
C9B19	CAP_0201_R	[8C4]
C9B20	CAP_0201_R	[9A4]
C9B21	CAP_0201_R	[9D7]
C9B22	CAP_0201_R	[10D3]
C9B23	CAP_0402_R	[9A4]
C9B24	CAP_0402_R	[10D3]
C9C1	CAP_0201_R	[9A4]
C9C2	CAP_0201_R	[11D7]
C9C3	CAP_0201_R	[8D6]
C9C4	CAP_0201_R	[11D8]
C9C5	CAP_0201_R	[9A7]
C9C6	CAP_0402_R	[8D6]
C9C7	CAP_0201_R	[14D3]
C9C8	CAP_0402_R	[14D3]
C9C9	CAP_0201_R	[11D4]
C9C10	CAP_0201_R	[14C3]
C9C11	CAP_0402_R	[14C3]
C9C12	CAP_0402_R	[14C3]
C9C13	CAP_0201_R	[14C3]
C9C14	CAP_0201_R	[14C6]
C9C15	CAP_0402_R	[14D6]
C9C16	CAP_0402_R	[14A2]
C9C17	CAP_0402_R	[14D7]
C9C18	CAP_0201_R	[14D6]
C9C19	CAP_0402_R	[14C6]
C9C20	CAP_0201_R	[14C3]
C9C21	CAP_0402_R	[14C3]
C9C22	CAP_0402_R	[16A7]
C9C23	CAP_0402_R	[16A7]
C9C24	CAP_0402_R	[16B7]
C9C25	CAP_0402_R	[16B7]
C9D1	CAP_0402_R	[30A5]
C9D1A	CAP_0402_R	[21A5]
C9D2	CAP_0603_R	[19C4]
C9D3	CAP_0402_R	[19C4]
C9D4	CAP_0402_R	[16D2]
C9D5	CAP_0402_R	[16D2]
C9D6	CAP_0402_R	[16C2]
C9D7	CAP_0402_R	[16D2]
C9D8	CAP_0402_R	[17D7]
C9E1	CAP_0603_R	[15D3]
C9E2	CAP_0603_R	[15B4]
C9E3	CAP_0603_R	[15B6]
C9E4	CAP_0805_R	[15D4]
C9E5	CAP_0402_R	[15B6]
C10A1	CAP_0402_R	[18B3]
C10B1	CAP_0402_R	[18B5]
C10B2	CAP_0402_R	[18C5]
C10B3	CAP_0402_R	[18C7]
C10B4	CAP_0402_R	[18C7]
C10B5	CAP_0603_R	[13A7]
C10B6	CAP_0402_R	[13D4]
C10B7	CAP_0402_R	[13B4]
C10C1	CAP_0402_R	[17B7]
C10C2	CAP_0603_R	[17B8]
C10C3	CAP_0402_R	[17B6]
C10C4	CAP_0402_R	[17B5]
C10C5	CAP_0402_R	[17B5]
C10D1	CAP_0402_R	[19B4]
C10D2	CAP_0402_R	[19B4]
C10D3	CAP_0402_R	[19B4]
C10E1	CAP_0402_R	[20B2]
C10E2	CAP_0402_R	[20B2]
C10E3	CAP_0603_R	[20B3]
C10E4	CAP_0603_R	[20A4]
C10E5	CAP_0402_R	[20A5]
C10E6	CAP_0402_R	[20A4]
C10E7	CAP_0402_R	[20A4]
C10E8	CAP_0402_R	[20A4]
C10E9	CAP_0402_R	[20A4]
C10E10	CAP_0402_R	[20A3]
CR1B1	TVS_DUAL_DIFF_PAIR_SLP251 0P8_R	[13C5 13C4]
CR1C1	TVS_DUAL_DIFF_PAIR_SLP251 0P8_R	[13C6 13C6]
CR1E1	TVS_USB_XSOP7_R	[17C3]
CR1E2	LED_0603_R	[15C3]
CR2C1	TVS_USB_XSOP7_R	[17A4]
CR2C2	TVS_DUAL_DIFF_PAIR_SLP251 0P8_R	[17A5 17A6]
CR2D1	DIODECC_S23_R	[17D6]
CR4E1	TVS_BIDIR2_SOD882_R	[24A8]

CR5E1	LED_0603_R	[30D5]
CR5E2	TVS_BIDIR2_SOD882_R	[24C7]
CR5E3	TVS_BIDIR2_SOD882_R	[24B7]
CR7B1	DIODESER_QUAD_XSOP7_R	[25A5]
CR7B2	DIODESER_QUAD_XSOP7_R	[25A6]
CR10C1	DIODECC_S323_R	[13B5]
HS3C1	HEATSINK_50MMX67MM_ELLIPT_IC_12V	[12C6]
ISO3A1	GNDISO_4MIL	[8A7]
ISO5C1	GNDISO_4MIL	[29B2]
ISO5C2	GNDISO_4MIL	[28B2]
ISO5D1	GNDISO_4MIL	[33B4]
ISO5D2	GNDISO_4MIL	[33A3]
ISO5E1	GNDISO_4MIL	[33A3]
ISO6C1	GNDISO_10MIL	[27A5]
ISO8C1	GNDISO_10MIL	[5B1]
ISO10D1	GNDISO_4MIL	[21A4]
J1A1	HDR2X5KEY10_THR_R	[25D5]
J1A2	SERIAL_DSUB_DSUB9_R	[18C1]
J1C1	CON_HDMI_A_SMT_G_R	[13C3]
J1C2	USBX1_V3_RA_FLAG_TH_R	[17B4]
J1D1	RJ45_1X1GBIT_MAG_LED_RJ45_2_R	[19A2]
J1D2	AUDIO_JACK_2PORT_LIMEPINK_THR_R	[21C4 21A4]
J1E1	CON_USB_MICRO_AB_TH_UAB_11P	[17C2]
J2D1	SATA_THR_SHRD_R	[16D1]
J2D2	MINI_PCI_EXPRESS_SMT_HALF_STND_R	[15C5]
J3A1	SKT2X25_THR_R	[26D5]
J3A2	SKT3X25_THR_R	[26B5]
J4A1	HDR2X10_THR_RA_SHR2	[22A1]
J4A2	FAN1X4_4PIN_FAN_R	[27C2]
J4E1	HDR1X1_THR	[24A8]
J4E2	SKT_PWR_IDE_THR_R	[16B1]
J5B1	CON_SD_SM1_R	[25B3]
J5C1	PWR_JACK_5P_THR_R	[27D6]
J5E1	HDR1X1_THR	[24C8]
J5E2	HDR1X1_THR	[24A8]
J7B1	HDR_24_FPC_RA_SMT2_R	[22C6]
L1B1	INDUCTOR_0402_R	[13A4]
L1D1	INDUCTOR_0402_R	[21A5]
L1D2	INDUCTOR_0402_R	[21C6]
L1E1	INDUCTOR_0402_R	[21B6]
L1E2	INDUCTOR_0402_R	[21A5]
L1E3	CHOKE_2012_R	[17C4 17C4]
L1E4	INDUCTOR_0402_R	[20B1]
L1E5	INDUCTOR_0402_R	[20A2]
L2A1	INDUCTOR_SMD_R	[34A5]
L2A2	INDUCTOR_SMD_R	[34A5]
L2D1	INDUCTOR_2016_R	[19C3]
L2D2	INDUCTOR_SMD_R	[19C3]
L5C1	INDUCTOR_SMD_R	[29C3]
L5C2	INDUCTOR_SMD_R	[28C3]

L6D1	INDUCTOR_SMD_R	[33B4]
L6E1	PWR_INDUCTOR_SMDA_R	[33A4]
L6E2	PWR_INDUCTOR_SMDA_R	[33A4]
L7D1	INDUCTOR_SMD_R	[35A5]
L7D2	INDUCTOR_SMD_R	[35D5]
L7D3	INDUCTOR_SMD_R	[35C5]
L7D4	INDUCTOR_SMD_R	[35A5]
L7E1	INDUCTOR_SMD_R	[35B5]
L7E2	INDUCTOR_SMD_R	[35B5]
L8B1	INDUCTOR_0402_R	[8A3]
L8D1	INDUCTOR_SMD_R	[34C4]
L8D2	INDUCTOR_SMD_R	[34D4]
L8D3	INDUCTOR_SMD_R	[34B4]
L8D4	INDUCTOR_SMD_R	[34B4]
L9B1	INDUCTOR_0402_R	[9B4]
L9B2	INDUCTOR_0402_R	[9A4]
L9C1	INDUCTOR_0402_R	[14C2]
L9C2	INDUCTOR_0402_R	[14D2]
L9C3	INDUCTOR_0402_R	[14C7]
L9C4	CHOKE_2012_R	[17B6 17B6]
L10B1	INDUCTOR_0402_R	[13B6]
L10B2	INDUCTOR_0402_R	[13B6]
L10B3	INDUCTOR_0402_R	[13C4]
L10E1	INDUCTOR_0402_R	[20A6]
M1A1	BRD_MOUNT_BRDMNT2	[12B7]
M1E1	BRD_MOUNT_BRDMNT2	[12A7]
M2E1	PEM_SMT_R	[15D4]
M3E1	PEM_SMT_R	[15C4]
M5A1	BRD_MOUNT_BRDMNT2	[12A6]
M5E1	BRD_MOUNT_BRDMNT2	[12B6]
Q1A1	MOSFETN_SC70S_SC70S_R	[25C4]
Q1A2	MOSFETN_SC70S_SC70S_R	[25D6]
Q1A3	MOSFETN_SC70S_SC70S_R	[25C3]
Q1E1	MOSFETN_SC70S_SC70S_R	[21B5]
Q2D1	MOSFETN_SC70S_SC70S_R	[18A2]
Q2D2	MOSFETN_SC70S_SC70S_R	[18A3]
Q2D3	MOSFETN_SC70S_SC70S_R	[17C6]
Q3E1	MOSFETN_SC70S_SC70S_R	[16A2]
Q3E2	MOSFETP_DFN3X3_DFN3X3_R	[16A2]
Q4A1	MOSFETN_SC70S_SC70S_R	[27C3]
Q4A2	MOSFETPSOT23_S23_R	[27D2]
Q4E1	MOSFETNSOT23_S23_R	[24A6]
Q4E2	MOSFETP_SC70S_SC70S_R	[24A6]
Q5D1	MOSFETNSOT23_S23_R	[32B1]
Q5D2	MOSFETNSOT23_S23_R	[32B2]
Q6C1	MOSFETN_DFN_DUAL_DFN3X3	[29C4]
Q6C2	MOSFETN_DFN_DUAL_DFN3X3	[28C4]
Q9A1	MOSFETPSOT23_S23_R	[9C3]
Q9A2	MOSFETPSOT23_S23_R	[9D3]

Q9A3	MOSFETNSOT23_S23_R	[9C3]
Q9A4	MOSFETNSOT23_S23_R	[9D3]
Q9D1	NPN_S363_R	[19B6 19B6]
Q9D2	MOSFETN_SC70S_SC70S_R	[15C2]
Q9D3	MOSFETN_SC70S_SC70S_R	[15C2]
Q9E1	MOSFETNSOT23_S23_R	[17B2]
Q9E2	MOSFETNSOT23_S23_R	[17B3]
Q9E3	MOSFETNSOT23_S23_R	[17A2]
Q10B1	MOSFETNSOT23_S23_R	[13C5]
R1A1	RES_0603_R	[25D4]
R1A2	RES_0603_R	[25D5]
R1A3	RES_0603_R	[25D4]
R1A4	RES_0402_R	[25C3]
R1A5	RES_0402_R	[25D3]
R1A6	RES_0402_R	[25C6]
R1A7	RES_0603_R	[25D5]
R1A8	RES_0402_R	[18C2]
R1B1	RES_0201_R	[24D7]
R1B2	RES_0201_R	[24C7]
R1B3	RES_0201_R	[24C7]
R1B4	RES_0201_R	[24D7]
R1B5	RES_0201_R	[24D6]
R1B6	RES_0201_R	[24C6]
R1B7	RES_0402_R	[13A7]
R1B8	RES_0402_R	[13B6]
R1B9	RES_0402_R	[13B6]
R1B10	RES_0402_R	[18B7]
R1B11	RES_0402_R	[18B7]
R1C1	RES_0402_R	[13D4]
R1C2	RES_0402_R	[17B7]
R1D1	RES_0402_R	[19A4]
R1D2	RES_0402_R	[19A1]
R1D3	RES_0402_R	[22D2]
R1D4	RES_0402_R	[22D2]
R1D5	RES_0402_R	[22D2]
R1D6	RES_0402_R	[21C5]
R1D7	RES_0402_R	[21C5]
R1D8	RES_0402_R	[21C5]
R1D9	RES_0402_R	[21C4]
R1E1	RES_0402_R	[21B4]
R1E2	RES_0402_R	[21B5]
R1E3	RES_0402_R	[21B5]
R1E4	RES_0402_R	[17D3]
R1E5	RES_0402_R	[20B1]
R1E6	RES_0402_R	[20B3]
R1E7	RES_0402_R	[20C7]
R1E8	RES_0402_R	[20B7]
R1E9	RES_0402_R	[20C3]
R1E10	RES_0402_R	[20C2]

TITLE
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NVIDIA CONFIDENTIAL

DOC NUMBER 602-7R375-0000-D00 | REV 4.04 | PAGE 46

R2A1	RES_0402_R	[18D6]
R2A2	RES_0402_R	[18D5]
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R2A4	RES_0402_R	[9D3]
R2A5	RES_0402_R	[9C3]
R2A6	RES_0402_R	[9D2]
R2A7	RES_0402_R	[9C2]
R2A8	RES_0402_R	[9D3]
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R2A12	RES_0402_R	[9C2]
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R2B3	RES_0201_R	[26C6]
R2B4	RES_0201_R	[26C5]
R2B5	RES_0201_R	[24D2]
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R2B8	RES_0201_R	[10B2]
R2B9	RES_0402_R	[8C7]
R2C1	RES_0402_R	[8C8]
R2C2	RES_0402_R	[30A7]
R2C3	RES_0402_R	[22A4]
R2C4	RES_0402_R	[14A3]
R2C5	RES_0201_R	[16B7]
R2C6	RES_0201_R	[16B7]
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R4A3	RES_0402_R	[22B2]
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R4B2	RES_0201_R	[6B4]
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R4E2	RES_0402_R	[31C7]
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R5D7	RES_0402_R	[32A5]
R5D8	RES_0402_R	[31B5]
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R5E5	RES_0402_R	[33D7]
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R6C3	RES_0805_R	[29B4]
R6C4	RES_0402_R	[29B7]
R6C5	RES_0402_R	[28B7]
R6C6	RES_0402_R	[28C7]
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R6C11	RES_0402_R	[28C3]
R6C12	RES_0805_R	[28C4]

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R6D3	RES_0402_R	[31A7]
R6D4	RES_0402_R	[31A7]
R6D5	RES_0402_R	[31B5]
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R6D12	RES_0402_R	[31C5]
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R6E2	RES_0402_R	[11A4]
R6E3	RES_0402_R	[11A2]
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R7B1	RES_0201_R	[6B7]
R7B2	RES_0201_R	[6B8]
R7C1	RES_0201_R	[7B7]
R7C2	RES_0201_R	[7B7]
R7C3	RES_0201_R	[7B3]
R7C4	RES_0201_R	[7B3]
R7C5	RES_0402_R	[7B5]
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R8B2	RES_0201_R	[24B3]
R8B3	RES_0201_R	[24B4]
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R8B19	RES_0201_R	[4C2]
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R8C7	RES_0201_R	[11A4]
R8C8	RES_0201_R	[11A4]
R9A1	RES_0402_R	[18D5]

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R9B2	RES_0201_R	[24B3]
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R9C5	RES_0201_R	[9A7]
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R9D13	RES_0402_R	[15C3]
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R10B2	RES_0402_R	[13D4]
R10B3	RES_0402_R	[13C5]

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R10E1	RES_0402_R	[17A3]
R10E2	RES_0402_R	[20B7]
R10E3	RES_0402_R	[20B6]
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R10E5	RES_0402_R	[20C3]
RT5D1	THERMISTOR_0402_R	[31A2]
SW4E1	BUTTON_6P_THICK_UNIV	[24A8]
SW5E1	BUTTON_6P_THICK_UNIV	[24B8]
SW5E2	BUTTON_6P_THICK_UNIV	[24C8]
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T3B5	TEE_TEE	[4C7]
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T3B25	TEE_TEE	[4C7]
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T3B27	TEE_TEE	[4C7]
T3B28	TEE_TEE	[4C7]
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T3B34	TEE_TEE	[4C7]
T3B35	TEE_TEE	[4B7]
T3B36	TEE_TEE	[4C7]
T3B37	TEE_TEE	[4B7]
T3B38	TEE_TEE	[4B7]
T3B39	TEE_TEE	[4A7]

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TITLE
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NVIDIA CONFIDENTIAL

DOC NUMBER 602-7R375-0000-D00 | REV 4.04 | PAGE 48

T3B40	TEE_TEE	[4A7]
T3B41	TEE_TEE	[4B7]
T3B42	TEE_TEE	[4A7]
T3B43	TEE_TEE	[4B7]
T3B44	TEE_TEE	[4B7]
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T3C2	TEE_TEE	[5C6]
T3C3	TEE_TEE	[5B6]
T3C4	TEE_TEE	[5B6]
T3C5	TEE_TEE	[5B6]
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T3C15	TEE_TEE	[5A6]
T3C16	TEE_TEE	[5A6]
T3C17	TEE_TEE	[5B6]
T3C18	TEE_TEE	[5A6]
T3C19	TEE_TEE	[5B6]
T3C20	TEE_TEE	[5B6]
T3C21	TEE_TEE	[5B6]
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T3C23	TEE_TEE	[5B6]
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T3C25	TEE_TEE	[5C6]
T3C26	TEE_TEE	[5C6]
T3C27	TEE_TEE	[5A6]
T3C28	TEE_TEE	[5B6]
T3C29	TEE_TEE	[5C6]
T3C30	TEE_TEE	[5A6]
T3C31	TEE_TEE	[5B6]
T3C32	TEE_TEE	[5A6]
T3C33	TEE_TEE	[5B6]
T3C34	TEE_TEE	[5B6]
T3C35	TEE_TEE	[5C6]
T3C36	TEE_TEE	[5C6]
T3C37	TEE_TEE	[5B6]
T3C38	TEE_TEE	[5B6]
T3C39	TEE_TEE	[5B6]
T3C40	TEE_TEE	[5A6]
T3C41	TEE_TEE	[5B6]
T3C42	TEE_TEE	[5A6]
T3C43	TEE_TEE	[5B6]
T3C44	TEE_TEE	[5B6]
T4B1	TEE_TEE	[6D7]
T4B2	TEE_TEE	[6D7]
T4B3	TEE_TEE	[7D7]
T4B4	TEE_TEE	[6C7]
T4B5	TEE_TEE	[7C7]
T4B6	TEE_TEE	[6D7]
T4B7	TEE_TEE	[6D7]
T4B8	TEE_TEE	[6C7]
T4B9	TEE_TEE	[7B7]
T4B10	TEE_TEE	[6D7]
T4B11	TEE_TEE	[7C7]
T4B12	TEE_TEE	[6D7]
T4B13	TEE_TEE	[6D7]
T4B14	TEE_TEE	[6B7]
T4B15	TEE_TEE	[7D7]
T4B16	TEE_TEE	[7C7]
T4B17	TEE_TEE	[6B7]
T4B18	TEE_TEE	[4D5]
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T4B20	TEE_TEE	[6C7]
T4B21	TEE_TEE	[6D7]
T4B22	TEE_TEE	[6D7]
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T4B29	TEE_TEE	[7D7]
T4B30	TEE_TEE	[6B7]
T4B31	TEE_TEE	[6B7]
T4B32	TEE_TEE	[4C5]
T4B33	TEE_TEE	[4C5]
T4C1	TEE_TEE	[4C5]
T4C2	TEE_TEE	[4C5]
T4C3	TEE_TEE	[4B5]
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T4C9	TEE_TEE	[4B5]
T4C10	TEE_TEE	[4C5]
T4C11	TEE_TEE	[4B5]
T4C12	TEE_TEE	[4C5]
T4C13	TEE_TEE	[4C5]
T4C14	TEE_TEE	[4C5]
T4C15	TEE_TEE	[4B5]
T4C16	TEE_TEE	[4B5]
T4C17	TEE_TEE	[4B5]
T4C18	TEE_TEE	[4C5]
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T4C20	TEE_TEE	[7C7]
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T4C31	TEE_TEE	[4C5]
T4C32	TEE_TEE	[7D7]
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T4C35	TEE_TEE	[7C7]
T4C36	TEE_TEE	[6C7]
T4C37	TEE_TEE	[7B7]
T4C38	TEE_TEE	[6D7]
T4C39	TEE_TEE	[7D7]
T4C40	TEE_TEE	[7D7]
T4C41	TEE_TEE	[6D7]
T4C42	TEE_TEE	[7C7]
T4C43	TEE_TEE	[4C5]
T4C44	TEE_TEE	[6C7]
T4C45	TEE_TEE	[7D7]
T4C46	TEE_TEE	[7B7]
T4C47	TEE_TEE	[7B7]
T4C48	TEE_TEE	[7D7]
T4C49	TEE_TEE	[7B7]
U1B1	SERIAL_RS232_3V3_TSSOP16_R	[18C4]
U1B2	LEVEL_SHIFTER_2BIT_SSOP8_R	[18C6]
U1B3	LEVEL_SHIFTER_2BIT_SSOP8_R	[18B6]
U1B4	POWER_SW_SON7_R	[13A6]
U1C1	POWER_SW_SON8_R	[17B6]
U1D1	PCA9306_QFN8_R	[22C3]
U1E1	ALC5639_QFN48	[20B5]
U2A1	EEPROM_2WIRE_8PIN_DFN08_R	[18D4]
U2A2	AS3728_CSP	[34A6]
U2C1	POWER_SW_BGA04_R	[30A7]
U2C2	TEMP_SENSOR_DFN08	[18A5]
U2D1	SLG5NV1430V_TDFN-6_R	[30A4]
U2D2	RTL8111GS_QFN-33_R	[19B5]
U2D3	POWER_SW_SOT23_5B_R	[17C7]
U3A1	EEPROM_SPI_8PIN_SOIC_R	[23A5]
U3C1	T124MID_PM375_BGA	[4C6]
U3C1	T124MID_PM375_BGA	[5B5]
U3C1	T124MID_PM375_BGA	[8C5]
U3C1	T124MID_PM375_BGA	[9C5]

U3C1	T124MID_PM375_BGA	[10B5]
U3C1	T124MID_PM375_BGA	[11C6]
U3C1	T124MID_PM375_BGA	[12B3]
U3C1	T124MID_PM375_BGA	[14C5]
U3E1	SLG5NV1430V_TDFN-6_R	[16B2]
U4A1	RST_MON_SOT23_6PIN_R	[22A5]
U4A3	RST_MON_SOT23_3_R	[22B5]
U4B1	DDR3_X16_BGA100_2	[6C2]
U4B2	POWER_SW_BGA04_R	[30B3]
U4C1	DDR3_X16_BGA100_2	[7C6]
U5A1	BUFFER_5PIN_SC70_R	[22A3]
U5C1	U_SWREG_TPS51220_QFN32	[27B5]
U5C1	U_SWREG_TPS51220_QFN32	[28B6]
U5C1	U_SWREG_TPS51220_QFN32	[29B6]
U5D1	SLG5NV1430V_TDFN-6_R	[30C6]
U5D2	D_FLIP_FLOP_6PIN_SC70_6	[31A6]
U6D1	AS3722_BGA	[31B4]
U6D1	AS3722_BGA	[32C6]
U6D1	AS3722_BGA	[33B5]
U7B1	DDR3_X16_BGA100_2	[6C6]
U7C1	DDR3_X16_BGA100_2	[7C2]
U7D1	EMMC_BGA169_1	[23C5]
U7D2	AS3728_CSP	[35D6]
U7D3	AS3728_CSP	[35A6]
U7E1	AS3728_CSP	[35B6]
U8D1	AS3728_CSP	[34D6]
U8E1	AS3728_CSP	[34B6]
U9E1	APL5910_SOP8P_R	[15B5]
Y2C1	XTAL_HC49_R	[19A6]
Y6D1	XTAL_CER_2P_R	[31B2]
Y8B1	XTAL_SMD4P_R	[8A4]

TITLE

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DOC NUMBER 602-7R375-0000-D00 | REV 4.04 | PAGE 50