Jetson AGX Xavier Series Interface Comparison and Migration

Application Note

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Document History

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Version	Date	Description of Change
1.0	June 22, 2021	Initial Release
1.1	July 6, 2021	• Updated JAXi signal and function in Table 2 • Updated safety MCU support in the "Safety MCU Interfaces" section • Updated pin function differences in Table 3
1.2	December 3, 2021	Updated to include Jetson AGX Xavier 64GB

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Introduction

This application note compares the features and interfaces supported on the NVIDIA® Jetson AGX Xavier™ Industrial, Jetson AGX Xavier 64GB, and the other Jetson AGX Xavier series modules. This application note also describes the migration path for designers familiar with Jetson AGX Xavier or Jetson AGX Xavier 64GB to design a carrier board that will support the features available on Jetson AGX Xavier Industrial.

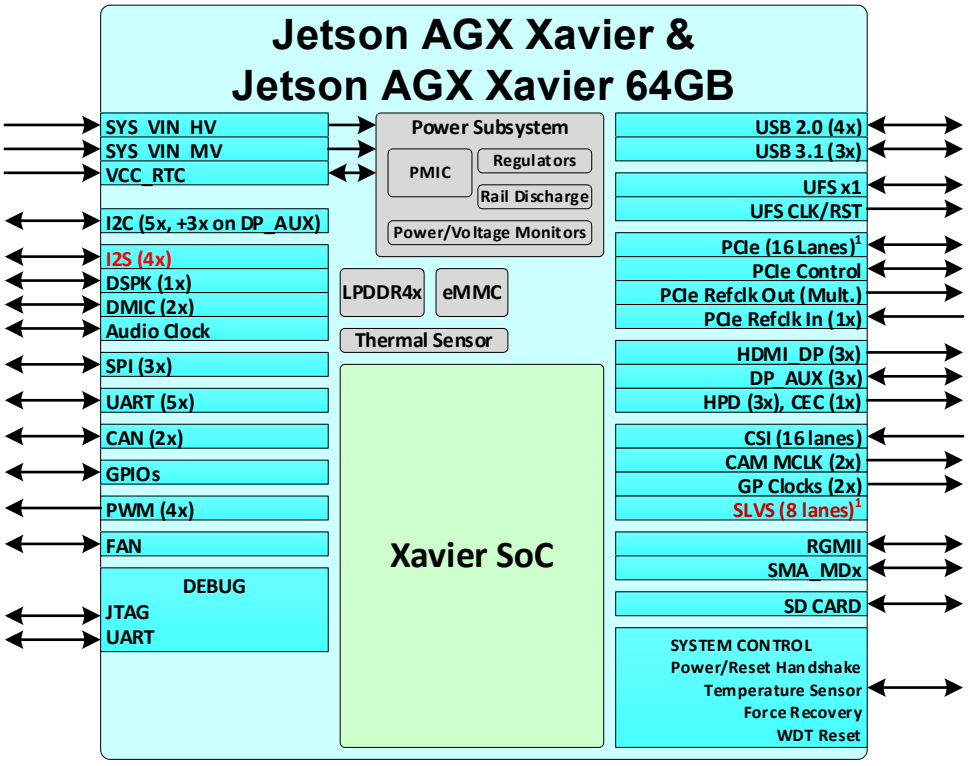
Note: Jetson AGX Xavier, Jetson AGX Xavier 64GB, and Jetson AGX Xavier Industrial may be referred to as JAX, JAX 64GB, and JAXi respectively.

Jetson AGX Xavier and Jetson AGX Xavier 64GB vs. Jetson AGX Xavier Industrial

JAX, JAX 64GB, and JAXi are largely pin compatible. This section describes the differences between the modules.

The following figures show the JAX and JAX 64GB, and JAXi block diagrams. The interfaces or blocks that are supported only by one of the modules are highlighted in red. The interface types that are supported on JAX, JAX 64GB, and JAXi modules but where the number of lanes and instances, voltage level, or access is different, are highlighted in magenta.

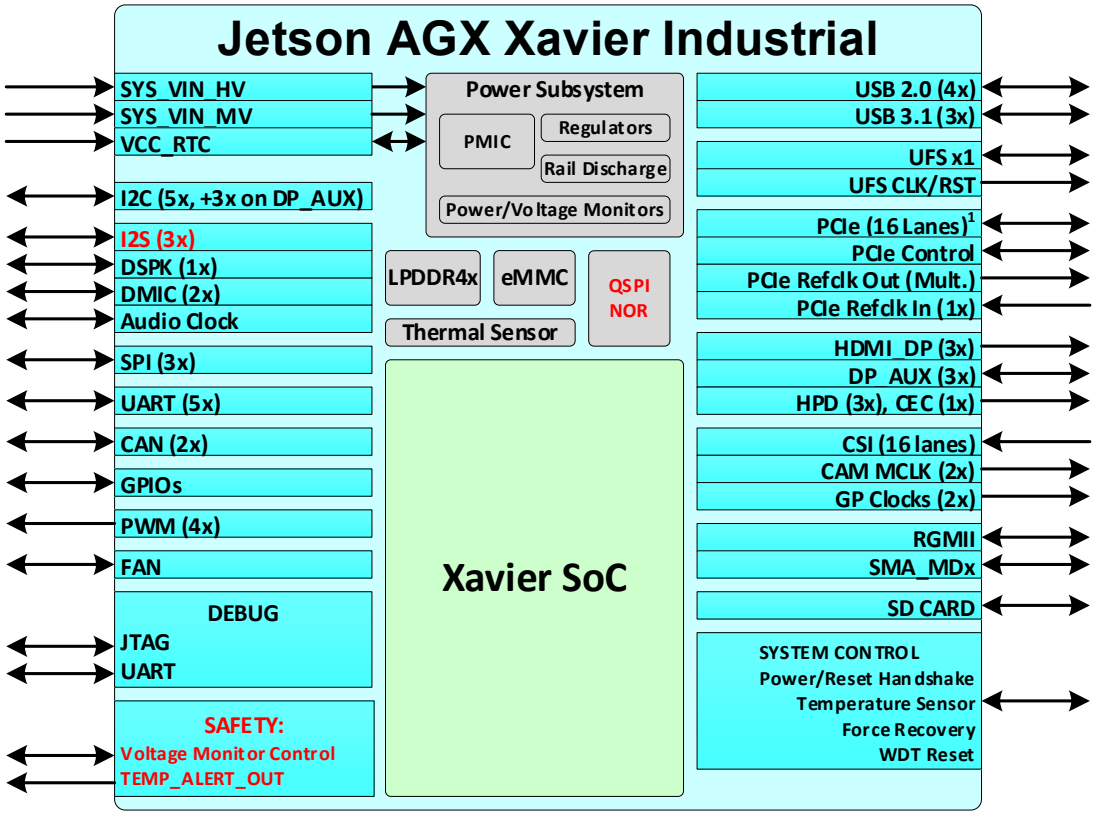
Figure 1. Jetson AGX Xavier and Jetson AGX Xavier 64GB Block Diagram



Note:

1. SLVS and PCIe share UPHY lanes.
2. DP_AUX pins can optionally be used as additional I2C interfaces.

Figure 2. Jetson AGX Xavier Industrial Block Diagram



Note: DP_AUX pins can optionally be used as additional I2C interfaces.

Module Feature and Interface Comparisons

Table 1 lists the key system specifications, devices, and interfaces that are supported on the JAX, JAX 64GB, or the JAXi module.

Table 1. JAX, JAX 64GB, and JAXi Feature Comparison

Feature	Jetson AGX Xavier	Jetson AGX Xavier 64GB	Jetson AGX Xavier Industrial
System Specifications and Device on the Module			
GPU	NVIDIA Volta™ architecture with 512 NVIDIA® CUDA® cores and 64 Tensor cores		
CPU	8-core NVIDIA Carmel Arm®v8.2 64-bit CPU, 8MB L2 + 4MB L3		
DL Accelerator	GPU (22.6 TOPs) and 2x NVDLA Engines (5.7 TOPs each)		GPU (19.8 TOPs) and 2x NVDLA Engines (5.27 TOPs each)
Vision Accelerator	2x 7-Way VLIW Vision Processor (1.1 DL INT8 TOP)		
Memory	8/16/32 GB 256-bit LPDDR4x	64 GB 256-bit LPDDR4x	32 GB 256-bit LPDDR4x w/ECC
Storage	32 GB eMMC		64 GB eMMC
QSPI NOR	Not supported		64 MB
Networking: RGMII	10/100/1000 Mbit		
Video Encode	4x 4K60 (H.265) 8x 4K30 (H.265) 16x 1080p60 (H.265) 32x 1080p30 (H.265) 30x1080p30 (H.264)		2x 4K60 (H.265/H.264) 6x 4K30 (H.265/H.264) 12x 1080p60 (H.265/H.264) 24x 1080p30 (H.265/H.264)
Video Decode	2x 8K30 (H.265) 6x 4K60 (H.265) 12x 4K30 (H.265) 26x 1080p60 (H.265) 52x 1080p30 (H.265) 30x 1080p30 (H.264		2x 8K30 (H.265) 4x 4K60 (H.265) 8x 4K30 (H.265) 18x 1080p60 (H.265) 36x 1080p30 (H.265) 24x 1080p30(H.264)
Mechanical	100 mm x 87 mm x 15.23 mm		

Feature	Jetson AGX Xavier	Jetson AGX Xavier 64GB	Jetson AGX Xavier Industrial
Input Voltage	HV rail: 9V to 20V MV rail: 5V		
Operating Temperature Range	-25C to 80C		-40C to 85C
Interfaces			
USB 2.0	4x		
USB 3.x	3x (3.1)		
PCIe	2 x1 (Gen4) + 1 x2 + 1 x4 + 1 x8. All support Root Port. Only x8 has both Root Port and Endpoint support.		
Display	Three multi-mode (e)DP 1.4/HDMI™ 2.0a		
CSI	16 lanes (4x4 or 6x2 or 6x1) MIPI CSI-2 D-PHY 1.2 (2.5Gb/s per pair, total up to 40 Gbps) C-PHY 1.1 (1.7Gsym/s per trio, total up to 62 Gbps)		
SLVS	8-lane		Not Supported
Audio (I2S)	4x		3x
SDIO/SD Card	1x SD Card/SDIO		
Gigabit Ethernet	Supported		
I2C	5x (+3x on DP_AUX pins)		
UART	5x		
SPI	3x		
CAN	2x		
JTAG	Supported		
Fan	PWM and Tach Input		

Function and Interface Difference Details

Module Input Voltage and Mechanicals

JAX, JAX 64GB, and JAXi have the same input voltage requirements, power sequencing, and are mechanically equivalent.

Interface Migration

The following sections show any differences between JAX, JAX 64GB, and JAXi. Any interfaces that remain the same between the two modules are not included.

PCIe, USB 3.1, UFS and SLVS Mapping Options

JAX, JAX 64GB, and JAXi support the same mapping for PCIe, USB 3.1, and UFS on the UPHY lanes. However, JAX and JAX 64GB support SLVS as an alternative on the PCIe x8 interface on the NVHSx pins. JAXi does not.

Audio

JAX and JAX 64GB support up to four I2S interfaces. JAXi supports up to three I2S interfaces. The GPIO05 pin which supports **I2S6_SDATA_OUT** functionality on JAX and JAX 64GB is instead routed to the SoC **CAN0_ERR** pin on JAXi so the I2S interface is not supported.

Table 2. JAX, JAX 64GB, and JAXi Audio Interface Differences

Pin #	Module Pin Name	JAXi Function	JAX Function	Xavier SoC Signal
B58	GPIO21	GPIO	GPIO or I2C6_SCLK	DAP6_SCLK
A58	GPIO20	GPIO	GPIO or I2C6_LRCK	DAP6_FS
A59	GPIO05	GPIO	GPIO or I2C6_SDATA_OUT	JAX and JAX 64GB: DAP6_DOUT JAXi: CAN0_ERR
B59	GPIO04	GPIO	GPIO or I2C6_SDATA_DIN	DAP6_DIN

I2C

JAX, JAX 64GB, and JAXi all support up to five I2C interfaces (plus up to three additional on the **DPU_AUX** pins) from the NVIDIA® Xavier™ system-on-chip (SoC). In addition, JAXi has an additional set of I2C pins (**VM_I2C**) to support connection to a Safety MCU to monitor the module voltages. The **VM_I2C** interface is routed to a mux along with the Xavier SoC **PWR_I2C** interface. When **SYS_RESET_N** is active, the **VM_I2C** interface is in control of the voltage monitors. When **SYS_RESET_N** is inactive, **PWR_I2C** has control.

SPI

JAX, JAX 64GB, and JAXi all support up to four SPI interfaces. For JAXi, SPI2 is available to interface to a Safety MCU if one is included in a design.

Safety MCU Interfaces

JAXi uses some of the existing signals to interface to a Safety MCU if implemented in a design. This includes:

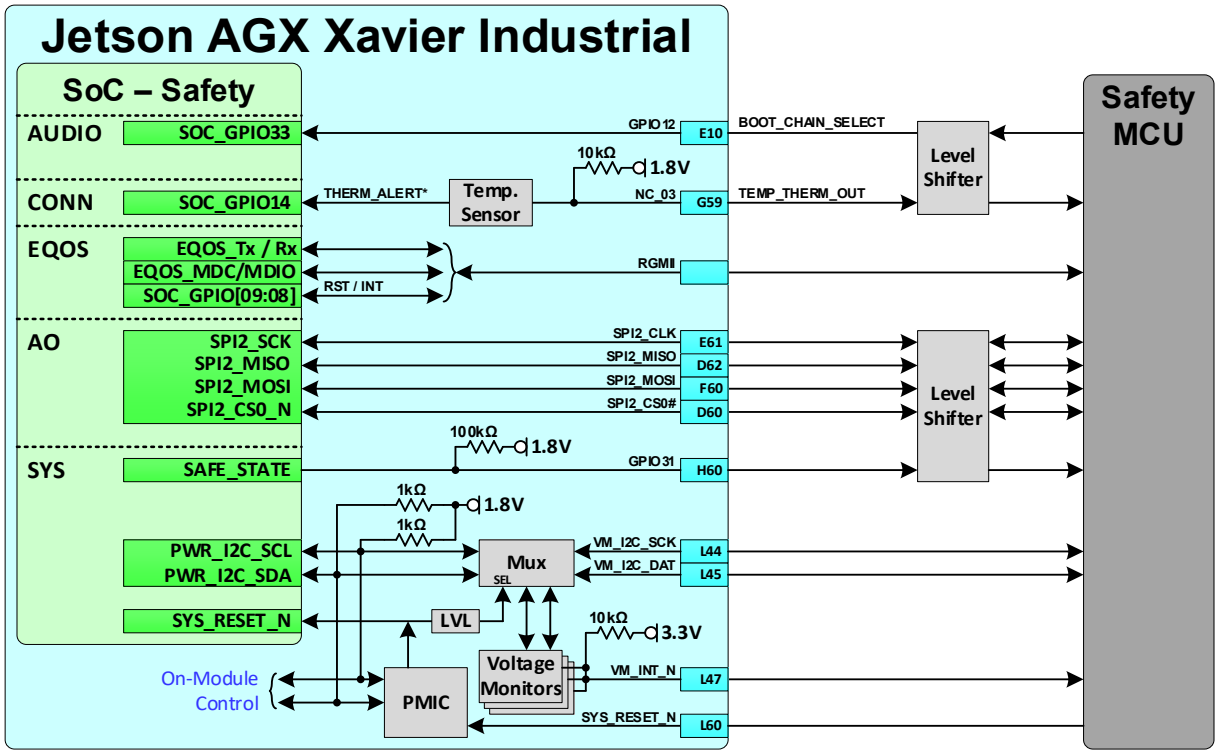
- SPI2
- EQOS and RGMII (Ethernet)
- GPIO31 (SAFESTATE)
- GPIO12 (BOOT_CHAIN_SELECT strap)

If not used to connect to a Safety MCU, the pins listed support the same functionality as on JAX or JAX 64GB.

In addition, several others interface pins that were not supported on JAX or JAX 64GB are available to interface to the Safety MCU including:

- VM_I2C (Voltage Monitor I2C)
- VM_INT_N (Voltage Monitor Interrupt)
- NC_03 (TEMP_THERM_OUT)

Figure 3. Safety MCU Connections



Connector Pin Difference Details

The following table lists the pins that have different functionality between JAX and JAX 64GB compared to JAXi. For some pins, the supported function is different. For others (highlighted in light blue), the functionality is similar, but for JAXi, the pins may be used to interface to a Safety MCU if implemented in a design.

Table 3. Connector Pin Function Differences

Module Pin #	Module Pin Name	Xavier SoC Pin Name	JAX and JAX 64GB Usage/Description	JAXi Usage / Description
B58	GPIO21	DAP6_SCLK	GPIO / I2S	GPIO
A58	GPIO20	DAP6_FS		
B59	GPIO04	DAP6_DIN		
A59	GPIO05	JAX and JAX 64GB: DAP6_DOUT JAXi: CAN0_ERR		
C55	GPIO18	SOC_GPIO40	GPIO / SLVS	GPIO only
K56	GPIO19	SOC_GPIO43		
L44	VM_I2C_SCK	–	Reserved	Voltage Monitor I2C, routed to Safety MCU if implemented.
L45	VM_I2C_DAT	–		
L47	VM_INT_N	–		Voltage Monitor Interrupt, routed to Safety MCU if implemented.
G59	NC_03	–		TEMP_THERM_OUT
H60	GPIO31	SAFE_STATE	GPIO	GPIO (for Safety MCU if implemented)
E10	GPIO12	SOC_GPIO33	GPIO	GPIO. Also boot chain support for Safety enabled designs.
E61	SPI2_CLK	SPI2_SCK	SPI or GPIO	Same. Routed to Safety MCU if needed. (SPI2_CS0 can initiate IST if low during power-on)
D60	SPI2_CS0_N	SPI2_CS0		
D62	SPI2_MISO	SPI2_MISO		
F60	SPI2_MOSI	SPI2_MOSI		
D25	NVHS0_SLVS_RX0_N	NVHS0_RX0_N	PCIe or SLVS	PCIe only
D24	NVHS0_SLVS_RX0_P	NVHS0_RX0_P		
B24	NVHS0_SLVS_RX1_N	NVHS0_RX1_N		

Module Pin #	Module Pin Name	Xavier SoC Pin Name	JAX and JAX 64GB Usage/Description	JAXi Usage / Description
B25	NVHS0_SLVS_RX1_P	NVHS0_RX1_P		
C26	NVHS0_SLVS_RX2_N	NVHS0_RX2_N		
C27	NVHS0_SLVS_RX2_P	NVHS0_RX2_P		
A27	NVHS0_SLVS_RX3_N	NVHS0_RX3_N		
A26	NVHS0_SLVS_RX3_P	NVHS0_RX3_P		
D29	NVHS0_SLVS_RX4_N	NVHS0_RX4_N		
D28	NVHS0_SLVS_RX4_P	NVHS0_RX4_P		
B28	NVHS0_SLVS_RX5_N	NVHS0_RX5_N		
B29	NVHS0_SLVS_RX5_P	NVHS0_RX5_P		
C30	NVHS0_SLVS_RX6_N	NVHS0_RX6_N		
C31	NVHS0_SLVS_RX6_P	NVHS0_RX6_P		
A31	NVHS0_SLVS_RX7_N	NVHS0_RX7_N		
A30	NVHS0_SLVS_RX7_P	NVHS0_RX7_P		
E31	NVHS0_SLVS_REFCLK0_N	NVHS0_REFCLK_N		
E30	NVHS0_SLVS_REFCLK0_P	NVHS0_REFCLK_P		
K53	UART1_TX	UART1_TX	UART or GPIO. Also used as SoC strap during power-on.	Same, but buffered on module to keep strap state from being affected by connected device. This changes direction to output only if used as GPIO
L51	UART1_RTS	UART1_RTS		
C58	UART2_TX	UART2_TX		
G58	UART2_RTS	UART2_RTS		
L5	UART4_TX	UART4_TX		
L4	UART4_RTS	UART4_RTS		
J58	UART5_TX	UART5_TX		
K58	UART5_RTS	UART5_RTS		

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