Jetson TK1 Development Kit Specification

Abstract

This document contains recommendations and guidelines for engineers to follow to create modules for the expansion connectors on the Jetson TK1 Development Kit as well as understand the capabilities of the other dedicated interface connectors and associated power solutions.

November 2014

DA-07507-001

Version 01

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Table of Contents

1.0 Introduction

1.1 Abbreviations and Definitions

The following table lists abbreviations that may be used throughout this document and their definitions.

Table 1. Abbreviations and Definitions

Abbreviation	Definition
BT	Bluetooth
CEC	Consumer Electronic Control
DDR3L	Double Data Rate DRAM, Third-generation
eMMC	Embedded MMC
GPS	Global Positioning System
HDMI	High Definition Multimedia Interface
HSIC	High Speed Inter Chip Interface
I2C	Inter IC
I2S	Inter IC Sound Interface
LCD	Liquid Crystal Display
LDO	Low Dropout (voltage regulator)
LVDS	Low Voltage Differential Signaling Interface
PCIe	Peripheral Component Interconnect Express interface
PCM	Pulse Code Modulation
PHY	Physical Interface (i.e. USB PHY)
PMC	Power Management Controller
PMU	Power Management Unit
RF	Radio Frequency
SATA	Serial “AT” Attachment interface
SDIO	Secure Digital I/O Interface
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
WiFi (WLAN)	Wireless Local Area Network

1.2 Jetson TK1 – High Level Definition Summary

Jetson is a low cost Tegra K1 developer kit intended to enable OEM's to evaluate the Tegra K1 architecture and then create a customized design that matches their exact requirements. Jetson provides basic boot options with expansion connectors to enable unused ports to be interfaced with customized hardware.

1.3 Feature List

Applications Processor
- Tegra K1 processor, CD575M
- 23x23mm ,0.7mm pitch

DRAM
- DDR3L-1866, 2GB
- Hynix H5TC4G63AFR-RDA
- 4 x 4Gb x16 memory (64 bit width)

Flash (Boot/Storage)
- SPI Flash: Winbond W25Q32DW, 32Mbit
- eMMC: Sandisk SDIN8DE4-16G-Q
  - 16GB, 4.51
- Full Size SD Card
- SATA Connector

HDMI
- HDMI Type A

USB
- 1x USB 3.0 Type A
- 1x USB 2.0 Micro AB

Audio
- Codec: Realtek ALC5639
- 3.5mm Microphone Jack
- 3.5mm Headset Jack

LAN
- Realtek RTL8111GS Gigabit MAC/PHY
- PCIe (x1 lane), RJ45 Connector

UI & Indicators
- Power, Reset & Force Recovery Buttons

Sensors
- Temp Sensor: TMP451

Debug
- JTAG: Standard 20-pin header
- UART: RS232, D-Sub 9 Connector

Mini-PCIe Connector
- PCIe x1 Lane
- USB 2.0
- I2C (3.3V)
- WLAN Control/LEDs

Display/Touch Expansion Header
- LVDS/eDP x4 Lanes
- Hot Plug Detect
- Backlight Enable/PWM
- Touch Controller Support
  - SPI, I2C
  - Clock, Shutdown, Reset

General Expansion Header
- Camera Support
  - CSI: 1 x4 + 1 x1
  - CLK, I2C & Control
  - Dedicated Power Rails
- HSIC
- UART
- GPIOs

Power
- PMU: AMS AS3722, BCTT-09
- CPU Supply: AS3728 Power Stages (x3)
- GPU Supply: AS3728 Power Stages (x2)
- CORE Supply: AS3728 Power Stage
- Pre-Regulators: TI TPS51220
- 12V DC Jack

PCB Technology
- 6-layer, Standard Technology

1.4 Jetson Block Diagram

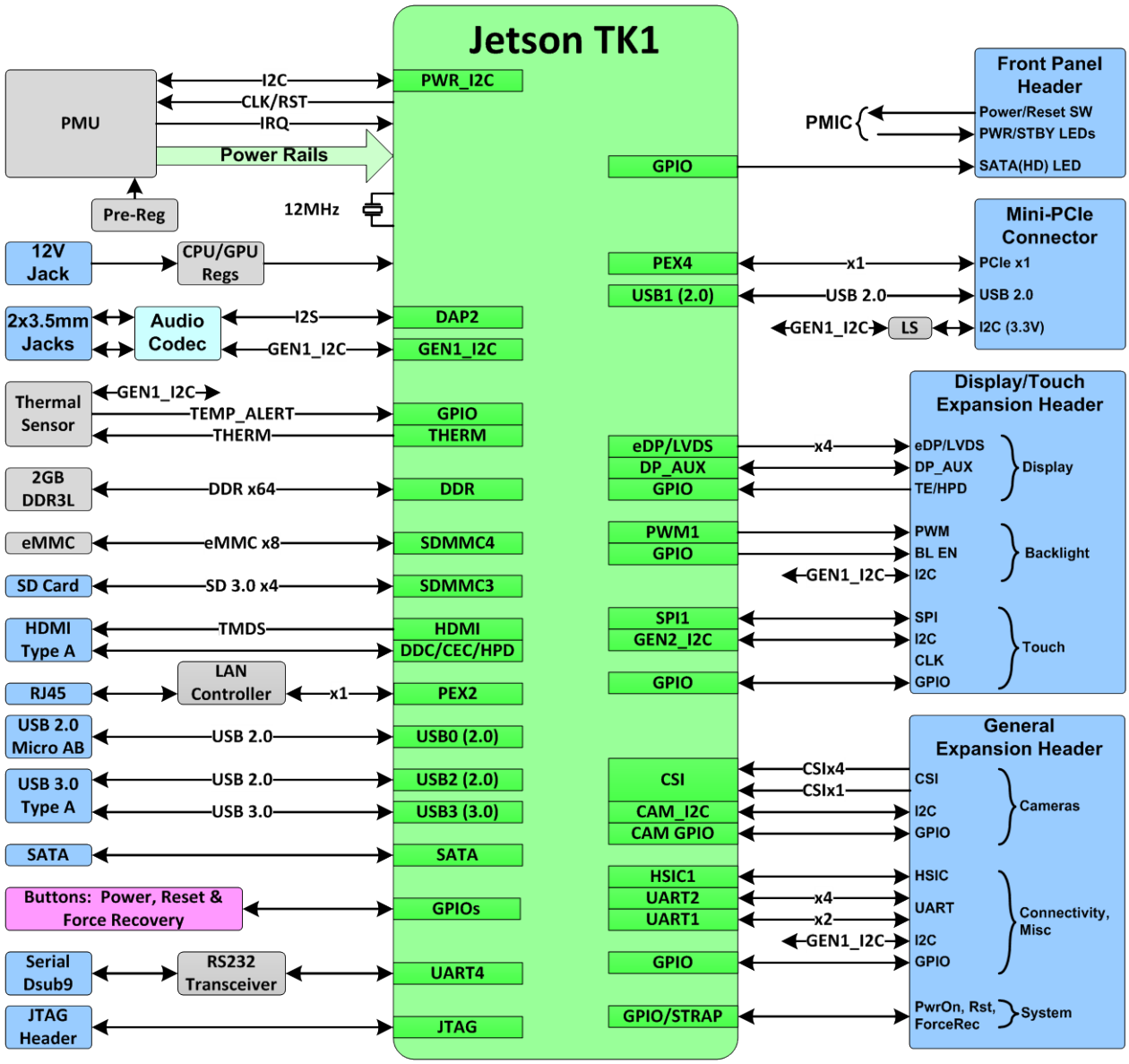
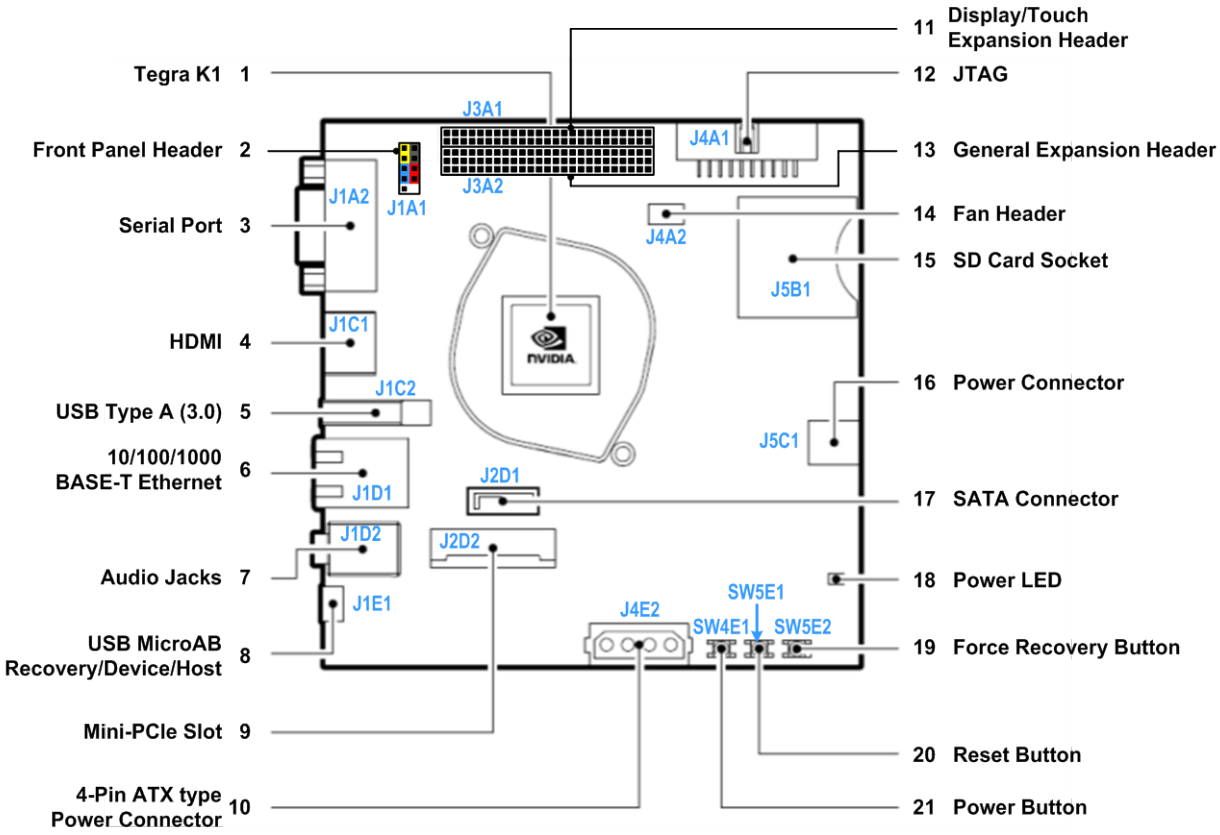


Figure 1. Jetson TK1 Developer Board Placement



1	Tegra K1	Applications Processor
2	Front Panel Header	2x5 0.1” pitch header (pin 10 removed)
3	Serial Port	D-SUB, 9-pin, right angle
4	HDMI connector	Type A, right angle
5	USB 3.0 connector	Type A, female, right angle
6	10/100/1000 Ethernet Connector	RJ45, right angle, integrated magnetics
7	Audio Jacks	3.5mm stacked: Stereo line out (Green) & mono mic (Pink)
8	USB 2.0 Connector	Micro-AB, female, right angle
9	Mini PCIe Slot	52-pin, Right angle
10	Power Connector	4-pin, ATX type (+5V & +12V)
11	Display/Touch Expansion Header	2x25, 2mm pitch, female header
12	JTAG header	Standard 20-pin header
13	General Expansion Header	3x25, 2mm pitch, female header
14	Fan header	4x1, 2.54mm pitch, w/guide post
15	SD Card connector/cage	Supports card detect & write protect
16	Power jack	Right angle, 5-pin (Accepts 2.1mm inner/5.5mm outer, center power jack
17	SATA connector	Vertical, Standard
18	Power LED	Green
19/20/21	Pushbuttons: Force Recovery/ Reset/Power	Normally open

2.0 Jetson Custom Expansion Interface Connections

The Jetson TK1 Developer Kit supports two custom expansion headers:

- Display/Touch Expansion Header, 2mm pitch (2x25 configuration)
- General Expansion Header, 2mm pitch (3x25 configuration)

Notes: Display/Touch & General Expansion Headers form 5x25 pin array. The headers can be used together for a single module, or separately for two modules, but if to be used concurrently, ensure the boards do not physically interfere with each other.

2.1 Display/Touch Expansion Header

The Jetson board includes a 2x25, 2mm pitch female expansion header (reference designator J3A1). This includes interface options for an embedded display and touch controller including:

- LVDS / eDP (4-lane) for embedded displays
- LCD Enable & PWM for embedded backlight control
- GEN1 I2C for LVDS display control
- DP_AUX & HPD for eDP display control & Hot Plug Detect
- SPI & GEN2_I2C (3.3V) options for Touch control
- Touch controller clock, reset & shutdown

Figure 2. Display/Touch Header Connections to Tegra

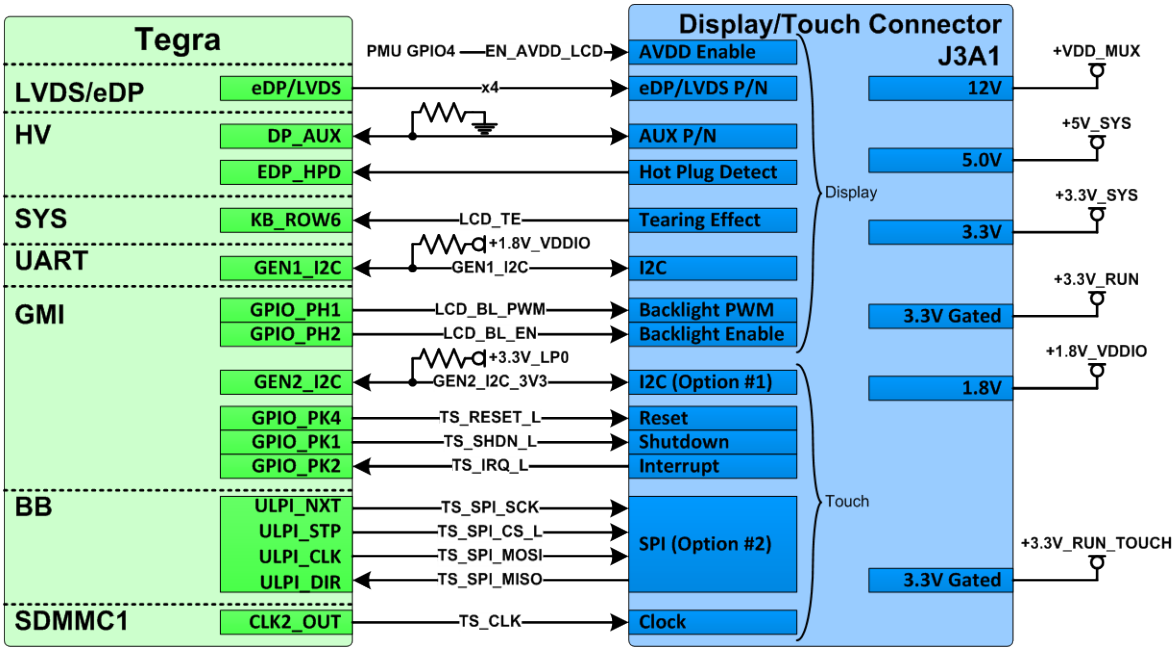


Figure 3. Display/Touch Header Location on Jetson TK1 (J3A1)

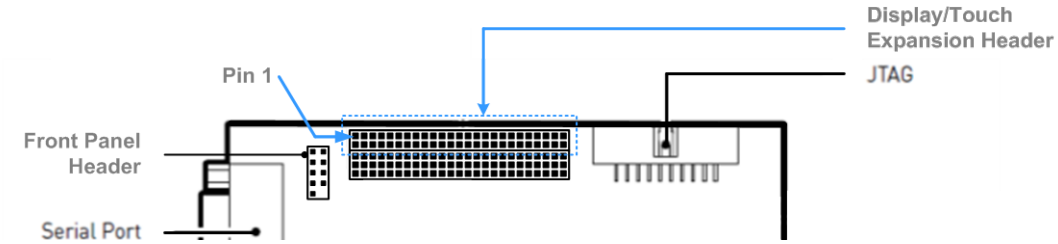


Table 2. Display / Touch Expansion Header Pin Descriptions

Pin #	Signal Name	Tegra K1 Ball	Usage/Description	Type/Dir Default	Associated Voltage Rail	Tegra Pad Type
1	**+5V_SYS**	NA	Main 5V from system	Power		
2	**GND**	NA	Tied to common **GND**	Ground		
3	**+1.8V_VDDIO**	NA	Main 1.8V supply from PMU switcher 5	Power		
4	**TS_SPI_SCK**	**ULPI_NXT**	SPI clock for Touchscreen controller (if SPI used)	Input	+1.8V_VDDIO	ST
5	**TS_SPI_MOSI**	**ULPI_CLK**	SPI MOSI for Touchscreen controller (if SPI used)	Input	+1.8V_VDDIO	ST
6	**TS_SPI_CS_L**	**ULPI_STP**	SPI chip select for Touchscreen controller (if SPI used)	Input	+1.8V_VDDIO	ST
7	**TS_SPI_MISO**	**ULPI_DIR**	SPI MISO for Touchscreen controller (if SPI used)	Output	+1.8V_VDDIO	ST
8	**GND**	NA	Tied to common **GND**	Ground		
9	**GND**	NA	Tied to common **GND**	Ground		
10	**+3.3V_RUN_TOUCH**	NA	AMS PMIC LDO9	Power		
11	**TS_SHDN_L**	**GPIO_PK1**	Shutdown control for Touchscreen controller	Input	+1.8V_VDDIO	CZ
12	**TS_CLK**	**CLK2_OUT**	Clock for Touchscreen controller	Input	+1.8V_VDDIO	ST
13	**TS_RESET_L**	**GPIO_PK4**	Reset for Touchscreen controller	Input	+1.8V_VDDIO	CZ
14	**GND**	NA	Tied to common **GND**	Ground		
15	**GND**	NA	Tied to common **GND**	Ground		
16	**+3.3V_SYS**	NA	Main 3.3V supply	Power		
17	**GPIO_PK2**	**GPIO_PK2**	Available GPIO	Output	+1.8V_VDDIO	CZ
18	**GEN2_I2C_SCL_3.3V**	**GEN2_I2C_SCL**	3.3V I2C IF (Pulled up to **+3.3V_LP0**)	Input, Open Drain	+3.3V_LP0	DD
19	**+1.8V_VDDIO**	NA	Main 1.8V supply from PMU switcher 5	Power		
20	**GEN2_I2C_SDA_3.3V**	**GEN2_I2C_SDA**	3.3V I2C IF (Pulled up to **+3.3V_LP0**)	Bidir, Open Drain	+3.3V_LP0	DD
21	**GEN1_I2C_SCL**	**GEN1_I2C_SCL**	1.8V I2C (Pulled to **+1.8V_VDDIO**)	Input, Open Drain	+1.8V_VDDIO	DD
22	**+3.3V_RUN**	NA	+3.3V rail that is off in LP0	Power		
23	**GEN1_I2C_SDA**	**GEN1_I2C_SDA**	1.8V I2C (Pulled to **+1.8V_VDDIO**)	Bidir, Open Drain	+1.8V_VDDIO	DD

Pin #	Signal Name	Tegra K1 Ball	Usage/Description	Type/Dir Default	Associated Voltage Rail	Tegra Pad Type
24	**EN_AVDD_LCD**	NA	Enable for Embedded display from PMU **GPIO4**	Input		
25	**+VDD_MUX**	NA	Main 12V from Jack	Power		
26	**GND**	NA	Tied to common **GND**	Ground		
27	**EN_VDD_BL**	**DAP3_DOUT**	Backlight supply enable	Input	+1.8V_VDDIO	ST
28	**DP_AUX_P**	**DP_AUX_P**	eDP AUX control interface (+)	Bidir	+1.05V_RUN_AVDD	LVDS/DP
29	**GND**	NA	Tied to common **GND**	Ground		
30	**DP_AUX_N**	**DP_AUX_N**	eDP AUX control interface (-)	Bidir	+1.05V_RUN_AVDD	LVDS/DP
31	**LVDS_TXD0_P**	**LVDS_TXD0_P**	LVDS Data lane 0 (+) or eDP Data lane 2 (+)	Input	+1.05V_RUN_AVDD	LVDS/DP
32	**GND**	NA	Tied to common **GND**	Ground		
33	**LVDS_TXD0_N**	**LVDS_TXD0_N**	LVDS Data lane 0 (-) or eDP Data lane 2 (-)	Input	+1.05V_RUN_AVDD	LVDS/DP
34	**LVDS_TXD1_P**	**LVDS_TXD1_P**	LVDS Data lane 1 (+) or eDP Data lane 1 (+)	Input	+1.05V_RUN_AVDD	LVDS/DP
35	**GND**	NA	Tied to common **GND**	Ground		
36	**LVDS_TXD1_N**	**LVDS_TXD1_N**	LVDS Data lane 1 (-) or eDP Data lane 1 (-)	Input	+1.05V_RUN_AVDD	LVDS/DP
37	**LVDS_TXD3_P**	**LVDS_TXD3_P**	LVDS Data lane 3 (+) – Not used for eDP	Input	+1.05V_RUN_AVDD	LVDS/DP
38	**GND**	NA	Tied to common **GND**	Ground		
39	**LVDS_TXD3_N**	**LVDS_TXD3_N**	LVDS Data lane 3 (-) – Not used for eDP	Input	+1.05V_RUN_AVDD	LVDS/DP
40	**LVDS_TXD2_P**	**LVDS_TXD2_P**	LVDS Data lane 2 (+) or eDP Data lane 0 (+)	Input	+1.05V_RUN_AVDD	LVDS/DP
41	**GND**	NA	Tied to common **GND**	Ground		
42	**LVDS_TXD2_N**	**LVDS_TXD2_N**	LVDS Data lane 2 (-) or eDP Data lane 0 (-)	Input	+1.05V_RUN_AVDD	LVDS/DP
43	**LVDS_TXD4_N**	**LVDS_TXD4_N**	LVDS Clock lane (+) or eDP Data lane 3 (+)	Input	+1.05V_RUN_AVDD	LVDS/DP
44	**GND**	NA	Tied to common **GND**	Ground		
45	**LVDS_TXD4_P**	**LVDS_TXD4_P**	LVDS Clock lane (-) or eDP Data lane 3 (-)	Input	+1.05V_RUN_AVDD	LVDS/DP
46	**EDP_HPD**	**DP_HPD**	eDP display Hot Plug Detect input	Output	+3.3V_LP0	ST
47	**GND**	NA	Tied to common **GND**	Ground		
48	**LCD_BL_EN**	**GPIO_PH2**	Backlight enable	Input	+1.8V_VDDIO	CZ
49	**LCD_TE**	**KB_ROW6**	Tearing Effect from embedded display (if supported)	Output	+1.8V_VDDIO	ST
50	**LCD_BL_PWM**	**GPIO_PH1**	Backlight PWM	Input	+1.8V_VDDIO	CZ

Notes:
- In the Type/Dir column, Output is from Module. Input is to Module. Bidir is for Bidirectional signals.
- See Section 5.0 for details on the standard Tegra Pad Types (ST, CZ & DD)

2.1.1 Display Guidelines

Jetson supports up to a 4-lane single-link LVDS interface or up to a 4-lane eDP interface. The maximum resolution supported with LVDS is 1920x1200 @ 60fps (24bpp color depth). With eDP, the maximum supported using the full 4 lanes is 3200x2000 @ 60fps. LVDS and eDP are multiplexed on the same pins. See LVDS/eDP Pin Assignment Options table below for pin assignments for each interface.

Table 3. eDP/LVDS Pin Assignment Options

Tegra Ball	LVDS (3-lane)	LVDS (4 lane)	eDP
LVDS0_TXD0_P/N	LVDS lane 0	LVDS lane 0	eDP lane 2
LVDS0_TXD1_P/N	LVDS lane 1	LVDS lane 1	eDP lane 1
LVDS0_TXD2_P/N	LVDS lane 2	LVDS lane 2	eDP lane 0
LVDS0_TXD3_P/N	N/A	LVDS lane 3	N/A
LVDS0_TXD4_P/N	LVDS clock lane	LVDS clock lane	eDP lane 3

Figure 4: eDP 4-Lane Connection Example

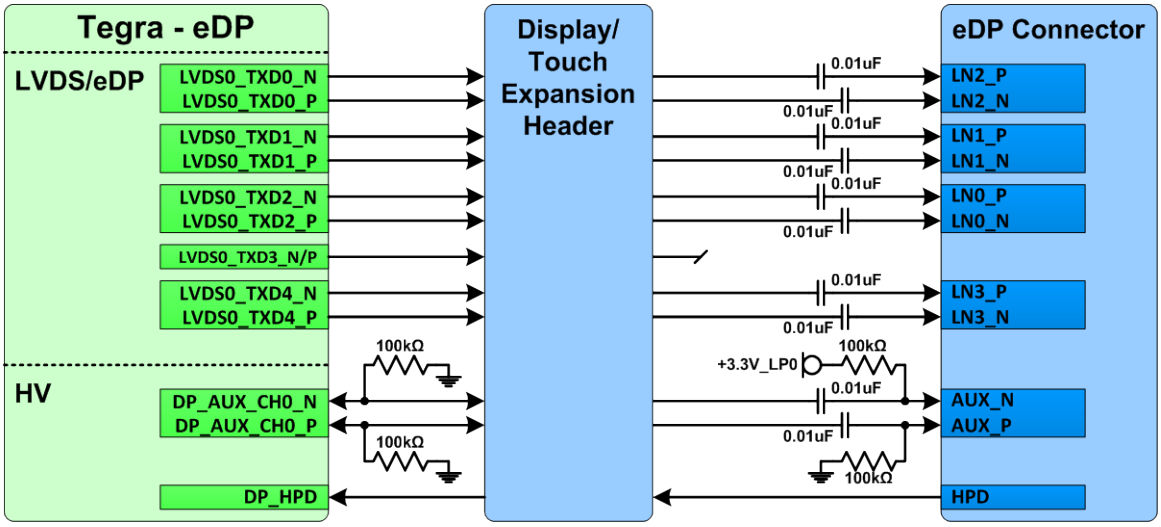
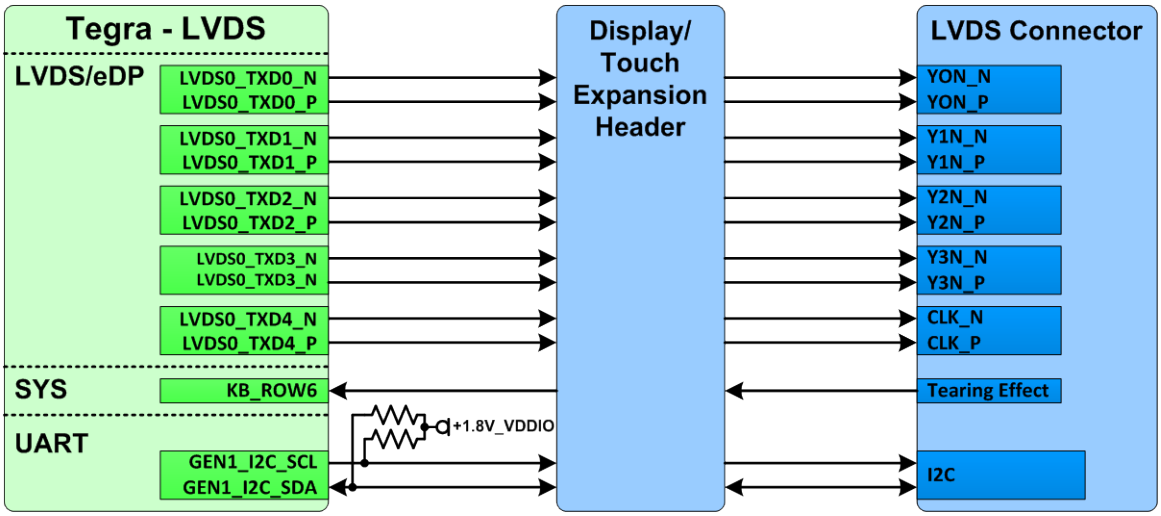


Figure 5: LVDS 4-Lane Connection Example



eDP Design Guidelines

Table 4. eDP (RBR / HBR) Main Link Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate (per data lane)	5.4	Gbps	
Min UI	185	ps	
Number of Loads	1	load	
Topology			Point-Point, Differential, Unidirectional
Termination	100	Ω	On die at TX/RX
Reference plane	GND		
Max PCB breakout length	7.63	mm	
Trace Impedance Diff pair / Single Ended	90 / 45-60	Ω	+15%
Max trace length from Tegra TX pin to connector	215 (1480)	mm (ps)	See Note 1. 175ps/inch delay assumed
Max number of signal vias	4		
PCB pair-to-pair spacing	3x	dielectric height	3x of the thinner of above and below
PCB main link to AUX Spacing	3x	dielectric height	3x of the thinner of above and below
Max stub length on the Vias Allowed			Rout below core to minimize stub length
Max Intra-pair (within pair) Skew	1	ps	See Note 1 & 2
Max Inter-pair (pair-pair) Skew	150	ps	See Note 1 & 2
Max GND transition via distance	< 1x	diff pair pitch	For signals switching reference layers, add symmetrical ground stitching via near signal vias.

Parameter	Requirement	Units	Notes
AC coupling cap	100	nF	Discrete 0402
If routing to eDP device includes a flex or 2nd PCB, the max trace & skew calculations must include all the PCBs/flex routing			
Keep critical eDP related traces including differential clock/data traces away from other signal traces or unrelated power traces/areas or power supply components			

Note:
1. Max Trace Delay & Max Trace Delay Skew matching must include substrate pin delays unless otherwise specified
2. Recommend doing trace length matching to <1ps before vias or any discontinuity to minimize common mode conversion
3. Asymmetric Stripline used on main board. Same configuration is recommended for module routing.

Table 5. eDP Auxiliary Channel Signal Routing Requirements

Parameter	Requirement	Units	Notes
Termination, Reference plane, Max breakout, Impedance, Max trace length, Max Vias	Same as Main Link		
PCB pair-to-pair spacing	2x	dielectric height	
Max Intra-pair (within pair) Skew	Same as Main Link		
Max Inter-pair (pair-pair) Skew	No requirement		

Note: Asymmetric Stripline used on main board. Same configuration is recommended for module routing.

Table 6. eDP Interface Package & Jetson TK1 PCB Trace Delays

Signal	Package Delay (ps)	Jetson PCB Delay (ps)	Pkg + PCB Delay (ps)	Max Trace Delay Allowed (ps)	Available Max Trace Delay for Module (ps)
LVDS0_TXD0_N	50	460	510	1480	970
LVDS0_TXD0_P	51	459	510	1480	970
LVDS0_TXD1_N	44	453	497	1480	983
LVDS0_TXD1_P	45	452	497	1480	983
LVDS0_TXD2_N	30	438	468	1480	1012
LVDS0_TXD2_P	30	437	467	1480	1013
LVDS0_TXD3_N	46	467	513	1480	967
LVDS0_TXD3_P	47	467	514	1480	966
LVDS0_TXD4_N	38	457	495	1480	985
LVDS0_TXD4_P	38	456	494	1480	986
DP_AUX_P	75	379	454	1480	1026
DP_AUX_P	76	379	455	1480	1025

LVDS Design Guidelines

Table 7. LVDS Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency / Bit Rate	135 / 945	MHz / Mbps	
Number of Loads	1	load	
Topology			Point-Point or Multi-drop, Differential, Unidirectional
Termination	100	Ω	At the receiver (on die or on board)
Reference Plane	GND		
Trace Impedance Diff pair / Single Ended	90 / 45-55	Ω	+15%
Max Trace Length	10 (1700)	In (ps)	See Note 1
PCB pair-to-pair spacing	3x	dielectric height	3x of the thinner of above and below
Max Intra-pair (within pair) Skew	5	ps	See Note 1
Max Inter-pair (pair-pair) Skew	100	ps	See Note 1
If routing to LVDS device includes a flex or 2nd PCB, the max trace & skew calculations must include all the PCBs/flex routing			
Keep critical LVDS related traces including differential clock/data traces away from other signal traces or unrelated power traces/areas or power supply components			

Note: 1. Include Package & PCB routing delays for Max trace delays and max trace delay skew parameters.
2. Asymmetric Stripline used on main board. Same configuration is recommended for module routing.

Table 8. LVDS Interface Package & Jetson TK1 PCB Trace Delays

Signal	Package Delay (ps)	Jetson PCB Delay (ps)	Pkg + PCB Delay (ps)	Max Trace Delay Allowed (ps)	Available Max Trace Delay for Module (ps)
LVDS0_TXD0_N	50	460	510	1700	1190
LVDS0_TXD0_P	51	459	510	1700	1190
LVDS0_TXD1_N	44	453	497	1700	1203
LVDS0_TXD1_P	45	452	497	1700	1203
LVDS0_TXD2_N	30	438	468	1700	1232
LVDS0_TXD2_P	30	437	467	1700	1233
LVDS0_TXD3_N	46	467	513	1700	1187
LVDS0_TXD3_P	47	467	514	1700	1186
LVDS0_TXD4_N	38	457	495	1700	1205
LVDS0_TXD4_P	38	456	494	1700	1206

2.1.2 Touch Guidelines

Table 9. SPI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency	50	MHz	
Configuration / Device Organization	4	load	
Max Loading (total of all loads)	15	pF	
Reference plane	**GND**		
Breakout Region Impedance	Minimum width & spacing		
Max PCB breakout delay	75	ps	
Trace Impedance	50 – 60	Ω	+15%
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Trace spacing Microstrip / Stripline	4x / 3x	dielectric	
Max Trace Delay	890 (~5)	ps (in)	See Note 2
Max Trace Delay Skew between **MOSI** (**DOUT**), **MISO** (**DIN**) & **CS** to **SCK**	50	ps	

Note: 1. Up to 4 signal vias can share a single GND return via
2. Include Package & PCB routing delays for Max trace delays and max trace delay skew parameters.

Table 10. Touch SPI Interface Package & Jetson TK1 PCB Trace Delays

Signal	Package Delay (ps)	Jetson PCB Delay (ps)	Pkg + PCB Delay (ps)	Max Trace Delay Allowed (ps)	Available Max Trace Delay for Module (ps)
TS_SPI_SCK	71	521	591	890	299
TS_SPI_MOSI	80	490	570	890	320
TS_SPI_MISO	56	519	575	890	315
TS_SPI_CS_L	76	475	550	890	340

2.1.3 I2C Design Guidelines

Table 11. I2C Interface Signal Routing Requirements for Standard & Fast Modes

Parameter		Requirement	Units	Notes
Max Frequency	Standard / Fast Mode	100 / 400	kHz	See Note 1
Max Loading	Standard / Fast Mode	400	pF	Total of all loads
Reference plane		**GND** or **PWR**		
Trace Impedance		50 – 60	Ω	+15%
Trace Spacing		1x	dielectric	
Max Trace Delay	Standard Mode Fast Mode, Fast Mode Plus	3400 (~20) 1700 (~10)	ps (in)	Include Package & PCB routing delays

Note:
1. For I2C interfaces that are pulled up to 1.8V, disable the OD (Open Drain) option for these pads. For I2C interfaces that are pulled up to 2.8V or higher, enable the OD (Open Drain) option.
2. Max Trace Delay must include Tegra K1 package pin delays, Jetson TK1 PCB trace delays & Module trace delays.
3. Due to the Jetson TK1 trace routing on GEN1_I2C, the interface is limited to Standard Mode if used on a module.

Table 12. GEN2 I2C Interface Package & Jetson TK1 PCB Trace Delays

Signal	Package Delay (ps)	Jetson PCB Delay (ps)	Pkg + PCB Delay (ps)	Max Trace Delay Allowed (ps)		Available Max Trace Delay for Module (ps)	
				Standard Mode	Fast Mode	Standard Mode	Fast Mode
GEN2_I2C_SCL_3.3V	74	354	428	3400	1700	2972	1272
GEN2_I2C_SDA_3.3V	87	337	424	3400	1700	2976	1276

2.2 General Expansion Header

Jetson includes a 3x25, 2mm pitch female expansion header (reference designator J3A2), providing a number of interfaces to connect to Cameras and other peripherals including:

- CSI x4 lane IF for Camera 1 & x1 lane IF for Camera 2
- CAM_I2C, Clock & Control GPIOs for both Cameras
- HSIC
- GEN1_I2C
- UART2
- GPIO_PU[6:0]
- Power-on, Reset & Force Recovery signals: – Used for flashing initial SW image (or reflashing if corrupt)
- UART1 & PWR_I2C: Used for Nvidia debug. Should not be used on module designs

Figure 6: General Expansion Header Connections

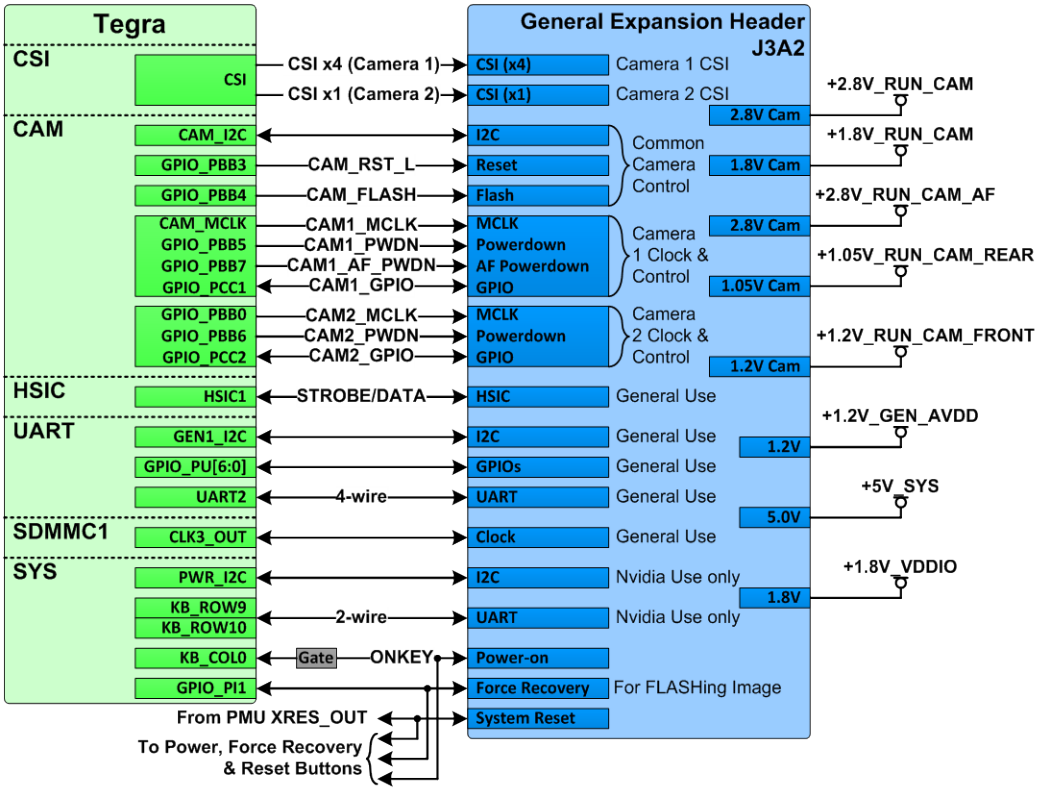


Figure 7. General Expansion Header Location on Jetson TK1 (J3A2)

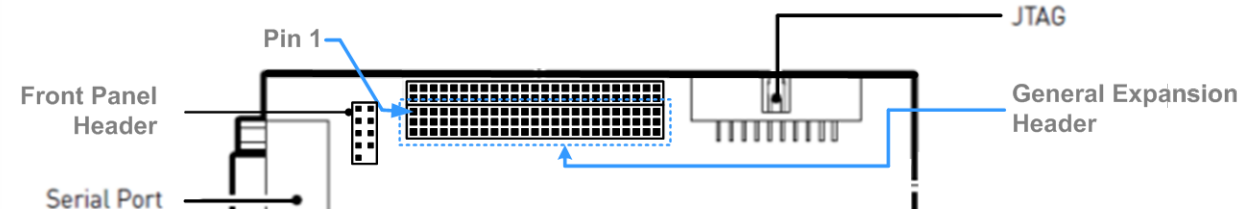


Table 13. General Expansion Header Pin Descriptions

Pin #	Signal Name	Tegra K1 Ball	Usage/Description	Type/Dir Default	Associated Voltage Rail	Tegra Pad Type
1	**+5V_SYS**	N/A	Main 5V from system	Power	---	---
2	**CAM2_PWDN**	**GPIO_PBB6**	Power Down for Camera 2	Input	+1.8V_RUN_CAM	ST
3	**+1.05V_RUN_CAM_REAR**	N/A	AMS PMIC LDO7 for Camera 1	Power	---	---
4	**CAM2_MCLK**	**GPIO_PBB0**	Master Reference Clock for Camera 2	Input	+1.8V_RUN_CAM	ST
5	**CAM_RST_L**	**GPIO_PBB3**	Reset for Camera(s)	Input	+1.8V_RUN_CAM	ST
6	**+2.8V_RUN_CAM**	N/A	AMS PMIC LDO4 for Camera(s)	Power	---	---
7	**CAM2_GPIO**	**GPIO_PCC2**	GPIO for Camera 2	Bidir	+1.8V_RUN_CAM	ST

Pin #	Signal Name	Tegra K1 Ball	Usage/Description	Type/Dir Default	Associated Voltage Rail	Tegra Pad Type
8	**CAM_I2C_SDA**	**CAM_I2C_SDA**	I2C Data for Camera(s)	Bidir, Open Drain	+1.8V_RUN_CAM	DD
9	**GND**	N/A	Tied to common **GND**	Ground	---	---
10	**GND**	N/A	Tied to common **GND**	Ground	---	---
11	**CAM_I2C_SCL**	**CAM_I2C_SCL**	I2C Clock for Camera(s)	Input, Open Drain	+1.8V_RUN_CAM	DD
12	**CSI_A_CLK_P**	**CSI_A_CLK_P**	CSI Clock (+) for Camera 1	Output	+1.2V_GEN_AVDD	CSI
13	**CSI_E_CLK_N**	**CSI_E_CLK_N**	CSI Clock (-) for Camera 2	Output	+1.2V_GEN_AVDD	CSI
14	**GND**	N/A	Tied to common **GND**	Ground	---	---
15	**CSI_A_CLK_N**	**CSI_A_CLK_N**	CSI Clock (-) for Camera 1	Output	+1.2V_GEN_AVDD	CSI
16	**CSI_E_CLK_P**	**CSI_E_CLK_P**	CSI Clock (+) for Camera 2	Output	+1.2V_GEN_AVDD	CSI
17	**CSI_E_D0_N**	**CSI_E_D0_N**	CSI Data Lane 0 (-) for Camera 2	Output	+1.2V_GEN_AVDD	CSI
18	**GND**	N/A	Tied to common **GND**	Ground	---	---
19	**GND**	N/A	Tied to common **GND**	Ground	---	---
20	**CSI_E_D0_P**	**CSI_E_D0_P**	CSI Data Lane 0 (+) for Camera 2	Output	+1.2V_GEN_AVDD	CSI
21	**CSI_A_D1_N**	**CSI_A_D1_N**	CSI Data Lane 1 (-) for Camera 1	Output	+1.2V_GEN_AVDD	CSI
22	**+1.2V_RUN_CAM_FRONT**	N/A	AMS PMIC LDO5 for Camera 2	Power	---	---
23	**GND**	N/A	Tied to common **GND**	Ground	---	---
24	**CSI_A_D1_P**	**CSI_A_D1_P**	CSI Data Lane 1 (+) for Camera 1	Output	+1.2V_GEN_AVDD	CSI
25	**+2.8V_RUN_CAM_AF**	N/A	AMS PMIC LDO10 for Camera 1	Power	---	---
26	**+1.8V_VDDIO**	N/A	AMS Switcher 5	Power	---	---
27	**GND**	N/A	Tied to common **GND**	Ground	---	---
28	**+1.2V_GEN_AVDD**	N/A	AMS PMIC LDO2, used to sync HSIC rails	Power	---	---
29	**+1.8V_RUN_CAM**	N/A	AMS PMIC LDO1	Power	---	---
30	**CSI_A_D0_N**	**CSI_A_D0_N**	CSI Data Lane 0 (-) for Camera 1	Output	+1.2V_GEN_AVDD	CSI
31	**HSIC1_STROBE**	**HSIC1_STROBE**	HSIC Strobe	Bidir	+1.2V_GEN_AVDD	HSIC
32	**GND**	N/A	Tied to common **GND**	Ground	---	---
33	**CSI_A_D0_P**	**CSI_A_D0_P**	CSI Data Lane 0 (+) for Camera 1	Output	+1.2V_GEN_AVDD	CSI
34	**GND**	N/A	Tied to common **GND**	Ground	---	
35	**HSIC1_DATA**	**HSIC1_DATA**	HSIC Data	Bidir	+1.2V_GEN_AVDD	HSIC
36	**GND**	N/A	Tied to common **GND**	Ground	---	---
37	**+1.8V_VDDIO**	N/A	AMS Switcher 5	Power	---	---
38	**GND**	N/A	Tied to common **GND**	Ground	---	---
39	**CSI_B_D1_N**	**CSI_B_D1_N**	CSI Data Lane 3 (-) for Camera 1	Output	+1.2V_GEN_AVDD	CSI
40	**GPIO_PU0**	**GPIO_PU0**	**GPIO PU0**: Available for general use	Bidir	+1.8V_VDDIO	ST

Pin #	Signal Name	Tegra K1 Ball	Usage/Description	Type/Dir Default	Associated Voltage Rail	Tegra Pad Type
41	**BR_UART1_TXD**	**KB_ROW9**	For PM342 style Laguna FFD header	Input	+1.8V_VDDIO	---
42	**CSI_B_D1_P**	**CSI_B_D1_P**	CSI Data Lane 3 (+) for Camera 1	Output	+1.2V_GEN_AVDD	---
43	**GPIO_PU1**	**GPIO_PU1**	**GPIO PU1**: Available for general use	Bidir	+1.8V_VDDIO	ST
44	**BR_UART1_RXD**	**KB_ROW10**	For PM342 style Laguna FFD header	Output	+1.8V_VDDIO	---
45	**GND**	N/A	Tied to common **GND**	Ground	---	---
46	**GPIO_PU2**	**GPIO_PU2**	**GPIO PU2**: Available for general use	Bidir	+1.8V_VDDIO	ST
47	**GND**	N/A	Tied to common **GND**	Ground	---	---
48	**CSI_B_D0_P**	**CSI_B_D0_P**	CSI Data Lane 2 (+) for Camera 1	Output	+1.2V_GEN_AVDD	CSI
49	**GPIO_PU3**	**GPIO_PU3**	**GPIO PU3**: Available for general use	Bidir	+1.8V_VDDIO	ST
50	**PWR_I2C_SCL**	**PWR_I2C_SCL**	Power I2C Clock: For Nvidia use only	Input, Open Drain	+1.8V_VDDIO	DD
51	**CSI_B_D0_N**	**CSI_B_D0_N**	CSI Data Lane 2 (-) for Camera 1	Output	+1.2V_GEN_AVDD	CSI
52	**GPIO_PU4**	**GPIO_PU4**	**GPIO PU4**: Available for general use	Bidir	+1.8V_VDDIO	ST
53	**PWR_I2C_SDA**	**PWR_I2C_SDA**	Power I2C Data: For Nvidia use only	Bidir, Open Drain	+1.8V_VDDIO	DD
54	**GND**	N/A	Tied to common **GND**	Ground	---	---
55	**GPIO_PU5**	**GPIO_PU5**	**GPIO PU5**: Available for general use	Bidir	+1.8V_VDDIO	ST
56	**GEN1_I2C_SCL**	**GEN1_I2C_SCL**	GEN1 I2C Clock: 1.8V I2C IF available for general use	Input, Open Drain	+1.8V_VDDIO	DD
57	**CAM1_GPIO**	**GPIO_PCC1**	GPIO for Camera 1	Bidir	+1.8V_RUN_CAM	ST
58	**GPIO_PU6**	**GPIO_PU6**	**GPIO PU6**: Available for general use	Bidir	+1.8V_VDDIO	ST
59	**GEN1_I2C_SDA**	**GEN1_I2C_SDA**	GEN1 I2C Data: 1.8V I2C IF available for general use	Bidir, Open Drain	+1.8V_VDDIO	DD
60	**CAM1_AF_PWDN**	**GPIO_PBB7**	Autofocus Powerdown for Camera 1	Input	+1.8V_RUN_CAM	ST
61	**ONKEY_L**	**KB_COL0 (indirect)**	Power On (to PMU ONKEY & gated version to Tegra)	Bidir	+2.5V_AON_RTC	---
62	**GND**	N/A	Tied to common **GND**	Ground	---	---
63	**CAM_FLASH**	**GPIO_PBB4**	Flash enable to control camera flash driver	Input	+1.8V_RUN_CAM	ST
64	**PMU_RESET_IN_L**	N/A	System Reset signal	Bidir	+2.5V_AON_RTC	---
65	**UART2_RXD**	**UART2_RXD**	UART 2 Receive	Output	+1.8V_VDDIO	ST
66	**CAM1_PWDN**	**GPIO_PBB5**	Powerdown for Camera 1	Input	+1.8V_RUN_CAM	ST
67	**FORCE_RECOVERY_L**	**GPIO_PI1 (indirect)**	Force Recovery: To enter Forced Recovery mode	Bidir	+2.5V_AON_RTC	---
68	**UART2_TXD**	**UART2_TXD**	UART 2 Transmit	Input	+1.8V_VDDIO	ST
69	**CAM1_MCLK**	**CAM_MCLK**	Master Reference Clock for Camera 1	Input	+1.8V_RUN_CAM	ST
70	**CLK3_OUT**	**CLK3_OUT**	Clock 3 Output: Available clock source from Tegra K1	Input	+1.8V_RUN_CAM	ST
71	**UART2_CTS_L**	**UART2_CTS_L**	UART 2 Clear to Send	Output	+1.8V_VDDIO	ST

Pin #	Signal Name	Tegra K1 Ball	Usage/Description	Type/Dir Default	Associated Voltage Rail	Tegra Pad Type
72	NC	N/A	Not used	---	---	---
73	**GND**	N/A	Tied to common **GND**	Ground	---	---
74	**UART2_RTS_L**	**UART2_RTS_L**	UART 2 Request to Send	Input	+1.8V_VDDIO	ST
75	NC	N/A	Not used	---	---	---

Notes:
- In the Type/Dir column, Output is from Module. Input is to Module. Bidir is for Bidirectional signals.
- See Section 5.0 for details on the standard Tegra Pad Types (ST & DD)

2.2.1 Camera/CSI Guidelines

Figure 8: Dual Camera Connection Example

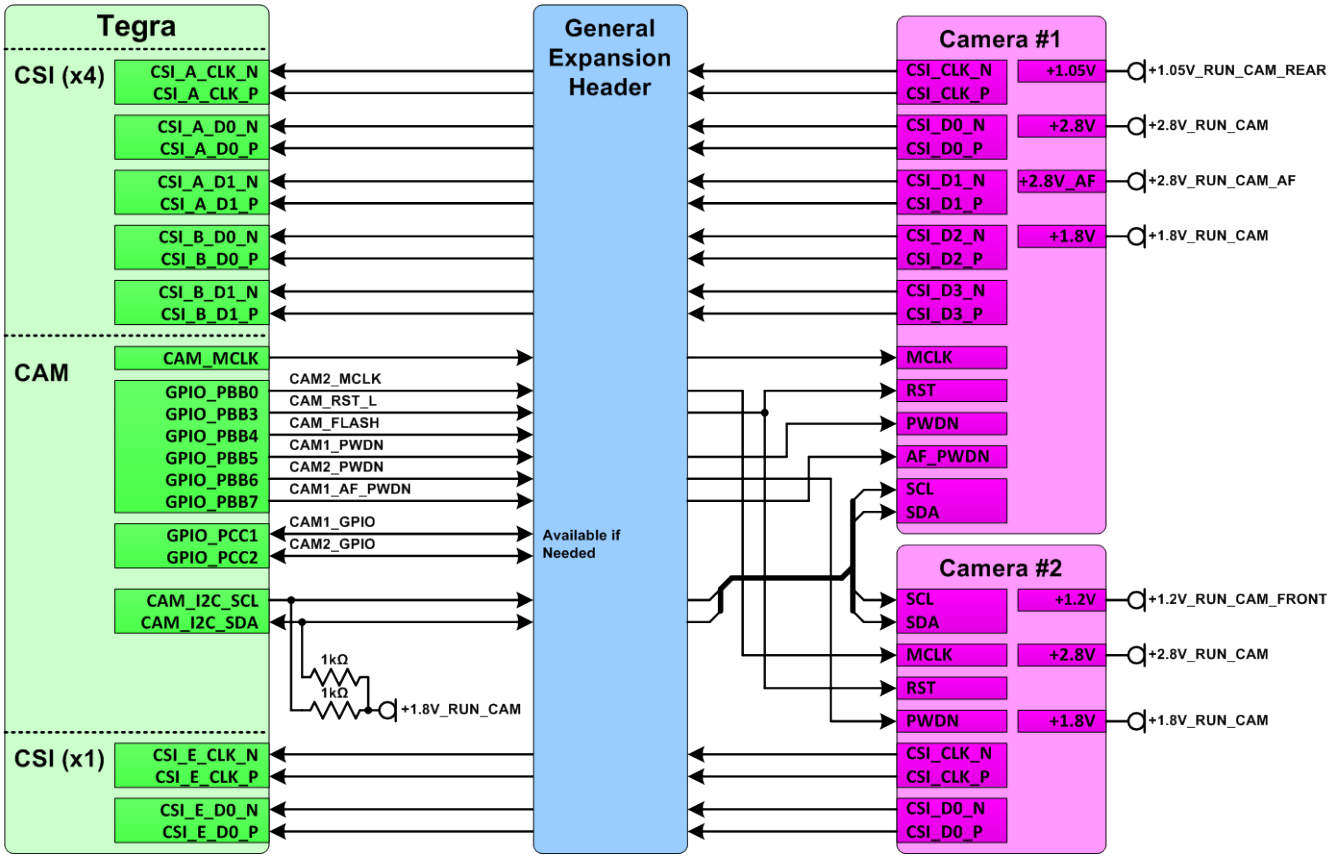


Table 14. MIPI CSI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency/Data Rate (per data lane)	750 / 1500	MHz/Mbps	
Number of Loads / loading per pin	1 / 10	Load / pf	
Reference plane	**GND** or **PWR**		See Note 1
Breakout Region Impedance Diff pair / Single Ended	90 / 45-55	Ω	+15%
Max PCB breakout delay	48	ps	
Trace Impedance Diff pair / Single Ended	90 / 45-55	Ω	
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 2
Trace spacing Microstrip / Stripline	2x / 2x	dielectric	
Max Trace Delay	1620	ps	See Note 3
Max Intra-pair Skew	1	ps	See Note 3
Max Trace Delay Skew between **DQ** & **CLK**	10	ps	See Note 3

Note:
1. If **PWR**, 0.01uF decoupling cap required for return current
2. Up to 4 signal vias can share a single **GND** return via
3. Include Package & PCB routing delays for Max trace delays and max trace delay skew parameters.

Table 15. CSI Interface Package & Jetson TK1 PCB Trace Delays

Signal	Package Delay (ps)	Jetson PCB Delay (ps)	Pkg + PCB Delay (ps)	Max Trace Delay Allowed (ps)	Available Max Trace Delay for Module (ps)
CSI_A_CLK_N	46	567	613	1620	1007
CSI_A_CLK_P	46	567	613	1620	1007
CSI_A_D0_N	81	531	612	1620	1008
CSI_A_D0_P	81	530	611	1620	1009
CSI_A_D1_N	61	560	621	1620	999
CSI_A_D1_P	62	559	621	1620	999
CSI_B_D0_N	78	558	636	1620	984
CSI_B_D0_P	79	556	635	1620	985
CSI_B_D1_N	66	572	638	1620	982
CSI_B_D1_P	67	572	639	1620	981
CSI_E_CLK_N	67	391	458	1620	1162
CSI_E_CLK_P	68	390	458	1620	1162
CSI_E_D0_N	57	398	455	1620	1165
CSI_E_D0_P	58	397	455	1620	1165

2.2.2 HSIC Guidelines

Figure 9: HSIC Connection Example

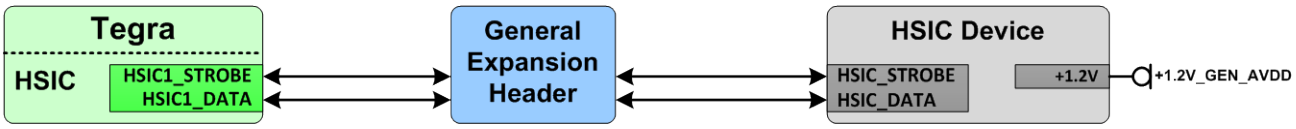


Table 16. HSIC Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency (High Speed) Bit Rate / UI period / Freq.	480 / 2.083 / 240	Mbps / ns / MHz	
Input Buffer Loading	1 – 5	pF	
Reference plane	**GND**		
Max PCB breakout delay	17	ps	
Trace Impedance	50	Ω	+15%
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Trace spacing Microstrip / Stripline	4x / 3x	dielectric	
Trace Delay Min / Max	133 (667)	Mm (ps)	See Note 2
Max Trace Delay Skew between **HSIC[2:1]_STROBE** & **DATA**	15	ps	See Note 2

Note: 1. Up to 4 signal vias can share a single GND return via
2. Include Package & PCB routing delays for Max trace delays and max trace delay skew parameters.

Table 17. HSIC Interface Package & Jetson TK1 PCB Trace Delays

Signal	Package Delay (ps)	Jetson PCB Delay (ps)	Pkg + PCB Delay (ps)	Max Trace Delay Allowed (ps)	Available Max Trace Delay for Module (ps)
HSIC1_STROBE	55	480	535	667	132
HSIC1_DATA	54	478	532	667	135

2.2.3 I2C Guidelines

See I2C Interface Routing Requirements in section 2.1 (Display / Touch Expansion Header).

Table 18. GEN1 I2C Interface Package & Jetson TK1 PCB Trace Delays

Signal	Package Delay (ps)	Jetson PCB Delay (ps)	Pkg + PCB Delay (ps)	Max Trace Delay Allowed (ps)		Available Max Trace Delay for Module (ps)	
				Std Mode	Fast Mode	Std Mode	Fast Mode
GEN1_I2C_SCL	61	1883	1944	3400	1700	1456	NA
GEN1_I2C_SDA	61	1903	1964	3400	1700	1436	NA

2.3 Front Panel Header Slot

The Jetson board has a 2x5 0.1" pitch header (pin 10 removed). The reference designator for the header is J1A1. The Tegra connections and power rails associated with the Front Panel Header are shown in the figure below.

Figure 10. Front Panel Connections

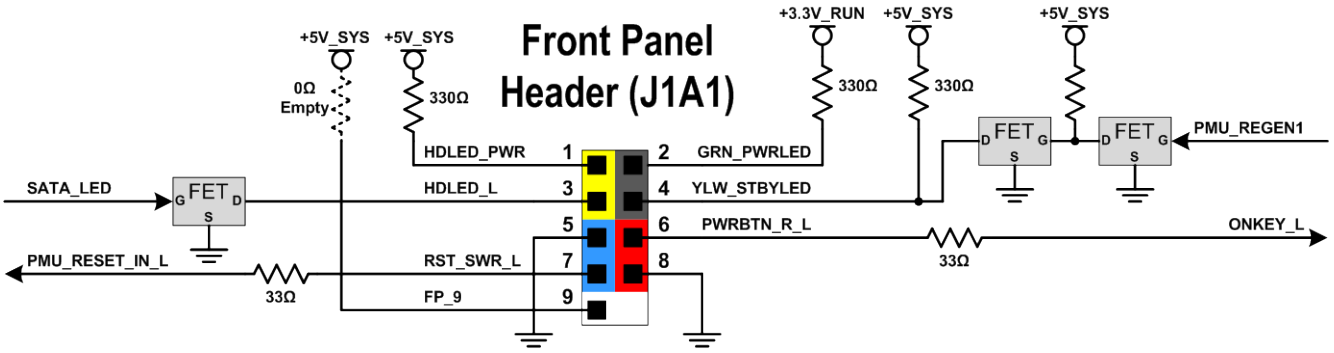


Figure 11. Front Panel Header Location on Jetson TK1 (J3A2)

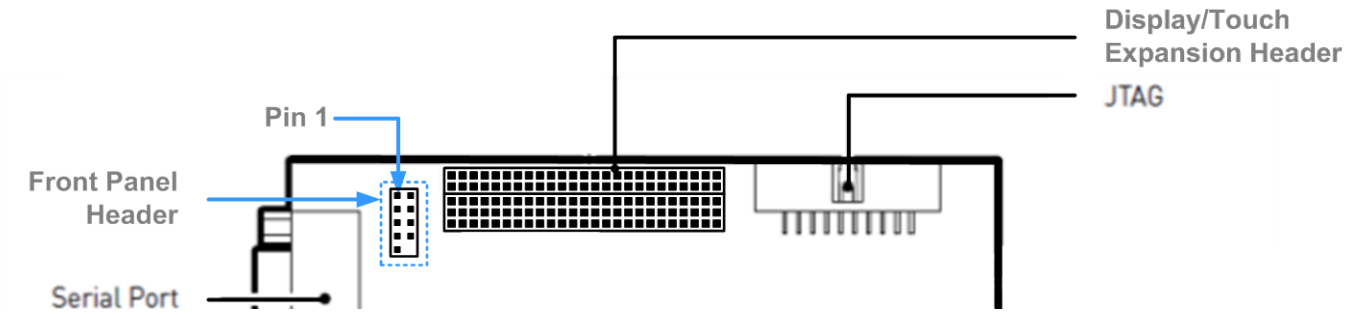


Table 19. Front Panel Header Pin Descriptions

Pin #	Signal Name	Tegra K1 Ball	Usage/Description	Type/Dir Default	Associated Voltage Rail	Tegra Pad Type
1	**HDLED_PWR**	---	Hard Disk LED – Pulled to power rail w/330ohm resistor	LED Power	+5V_SYS	---
2	**GRD_PWRLED**	---	Green Power LED – Pulled to power rail w/330ohm resistor	LED Power	+3.3V_RUN	---
3	**HDLED_L**	DAP1_DOUT (indirect)	Hard Disk (SATA) LED enable	Input	+1.8V_VDDIO	ST
4	**YLW_STBYLED**	---	Yellow Standby LED – Pulled to power rail w/330ohm resistor	LED Power	+5V_SYS	---
5	**GND**	---	Tied to common **GND**	Ground	---	---
6	**PWRBTN_R_L**	---	Power button signal to PMU	Output	+2.5V_AON_RTC	---
7	**RST_SWR_L**	---	Reset signal to PMU	Output	+2.5V_AON_RTC	---

Pin #	Signal Name	Tegra K1 Ball	Usage/Description	Type/Dir Default	Associated Voltage Rail	Tegra Pad Type
8	**GND**	---	Tied to common **GND**	Ground	---	---
9	**FP_9**	---	Optionally tied to power rail	Power	+5V_SYS	---
10	**No Pin (key)**	---	---	---	---	---

Notes:
- In the Type/Dir column, Output is from Module. Input is to Module. Bidir is for Bidirectional signals.
- See Section 5.0 for details on the standard Tegra Pad Types (ST)

3.0 Jetson Standard Expansion Connectors

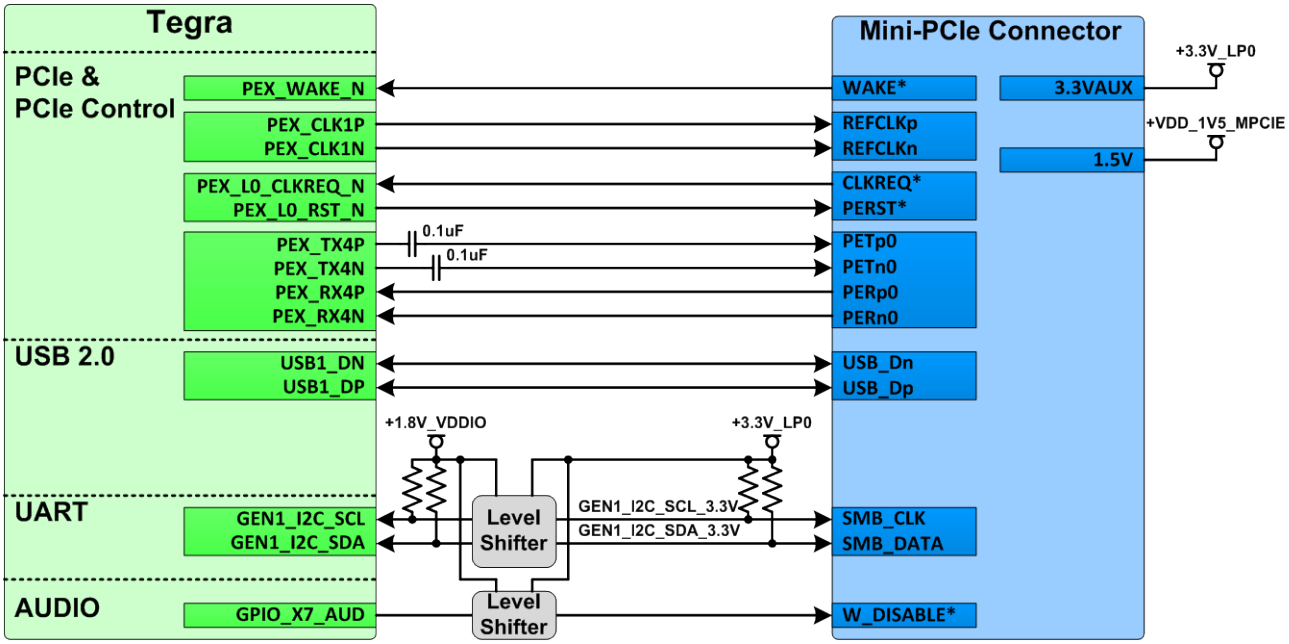
The Jetson TK1 Developer Kit provides a number of standard expansion connectors to support additional functionality beyond what is integrated on the main board. This includes:

- Mini-PCIe Expansion Slot
- USB 2.0: Micro AB Connector
- USB 3.0: Type A Connector
- Ethernet: RJ45 Connector
- SATA: Standard SATA Connector + 1x4 HDD Power Connector (ATX type)
- SD Card Connector/Cage: Supports card detect & write protect
- HDMI: Type A Connector

3.1 Mini-PCIe Expansion Slot

Jetson includes a Mini-PCIe Expansion slot at location J2D2. The connections and power rails associated with the connector are shown in the figure below.

Figure 12. Mini-PCIe Connections to Tegra



Notes: - Device TX AC caps are assumed to be located on the device side of the connector.

Table 20. Mini-PCIe Connector Pin Descriptions

Pin #	Signal Name	Tegra K1 Ball	Usage/Description	Type/Dir Default	Associated Voltage Rail	Tegra Pad Type
1	**WAKE***	**PEX_WAKE_N**	PCIe Wake	Output	+3.3V_LP0	ST
2	**3.3VAUX**		3.3V Supply – To **+3.3V_LP0** (gated **+3.3V_SYS** supply)	Power	---	---
3	**COEX1**		Not Used – No Connect	---	---	---
4	**GND**		Tied to common **GND**	Ground	---	---
5	**COEX2**		Not Used – No Connect	---	---	---
6	**1.5V**		1.5V supply – From APL5910 LDO	Power	---	---
7	**CLKREQ***	**PEX_L0_CLKREQ_N**	PCIe Clock Request	Output	+3.3V_LP0	ST
8	**UIM_PWR**		Not Used – No Connect	---	---	---
9	**GND**		Tied to common **GND**	Ground	---	---
10	**UIM_DATA**		Not Used – No Connect	---	---	---
11	**REFCLKn**	**PEX_CLK1_N**	PCIe Reference Clock (-)	Input	+3.3V_LP0	PCIe
12	**UIM_CLK**		Not Used – No Connect	---	---	---
13	**REFCLKp**	**PEX_CLK1_P**	PCIe Reference Clock (+)	Input	+3.3V_LP0	PCIe
14	**UIM_RESET**		Not Used – No Connect	---	---	---
15	**GND**		Tied to common **GND**	Ground	---	---
16	**UIM_VPP**		Not Used – No Connect	---	---	---
17	**RESERVED**		Not Used – No Connect	---	---	---
18	**GND**		Tied to common **GND**	Ground	---	---
19	**RESERVED**		Not Used – No Connect	---	---	---
20	**W_DISABLE***	**GPIO_X7_AUD (indirect)**	WiFi/WLAN disable – To Tegra GPIO through level translator	Input	+1.8V_VDDIO	ST
21	**GND**		Tied to common **GND**	Ground	---	---
22	**PERST***	**PEX_L0_RST_N**	PCIe Reset	Input	+3.3V_LP0	ST
23	**PERn0**	**PEX_RX4_N**	PCIe Receive (-)	Output	NA (AC Coupled)[2]	PCIe
24	**3.3VAUX**		3.3V Supply – To **+3.3V_LP0** (gated **+3.3V_SYS** supply)	Power	---	
25	**PERp0**	**PEX_RX4_P**	PCIe Receive (+)	Output	NA (AC Coupled)[2]	PCIe
26	**GND**		Tied to common **GND**	Ground	---	---
27	**GND**		Tied to common **GND**	Ground	---	---
28	**1.5V**		1.5V supply – From APL5910 LDO	Power	---	---
29	**GND**		Tied to common **GND**	Ground	---	---
30	**SMB_CLK**	**GEN1_I2C_SCL (indirect)**	SM Bus Clock – To Tegra through 1.8V/3.3V level shifter	Input, Open Drain	+1.8V_VDDIO	DD

Pin #	Signal Name	Tegra K1 Ball	Usage/Description	Type/Dir Default	Associated Voltage Rail	Tegra Pad Type
31	**PETn0**	**PEX_TX4_N**	PCIe Transmit (-)	Input	NA (AC Coupled)	PCIe
32	**SMB_DATA**	**GEN1_I2C_SDA (indirect)**	SM Bus Data – To Tegra through 1.8V/3.3V level shifter	Bidir, Open Drain	+1.8V_VDDIO	DD
33	**PETp0**	**PEX_TX4_P**	PCIe Transmit (+)	Input	NA (AC Coupled)	PCIe
34	**GND**		Tied to common **GND**	Ground	---	---
35	**GND**		Tied to common **GND**	Ground	---	---
36	**USB_Dn**	**USB1_DN**	USB Data (-)	Bidir	+3.3V_LP0	USB
37	**GND**		Tied to common **GND**	Ground	---	---
38	**USB_Dp**	**USB1_DP**	USB Data (+)	Bidir	+3.3V_LP0	USB
39	**3.3VAUX**		3.3V Supply – To **+3.3V_LP0** (gated **+3.3V_SYS** supply)	Power	---	---
40	**GND**		Tied to common **GND**	Ground	---	---
41	**3.3VAUX**		3.3V Supply – To **+3.3V_LP0** (gated **+3.3V_SYS** supply)	Power	---	---
42	**LED_WWAN***		WWAN LED Control. Connected to **+3.3V_LP0** through LED		---	---
43	**GND**		Tied to common **GND**	Ground	---	---
44	**LED_WLAN***		See pin 42 above		---	---
45	**RESERVED**		Not Used – No Connect	---	---	---
46	**LED_WPAN***		See pin 42 above		---	---
47	**RESERVED**		Not Used – No Connect	---	---	---
48	**1.5V**		1.5V supply – From APL5910 LDO	Bidir	---	---
49	**RESERVED**		Not Used – No Connect	---	---	---
50	**GND**		Tied to common **GND**	Ground	---	---
51	**RESERVED**		Not Used – No Connect	---	---	---
52	**3.3VAUX**		3.3V Supply – Connected to **+3.3V_LP0** (gated **+3.3V_SYS**)	Power	---	---

Notes:
1. In the Type/Dir column, Output is from Module. Input is to Module. Bidir is for Bidirectional signals.
2. See Section 5.0 for details on the standard Tegra Pad Types (ST & DD)
3. AC coupling on PERp0/PERn0 on PCIe Mini Card.

3.1.1 PCIe Design Guidelines

Table 21. PCIe Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency / UI Period	5.0 / 200	Gbps / ps	2.5GHz, half-rate architecture
Topology	Point-point		Unidirectional, differential
Configuration / Device Organization	1	Load	
Max Load (per pin)	N/A	pF	See return loss spec in PCIe 2.0 spec
Termination	50	Ω	To **GND** Single Ended for P & N
Reference plane	**GND**		
Breakout RegionWidth & line spacing / pair spacing	4 / 10	Mils	Maximum pair spacing of 500 mils
Trace Impedance differential / Single Ended	90 / 45 – 60	Ω	+15%
Pair to Pair Trace Spacing Stripline / Microstrip	3x / 4x	Dielectric	
Tx to Rx spacing			Recommend Tx & Rx signals routed on separate layers w/**GND** between for isolation. See note 1
Spacing to planes/cap. pads Stripline / Microstrip	3x / 4x	Dielectric	
Max Trace Length/Delay	10” (1700)	in (ps)	For trace with loss <=0.4dB/in @ 2.5GHz. See note 2 & 3
Max Within Pair Trace Delay Skew	1	ps	See note 3 & 4
Max Pair to Pair Trace Delay Skew (RX to RX or TX to TX – Within Link)	600	ps	See note 3 & 4
Trace Width Options	4 / 5 / 6	Mils	See note 2
Max # of Vias TX traces / RX traces	4 / 2		
Routing signals over the antipad	Not allowed		
Serpentine line rule (Min spacing between turns) Stripline / Microstrip	3x / 4x	Dielectric	3x of thinner of above & below
Max distance for DC Blocking capacitor	0.3	in	connector if one exists, or near receiver
PTH (Plated Through-hole) Vias	Keep **GND** via as close as possible		
Ground sliver between BGA pads	Remove ground slivers between BGA pads & feed-through to vias		
Ground plane under DC blocking cap pads	Remove **GND** plane under DC blocking capacitor pads. If board has ICT pads, remove plane under those as well. Void is size of pad + ring equal to dielectric thickness.		

Note:
1. If routing in the same layer is necessary, route group TX & RX separately wo/mixing RX/TX routes & keep distance between nearest TX/RX trace & RX to other signals 3x RX-RX separation
2. Max Trace Delay & Max Trace Delay Skew matching must include Tegra K1 package pin delays, Jetson TK1 PCB trace delays & Module trace delays.
3. Do trace length matching before the vias to transition to different layers or any discontinuity to minimize common mode conversion

Table 22. PCIe Interface Package & Jetson TK1 PCB Trace Delays

Signal	Package Delay (ps)	Jetson PCB Delay (ps)	Pkg + PCB Delay (ps)	Max Trace Delay Allowed (ps)	Available Max Trace Delay for Module (ps)
PEX_TX4_N	39	355	394	1700	1306
PEX_TX4_P	39	354	393	1700	1307
PEX_RX4_N	49	313	362	1700	1338
PEX_RX4_P	48	314	362	1700	1338
PEX_CLK1_N	73	334	407	1700	1293
PEX_CLK1_P	72	335	407	1700	1293

3.1.2 USB 2.0 Design Guidelines

Table 23. USB 2.0 Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Max Frequency (High Speed)	Bit Rate/UI period/Frequency	480/2.083/240	Mbps/ns/MHz	
Max Loading	High Speed / Full Speed / Low Speed	10 / 150 / 600	pF	
Reference plane		**GND**		
Breakout Region Impedance		Min width/spacing		
Trace Impedance	Diff pair / Single Ended	90 / 50	Ω	+15%
Via proximity (Signal to reference)		< 3.8 (24)	mm (ps)	See Note 1
Max Trace Delay		1150 (~7)	ps (in)	See Note 2
Max Intra-Pair Skew between USBx_DP & USBx_DN		7.5	ps	See Note 2

Note:
1. Up to 4 signal vias can share a single **GND** return via.
2. Max Trace Delay & Max Trace Delay Skew matching must include Tegra K1 package pin delays, Jetson TK1 PCB trace delays & Module trace delays.
3. Asymmetric Stripline used on main board. Same configuration is recommended for module routing.

Table 24. USB 2.0 Interface Package & Jetson TK1 PCB Trace Delays

Signal	Package Delay (ps)	Jetson PCB Delay (ps)	Pkg + PCB Delay (ps)	Max Trace Delay Allowed (ps)	Available Max Trace Delay for Module (ps)
USB1_DN	74	480	554	1150	596
USB1_DP	74	472	546	1150	604

3.1.3 I2C Design Guidelines

See I2C Interface Routing Requirements in section 2.1 (Display / Touch Expansion Header).

Table 25. GEN1 I2C Interface Package & Jetson TK1 PCB Trace Delays

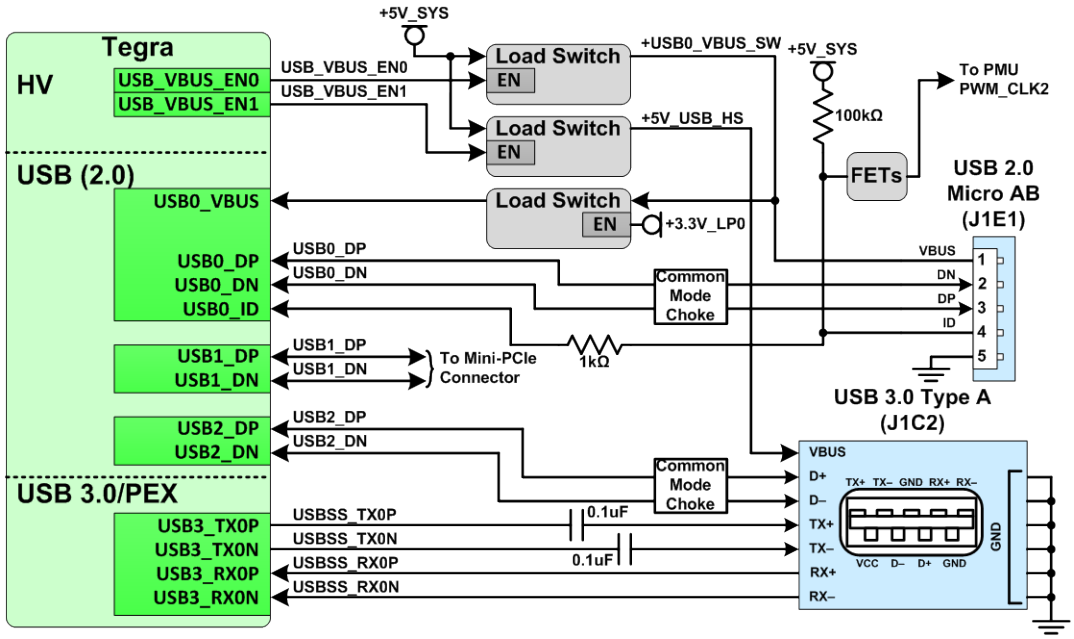
Signal	Package Delay (ps)	Jetson PCB Delay (ps)	Pkg + PCB Delay (ps)	Max Trace Delay Allowed (ps)		Available Max Trace Delay for Module (ps)	
				Standard Mode	Fast Mode	Standard Mode	Fast Mode
GEN1_I2C_SCL	61	1883	1944	3400	1700	1456	NA
GEN1_I2C_SDA	61	1903	1964	3400	1700	1436	NA

3.2 USB Ports

Jetson TK1 supports the following USB ports:

- Micro AB connector supporting Device/Host modes as well as USB Recovery mode (Reference designator J1E1).
- USB 3.0 Type A connector supporting Host mode only (Reference designator J1C2).
- VBUS for both USB connectors is provided by a dedicated TPS2065 Load Switch supporting up to 1A.

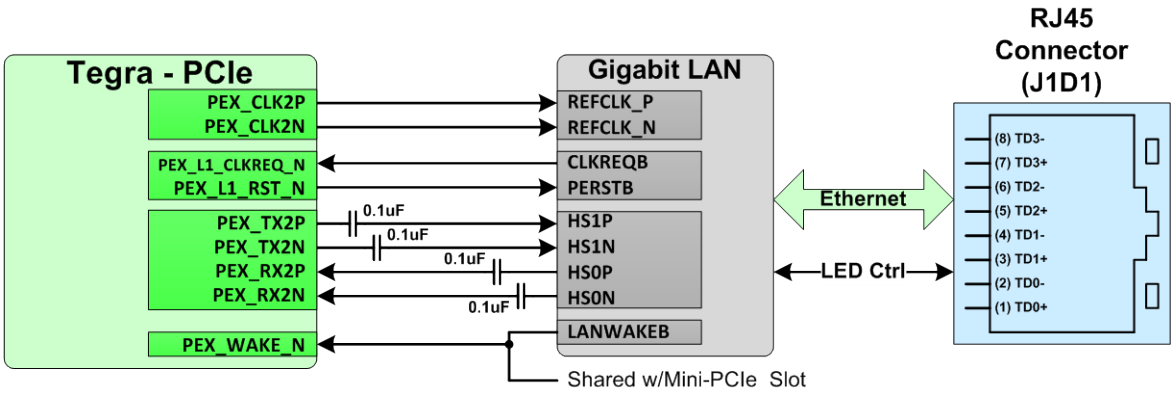
Figure 13. USB Port Connections



3.3 Gigabit LAN

Jetson uses one of the x1 PCIe lanes to interface to a Realtek RTL8111GS Gigabit LAN controller. A standard RJ45 connector is provided (Reference designator J1D1). Connections are shown below.

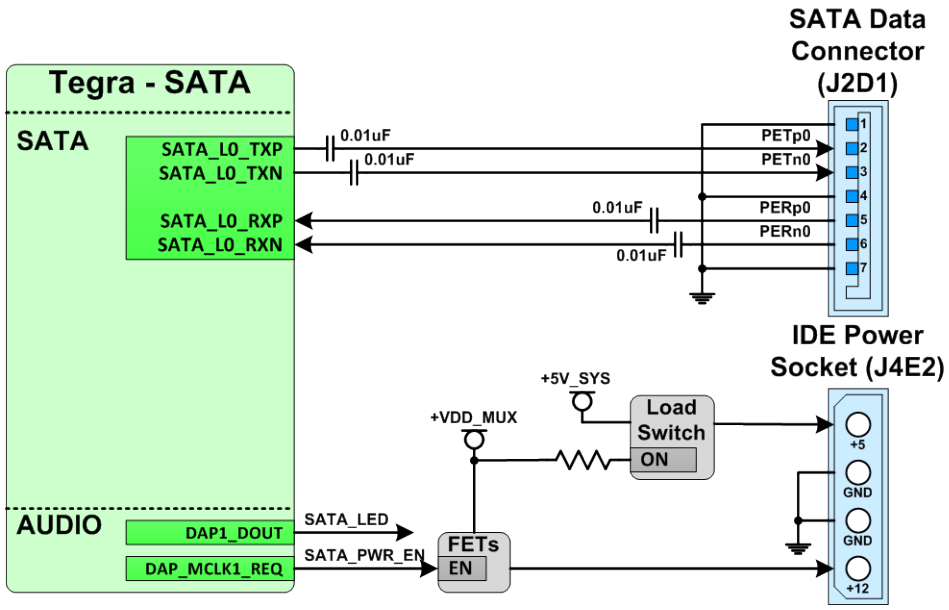
Figure 14. Jetson Gigabit LAN Connections



3.4 SATA

Tegra supports a SATA interface. Jetson TK1 routes this to a standard SATA connector (Reference designator J2D1). +5V & +12V is supplied from a standard IDE Power Socket (Reference designator J4E2). +5V is provided by a gated version of the main +5V_SYS supply which supports up to 4A (shared with other devices). 12V is from a gated version of the +12V supply from the DC jack.

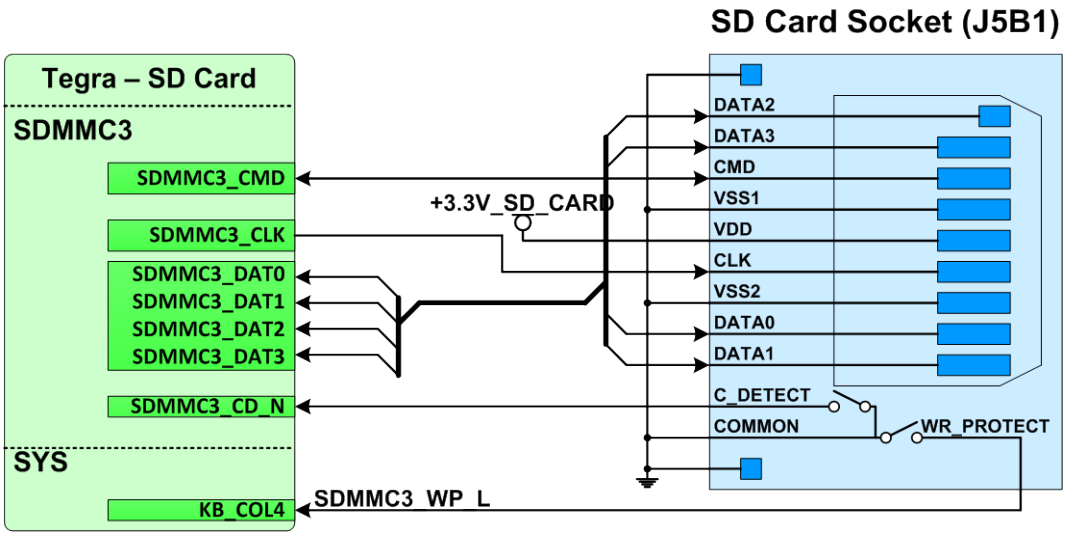
Figure 15. SATA Connections



3.5 SD Card

Tegra supports an SD Card interface which is routed to a full size SD socket (Reference designator J5B1) on the Jetson TK1 design. This interface supports up to the full SDR104 mode (UHS-1).

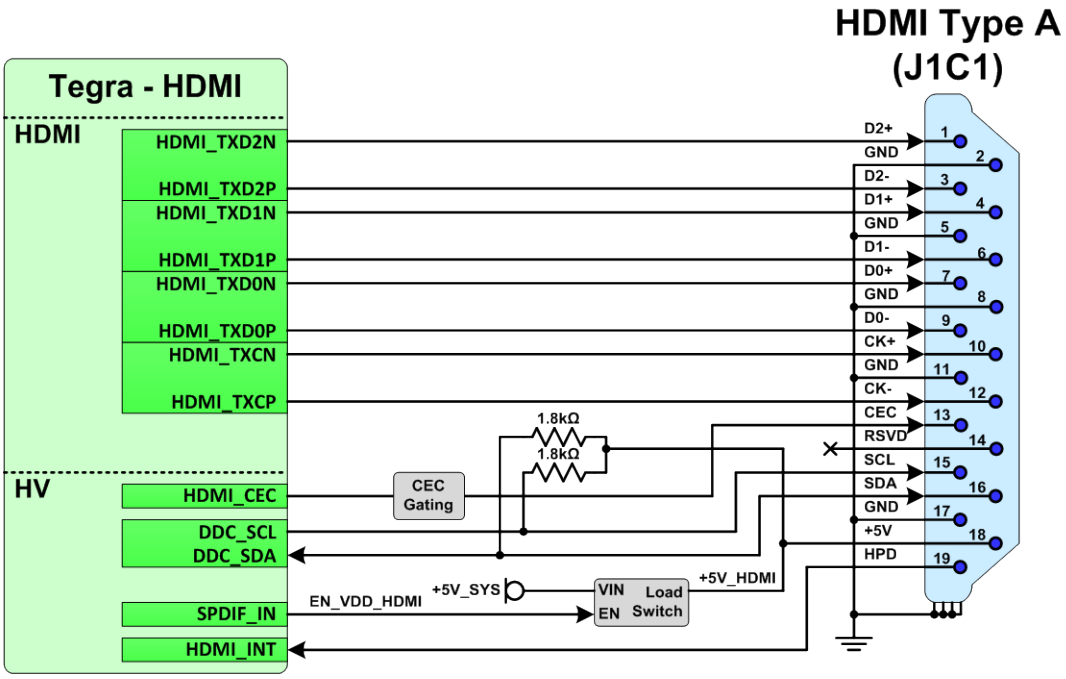
Figure 16. SD Card Connections



3.6 HDMI

A standard HDMI Type A connector (Reference designator J1C1) is supported on Jetson TK1. The +5V supply to the connector comes from an RT9728 Load Switch, supporting up to 1.3A.

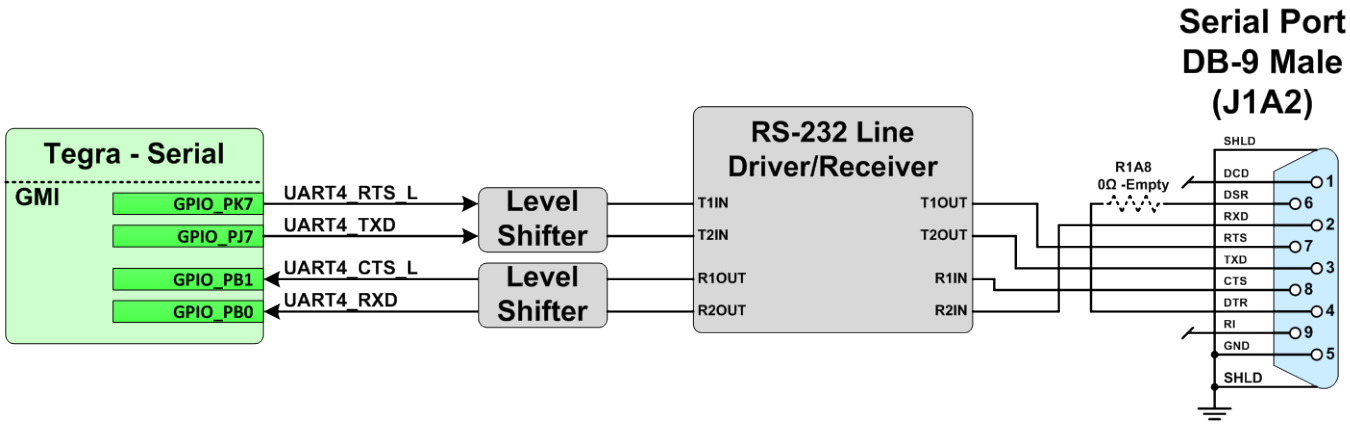
Figure 17. HDMI Connections



3.7 Serial Port

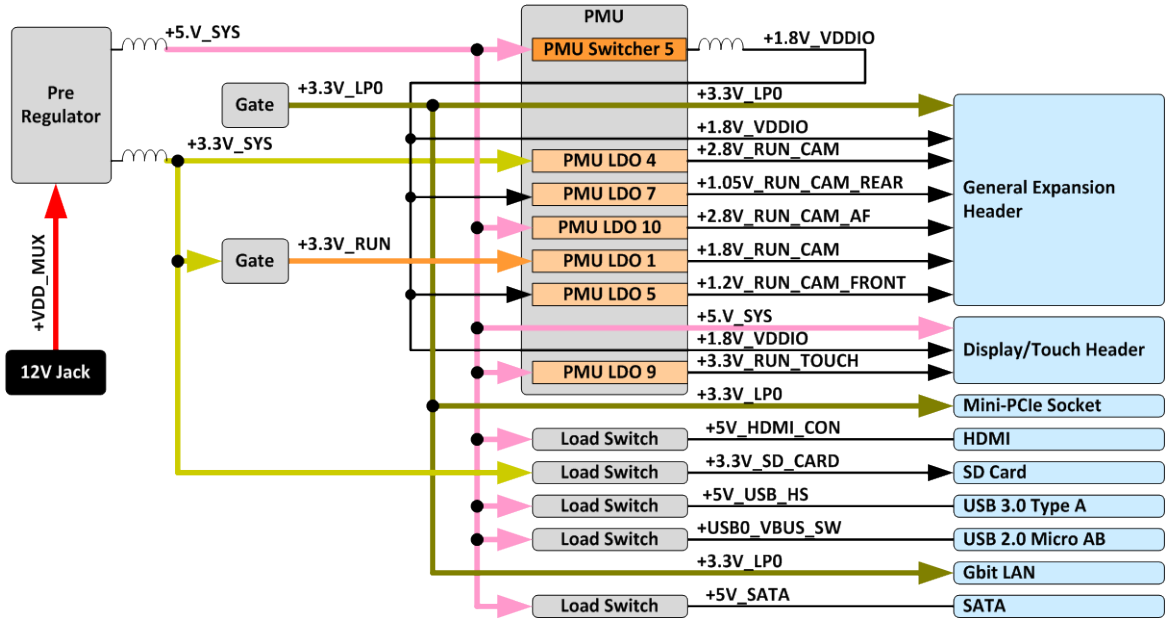
A standard DB-9 Male RS-232 Serial Port connector (Reference designator J1A2) is provided on Jetson TK1.

Figure 18. RS-232, DB-9 Serial Port Connections



4.0 Interface Power

Figure 19. Interface Connector Power Diagram



The table below shows the allocation of supplies to the connectors on the Jetson TK1 main board.

Table 26 Interface Power Supply Allocation

Power Rails	Usage	(V)	Power Supply or Gate	Source	Enable	Supported Current (mA)	Notes
+VDD_MUX	Main power from AC adapter	12	na	Power Jack	na	400	1, 2
+5V_SYS	Main 5V supply	5.0	TPS51220 Switcher	**+VDD_MUX**	PMU EN5V	500	
+3.3V_SYS	Main 3.3V supply	3.3	TPS51220 Switcher	**+VDD_MUX**	PMU GPIO2	500	
+3.3V_LP0 (Mini-PCIe 3.3VAUX)	Gated 3.3V supply. On in Deep Sleep	3.3	SLG5NV-1430V Gate	**+3.3V_SYS**	REGEN1	1100	
+3.3V_RUN	Gated 3.3V supply. Off in Deep Sleep	3.3	SLG5NV-1430V Gate	**+3.3V_SYS**	REGEN3	450	
+1.8V_VDDIO	Main 1.8V supply	1.8	PMU Switcher SD5	**+5V_SYS**	Pwr-on Seq	400	
+1.8V_RUN_CAM	Camera 1.8V supply	1.8	PMU LDO 1	**+3.3V_RUN**	I2C/PMU	100	
+2.8V_RUN_CAM	High voltage Camera supply	2.8	PMU LDO 4	**+3.3V_SYS**	I2C/PMU	300	
+1.2V_RUN_CAM_FRONT	Front Camera 1.2V supply	1.2	PMU LDO 5	**+1.8V_VDDIO**	I2C/PMU	300	
+1.05V_RUN_CAM_REAR	Rear camera 1.05V supply	1.05	PMU LDO 7	**+1.8V_VDDIO**	I2C/PMU	300	
+3.3V_RUN_TOUCH	High voltage touch supply	3.3	PMU LDO 9	**+5V_SYS**	I2C/PMU	50	
+2.8V_RUN_CAM_AF	Camera autofocus supply	2.8	PMU LDO 10	**+5V_SYS**	I2C/PMU	300	

Power Rails	Usage	(V)	Power Supply or Gate	Source	Enable	Supported Current (mA)	Notes
+VDD_1V5_MPCIE	Mini-PCIe 1.5V	1.5	APL5910 LDO		3.3VAUX	375	
+5V_USB_HS	USB 3.0 Type A VBUS supply	5.0	TPS2065 Load Switch	**+5V_SYS**	Tegra GPIO	900	
+USB0_VBUS_SW	USB 2.0 Micro AB VBUS supply	5.0	TPS2065 Load Switch	**+5V_SYS**	Tegra GPIO	500	
+5V_HDMI_CON	HDMI connector supply	5.0	RT9728 Load SW	**+5V_SYS**	Tegra GPIO	150	
+3.3V_SD_CARD	SD Card socket supply	3.3	TPS22908 Load SW	**+3.3V_SYS**	Tegra GPIO	500	
+5V_SATA	SATA connector supply	5.0	SLG5NV-1430V Gate	**+5V_SYS**	Tegra GPIO	1000	

Note:
1. Jetson TK1 is characterized to accept an input voltage of 12V +10%. The board may not reliably turn on with < 9.5V. A voltage > 13.2V may damage a SATA HDD using 12V. > 16V, the main board may be damaged. It may be possible to run the system on batteries around the 10-16V region (without HDDs requiring 12V), but NVIDIA has not tested this configuration.
2. Total current available on +VDD_MUX is determined by adapter used. The adapter supplied with the Jetson TK1 Developer Kit is rated at 5A.
3. The values shown in the "Supported Current" column indicate the total power available on the expansion connectors (not per pin).
4. If a given voltage rail cannot provide enough current, a possible solution is for the user to use a regulator from +5V_SYS, +3.3V_SYS or +1.8V_VDDIO to generate the desired rail.

5.0 Tegra Pad Details

Table 27. ST / CZ Pad Type Details

Symbol	Description	Min	Max	Units
V_{IL}	Input Low Voltage	-0.5	0.25 x VDD	V
V_{IH}	Input High Voltage	0.75 x VDD	0.5 + VDD	V
V_{OL}	Output Low Voltage (I_{OL} = 1mA)	---	0.15 x VDD	V
V_{OH}	Output High Voltage (I_{OH} = -1mA)	0.85 x VDD	---	V

Table 28. DD Pad Type Details

Symbol	Description	Min	Max	Units
V_{IL}	Input Low Voltage	-0.5	0.25 x VDD	V
V_{IH}	Input High Voltage	0.75 x VDD		V
V_{OL}	Output Low Voltage (I_{OL} = 1mA)	---	0.15 x VDD	V

Note: Do not drive unpowered signals (when associated power rail is off).

6.0 Design Guideline Glossary

The Design Guidelines include various terms. The descriptions in the table below are intended to show what these terms mean and how they should be applied to a design.

Table 29 Layout Guideline Tutorial

Trace Delays
Max Breakout Delay - Routing on Component layer: Maximum Trace Delay from inner ball to point beyond ball array where normal trace spacing/impedance can be met. Routing passes to layer other than Component layer: Trace delay from ball to via + via delay. Beyond this, normal trace spacing/impedance must be met. **Max Total Trace Delay** - Package route + Trace from ball to Device pin. This must include routing on the main PCB & any other Flex or secondary PCB. Delay is from Tegra to the final connector/device.
Intra/Inter Pair Skews
Intra Pair Skew (within pair) – Package + PCB - Difference in delay between two traces in differential pair: Shorter routes may require indirect path to equalize delays **Inter Pair Skew (pair to pair) – Package + PCB** - Difference between two (or possibly more) differential pairs
Impedance/Spacing
Microstrip vs Stripline - Microstrip: Traces next to single ref. plane. Stripline: Traces between two ref planes **Trace Impedance** - Impedance of trace determined by width & height of trace, distance from ref. plane & dielectric constant of PCB material. For differential traces, space between pair of traces is also a factor **Board trace spacing / Spacing to other nets** - Minimum distance between two traces. Usually specified in terms of dielectric height which is distance from trace to reference layers. **Pair to pair spacing** - Spacing between differential traces **Breakout spacing** - Possible exception to board trace spacing above is shown in figure to right where different spacing rules are allowed under Tegra in order to escape from Ball array. - This includes spacing between adjacent traces & between traces/vias or pads under the device in order to escape ball matrix. Outside device boundary, normal spacing rules apply.

Reference Return

Ground Reference Return Via & Via proximity (signal to reference)

- Signals changing layers & reference GND planes need similar return current path
- Accomplished by adding via, tying both GND layers together

Via proximity (sig to ref) is distance between signal & reference return vias

- GND reference via for Differential Pair
- Where a differential pair changes GND reference layers, return via should be placed close to & between signal vias (example to right)

Signal to return via ratio

- Number of Ground Return vias per Signal vias. For critical IFs, ratio is usually 1:1. For less critical IFs, several trace vias can share fewer return vias (i.e. 3:2 – 3 trace vias & 2 return vias).

Slots in Ground Reference Layer

- When traces cross slots in adjacent power or ground plane
- Return current has longer path around slot
- Longer slots result in larger loop areas
- Avoid slots in GND planes or do not route across them

Routing over Split Power Layer Reference Layers

- When traces cross different power areas on power plane
  - Return current must find longer path - usually a distant bypass cap
  - If possible, route traces w/solid plane (GND or PWR) or keep routes across single area
- If traces must cross two or more power areas, use stitching capacitors
  - Placing one cap across two PWR areas near where traces cross area boundaries provides high-frequency path for return current
  - Cap value typically 0.1uF & should ideally be within 0.1" of crossing