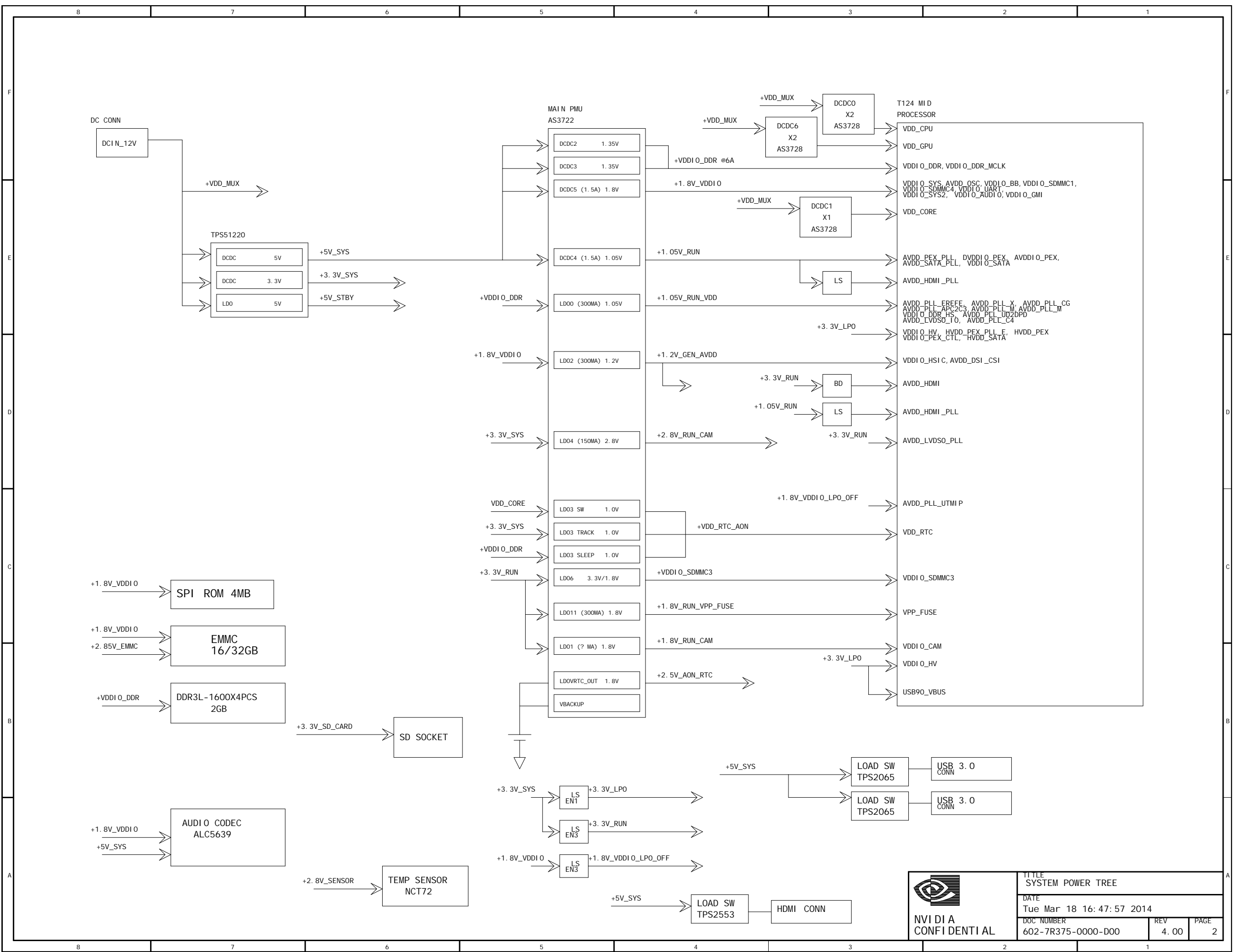


PAGE	TITLE
PAGE 1:	COVER PAGE
PAGE 2:	SYSTEM POWER TREE
PAGE 3:	I2C ADDRESS MAP
PAGE 4:	T124: CH0 MEMORY I/F
PAGE 5:	T124: CH1 MEMORY I/F
PAGE 6:	DDR3 X16 PAGE 1
PAGE 7:	DDR3 X16 PAGE 2
PAGE 8:	T124: SDMMC/ULPI/JTAG/KB
PAGE 9:	T124: CSI/DSI/HDMI/USB
PAGE 10:	T124: UART/GMI/DAP/SPI
PAGE 11:	T124: POWER
PAGE 12:	T124: GND
PAGE 13:	HDMI TYPE A CONN
PAGE 14:	T124: SATA, PEX, USB 3.0
PAGE 15:	MINI HALF PCIE
PAGE 16:	PEX OPTIONS AND SATA
PAGE 17:	USB PORTS
PAGE 18:	TEMP SENSOR, SERIAL, ID
PAGE 19:	PEX GIGE LAN/PHY
PAGE 20:	AUDIO CODEC
PAGE 21:	AUDIO CONNECTORS
PAGE 22:	JTAG CONN: I2C TRANSLATER
PAGE 23:	EMMC, SPI, ROM
PAGE 24:	SWITCHES & STRAPS
PAGE 25:	SD CONN & FRONT PANEL HDR
PAGE 26:	EXP: TOUCH/DISP & GENERAL
PAGE 27:	DC IN
PAGE 28:	+3.3V VR
PAGE 29:	+5V VR
PAGE 30:	LOAD SWITCHES
PAGE 31:	PMIC: LOGIC AND GPIOs
PAGE 32:	PMIC: CNTL, INT SW, LDOS
PAGE 33:	PMIC: DCDC
PAGE 34:	PMIC: T124 GPU AND CORE
PAGE 35:	VDD CPU VR
PAGE 36:	REVISION HISTORY
PAGE 37:	BASENET REPORT
PAGE 38:	BASENET REPORT
PAGE 39:	BASENET REPORT
PAGE 40:	BASENET REPORT
PAGE 41:	BASENET REPORT
PAGE 42:	BASENET REPORT
PAGE 43:	CREF PART REPORT
PAGE 44:	CREF PART REPORT
PAGE 45:	CREF PART REPORT
PAGE 46:	CREF PART REPORT
PAGE 47:	CREF PART REPORT
PAGE 48:	CREF PART REPORT
PAGE 49:	CREF PART REPORT

T124 Compact Development Module
 602-7R375-0000-D00
 SCH REV 4.00
 3/18/2014
 FAB REV D
 BOM REV A

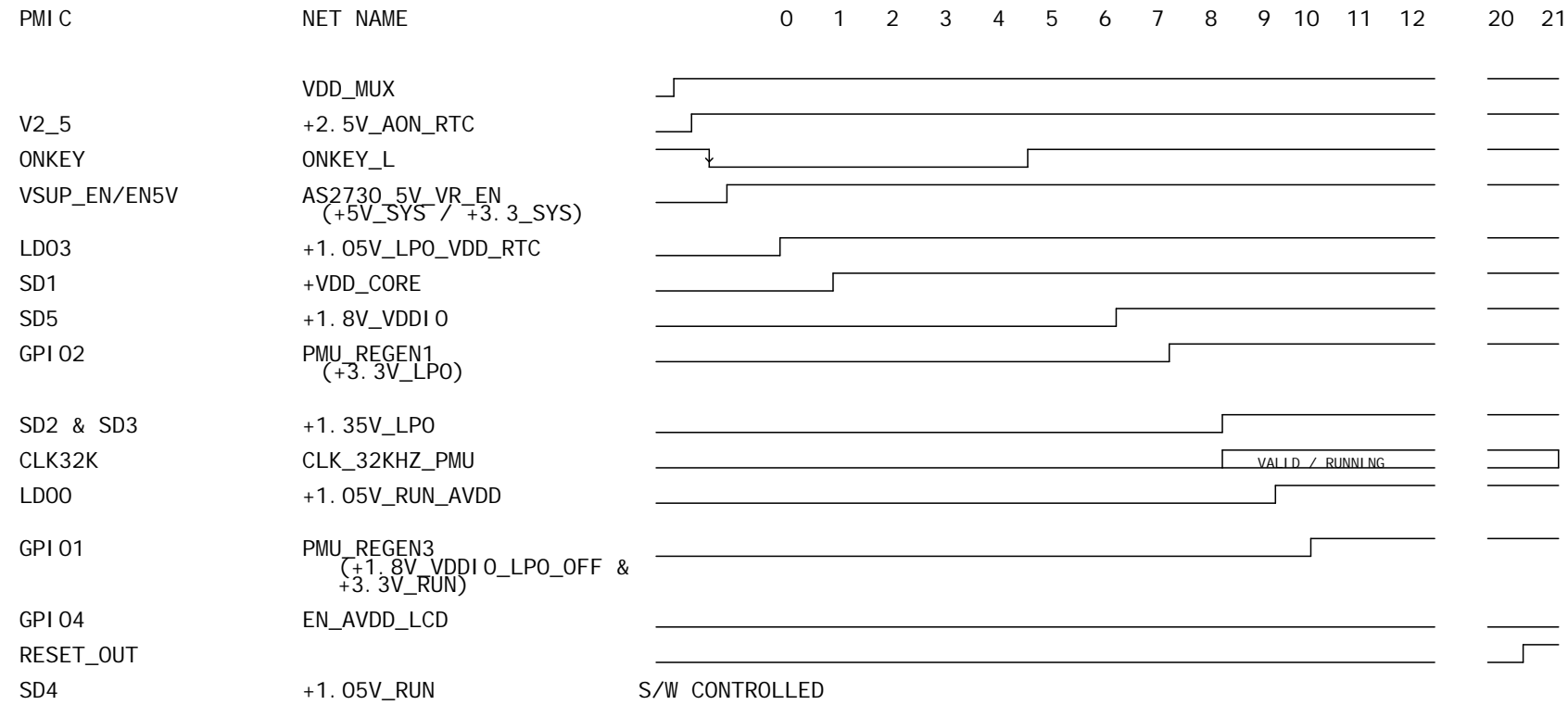
NVIDIA CORPORATION		
2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050		
NVIDIA CONFIDENTIAL		
ALL NVIDIA DESIGN SPECIFICATION, REFERENCE BOARDS, FILTERS, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, MATERIALS) ARE BEING PROVIDED AS IS. NVIDIA MAKES NO WARRANTIES, EXPRESSED OR IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES OF NONINFRINGEMENT, MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.		
TITLE		COVER PAGE
T124 Compact Development Module		
DATE		
Tue Mar 18 16:47:56 2014		
DOC NUMBER		
602-7R375-0000-D00		PAGE 1 OF 49



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TITLE SYSTEM POWER TREE		
DATE Tue Mar 18 16:47:57 2014		
DOC NUMBER 602-7R375-0000-D00	REV 4.00	PAGE 2

POWER SEQUENCING



I2C ADDRESS MAP

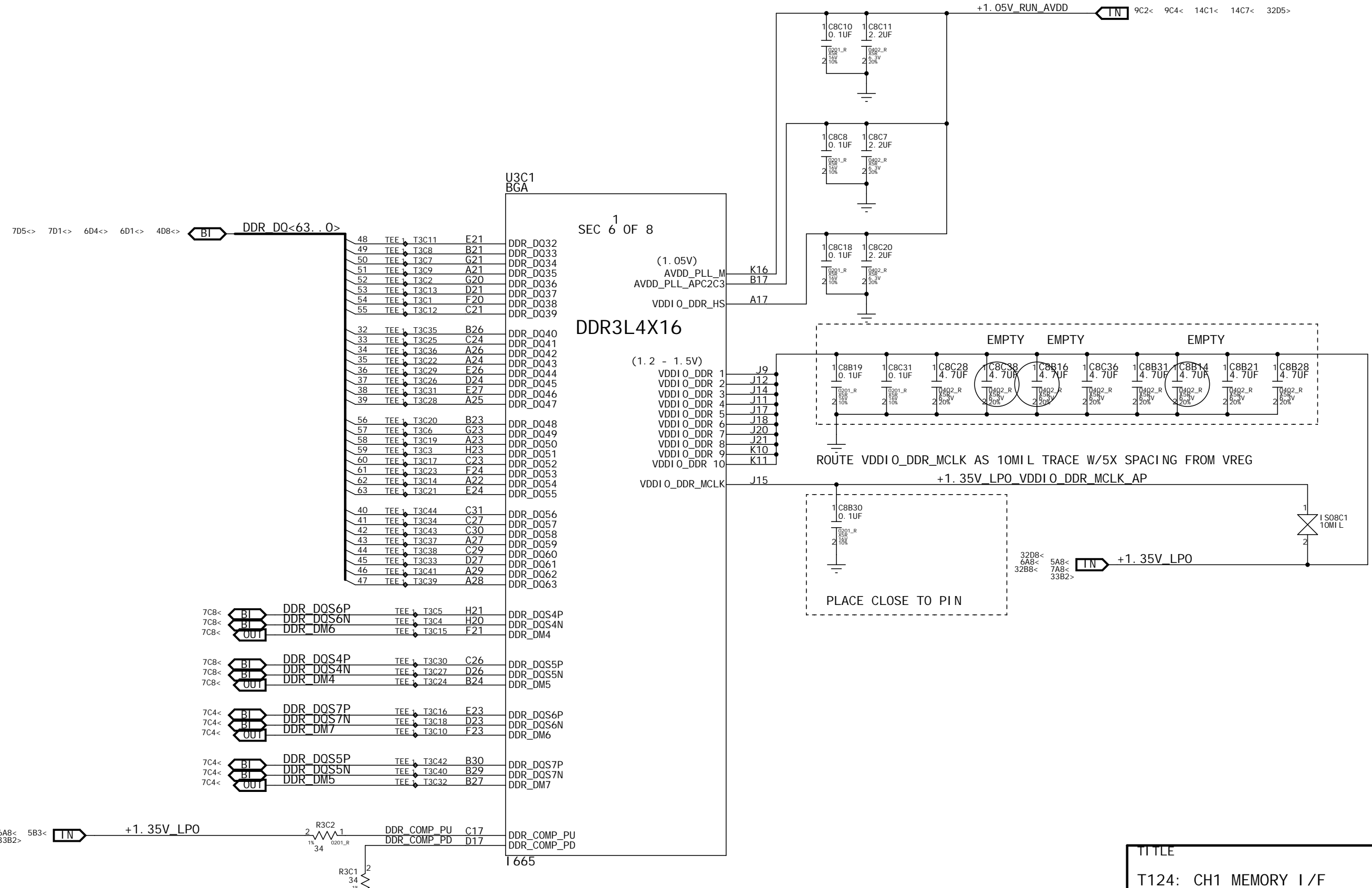
BUS	DEVICE	ADDRESS
GEN1_I2C - 1.8V	AUDIO CODEC	7' H1C, 8' H38
	TEMPERATURE SENSOR	7' H4C, 8' H98
	BOARD ID	7' H56, 8' HAC
	EXPANSION	UNKNOWN
GEN1_I2C - 3.3V	HALF MINI PCI E	UNKNOWN
GEN2_I2C - 3.3V	EXPANSION	UNKNOWN
PWR_I2C - 1.8V	PMIC AS3722	7' H40, 8' H80
	EXPANSION	UNKNOWN
CAM_I2C - 3.3V	EXPANSION	UNKNOWN

TITLE I2C ADDRESS MAP			
DOC NUMBER 602-7R375-0000-D00	REV 4.00	PAGE 3	

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Tue Mar 18 16:47:57 2014

T124: CH1 MEMORY I/F



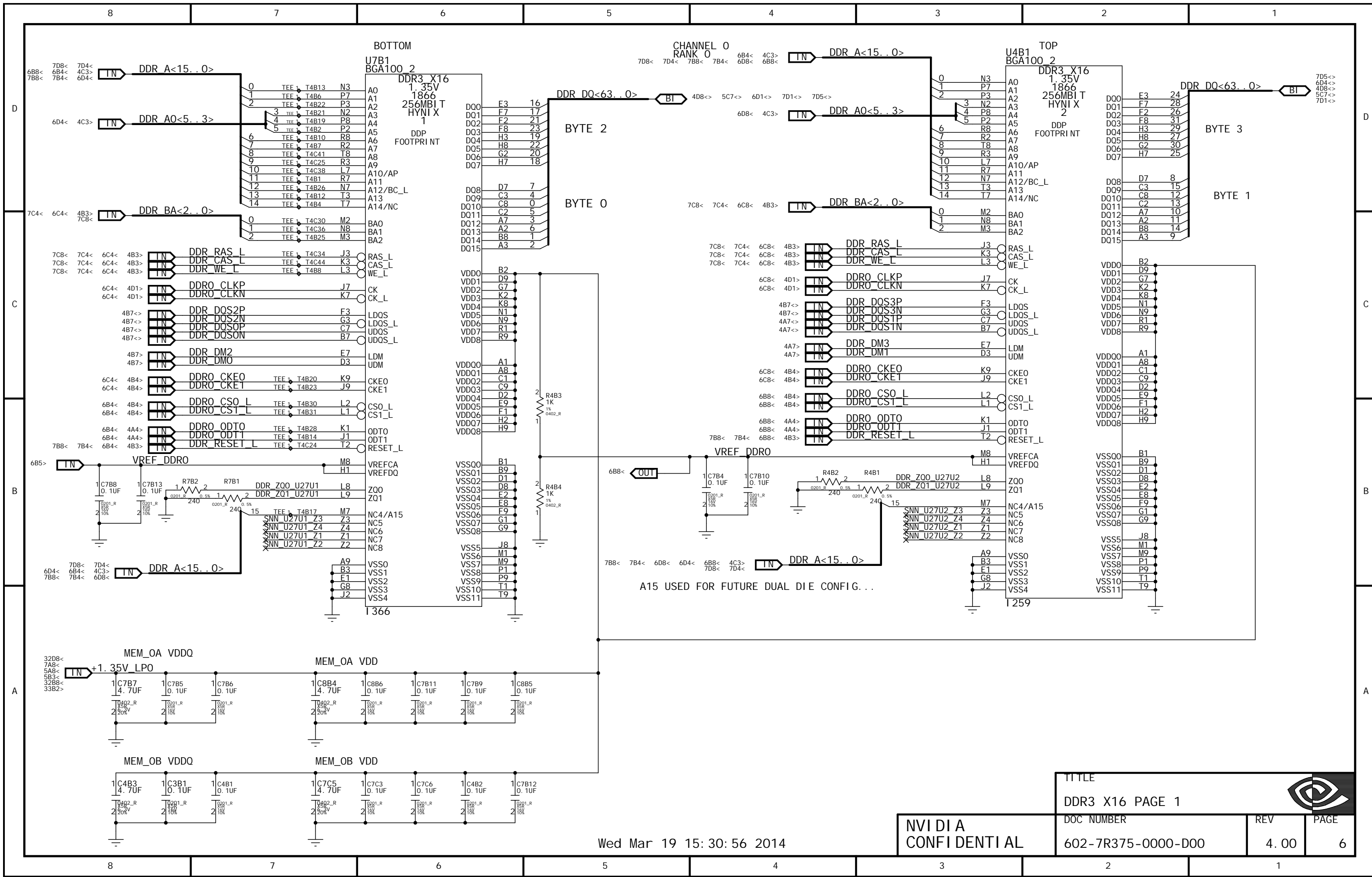
SEC 6 OF 8

DDR3L4X16

TITLE			
T124: CH1 MEMORY I/F			
DOC NUMBER	REV	PAGE	
602-7R375-0000-D00	4.00	5	


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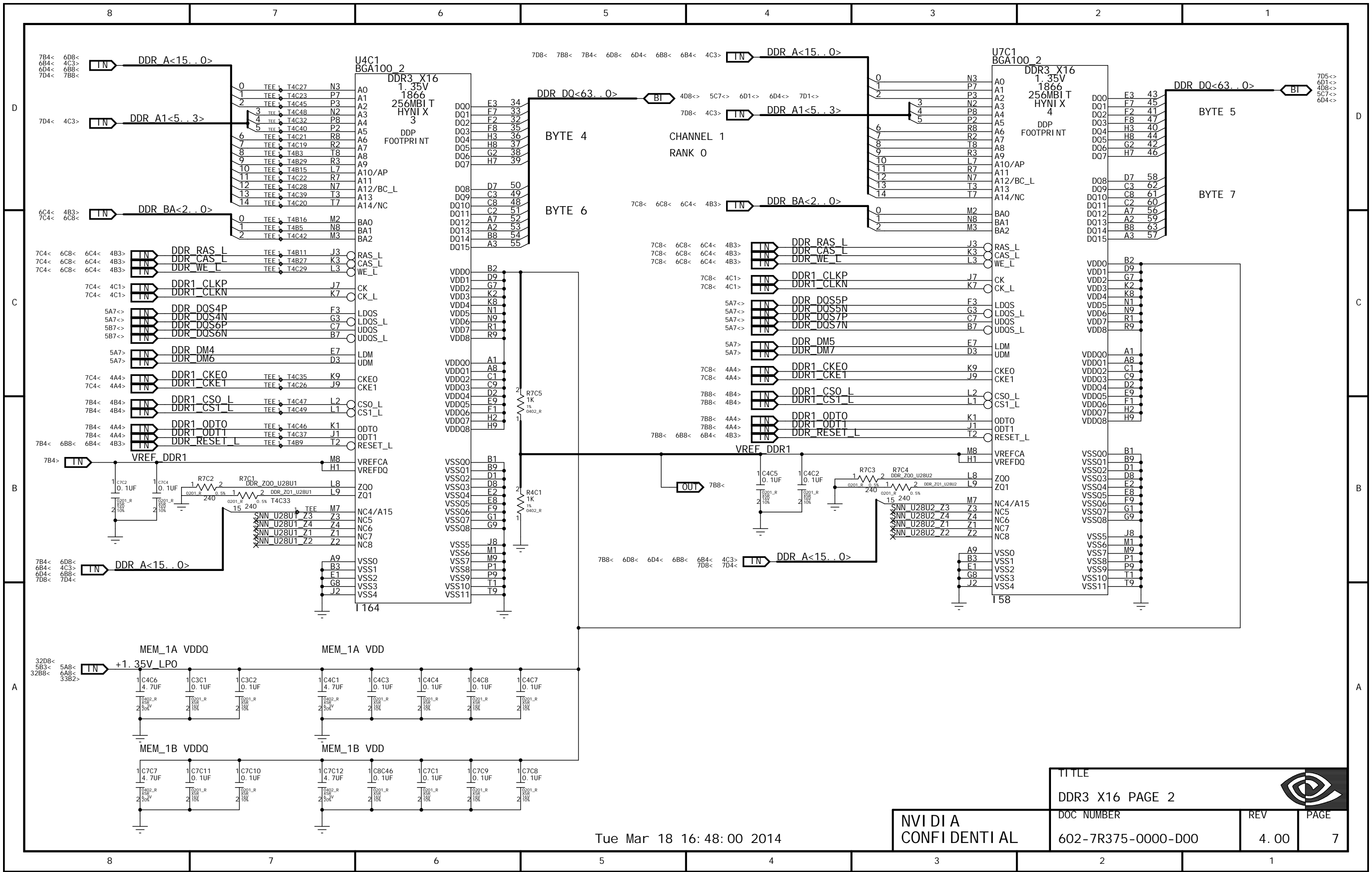
Tue Mar 18 16:47:58 2014



Wed Mar 19 15:30:56 2014

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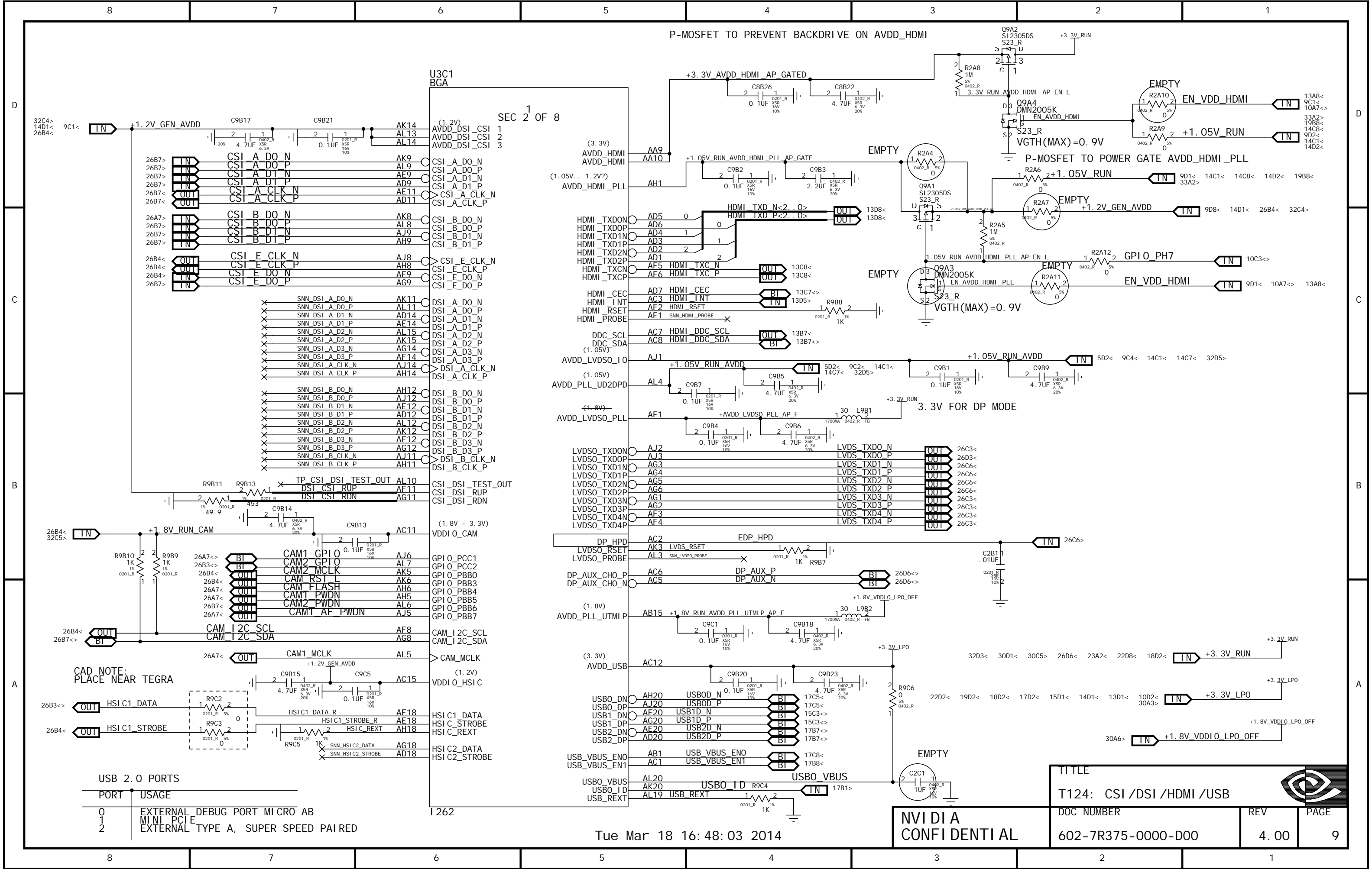
TITLE			
DDR3 X16 PAGE 1			
DOC NUMBER	REV	PAGE	
602-7R375-0000-D00	4.00	6	



TITLE		DDR3 X16 PAGE 2	
DOC NUMBER	REV	PAGE	
602-7R375-0000-D00	4.00	7	

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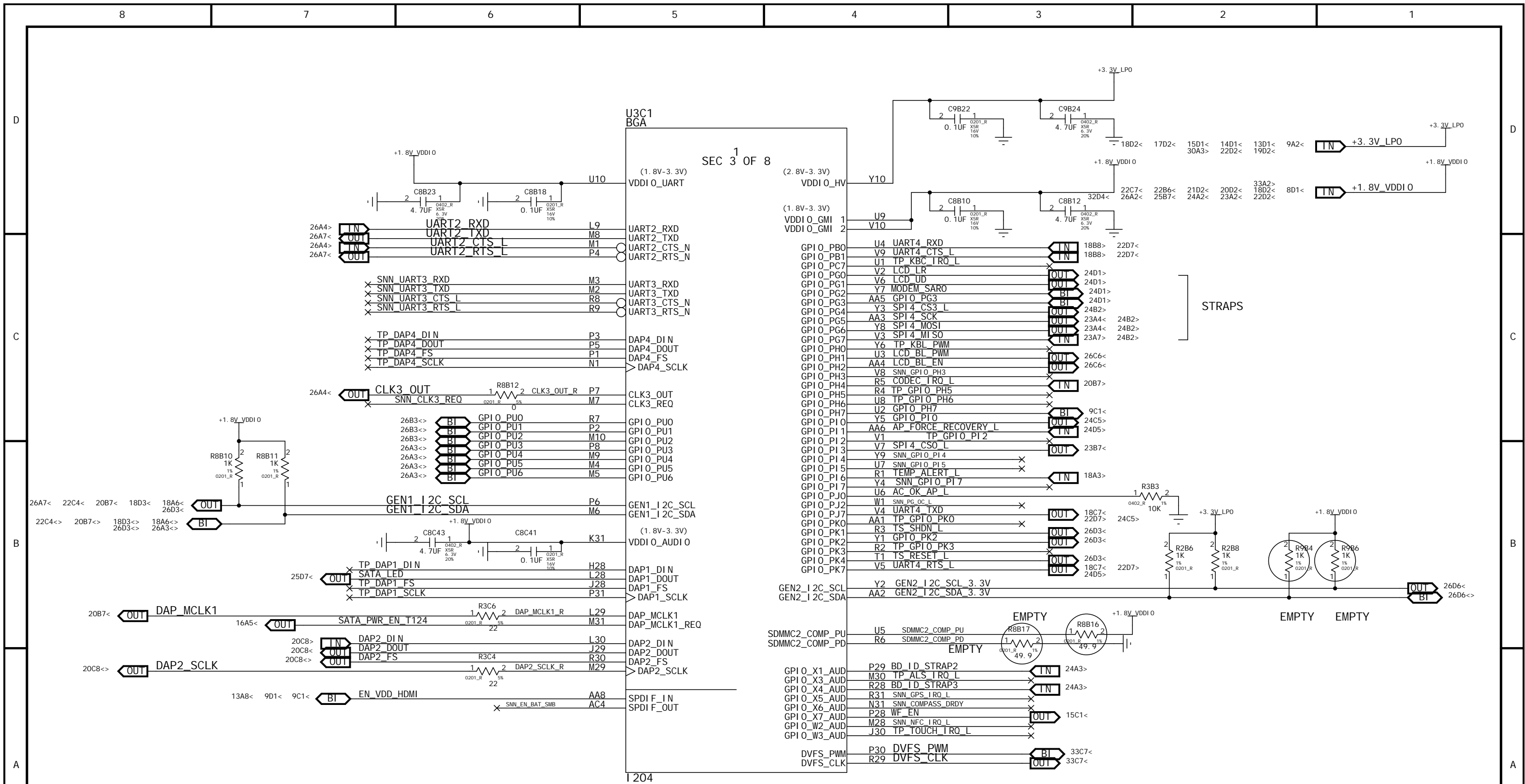
Tue Mar 18 16:48:00 2014



Tue Mar 18 16:48:03 2014

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TITLE		
T124: CSI/DSI/HDMI/USB		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.00	9

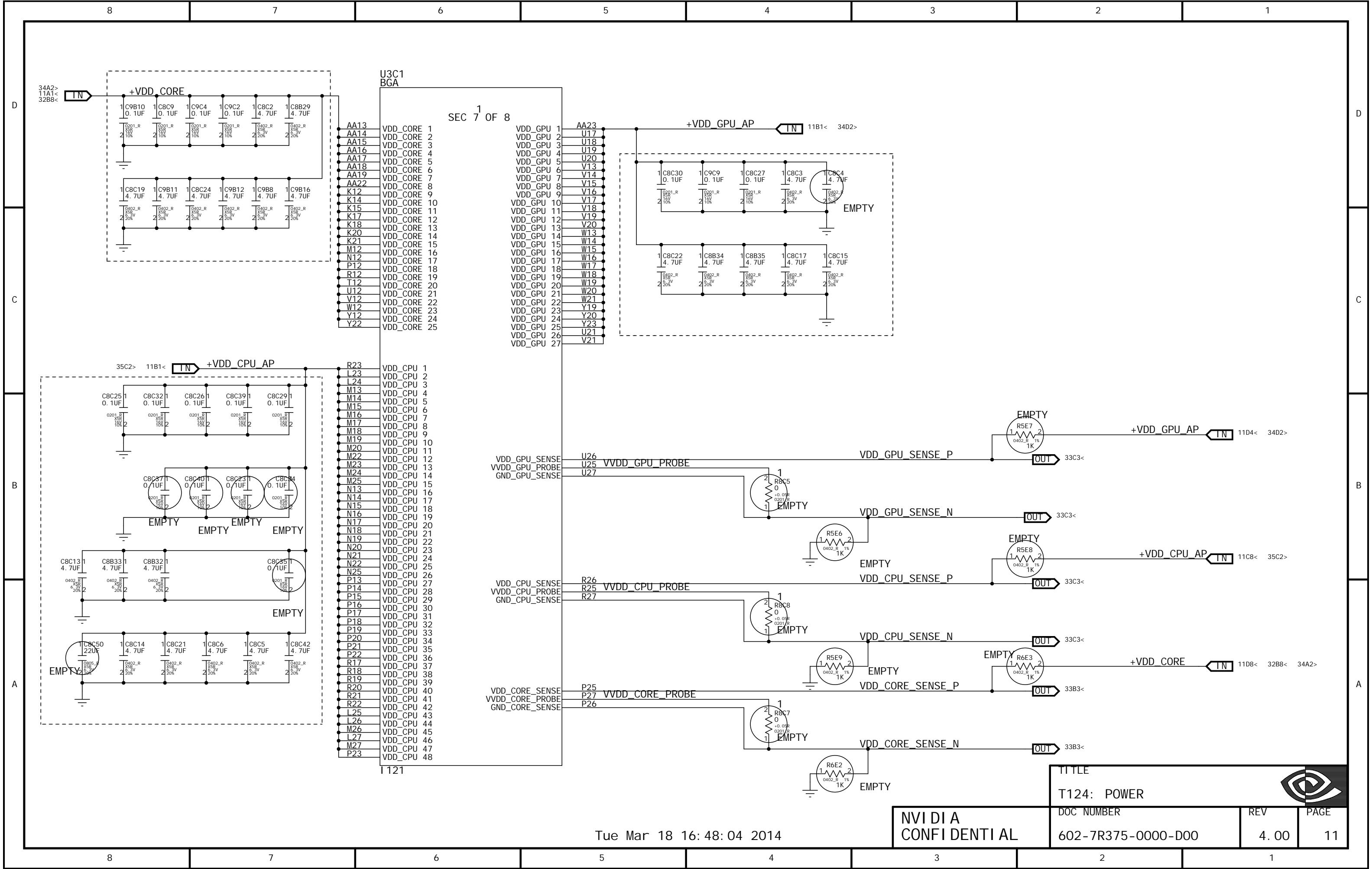


SET E_OD PAD = 1 WHEN PU VALUE DIFFERS FROM VDD SOURCE FOR GEN2 I2C

TITLE		
T124: UART/GMI/DAP/SPI		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.00	10

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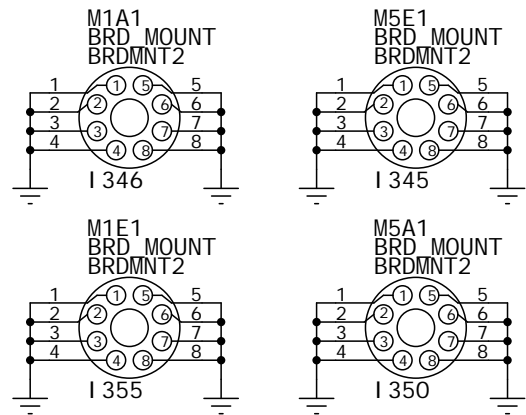
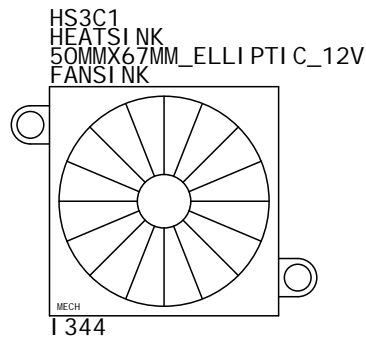
Tue Mar 18 16:48:04 2014



TITLE			
T124: POWER			
DOC NUMBER	REV	PAGE	
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CONFIDENTIAL

Tue Mar 18 16:48:04 2014



U3C1
BGA

SEC 1 OF 8

A2	GND 1	GND 21	AE16
AB21	GND 10	GND 22	AE19
L16	GND 100	GND 23	AE22
L17	GND 101	GND 24	AE28
L18	GND 102	GND 25	AE30
L19	GND 103	GND 26	AH2
N2	GND 104	GND 27	AH4
N4	GND 105	GND 28	AH7
N7	GND 106	GND 29	AH10
N10	GND 107	GND 3	AB2
N11	GND 108	GND 30	AH13
N28	GND 109	GND 31	AH16
AB25	GND 11	GND 32	AH19
N30	GND 110	GND 33	AH22
P11	GND 111	GND 34	AH25
R11	GND 112	GND 35	AH28
R13	GND 113	GND 36	AH30
R14	GND 114	GND 37	AK1
R15	GND 115	GND 38	AK4
R16	GND 116	GND 39	AK7
T2	GND 117	GND 4	AB4
T4	GND 118	GND 40	AK10
T7	GND 119	GND 41	AK13
AB28	GND 12	GND 42	AK16
T10	GND 120	GND 43	AK19
T11	GND 121	GND 44	AK22
T13	GND 122	GND 45	AK25
T14	GND 123	GND 46	AK28
T15	GND 124	GND 47	AK31
T16	GND 125	GND 48	AL2
T17	GND 126	GND 49	AL30
T18	GND 127	GND 5	AB7
T19	GND 128	GND 50	B1
T20	GND 129	GND 51	B4
AB30	GND 13	GND 52	B7
T21	GND 130	GND 53	B10
T22	GND 131	GND 54	B13
T25	GND 132	GND 55	B16
T28	GND 133	GND 56	B19
T30	GND 134	GND 57	B22
U11	GND 135	GND 58	B25
U13	GND 136	GND 59	B28
U14	GND 137	GND 6	AB10
U15	GND 138	GND 60	B31
U16	GND 139	GND 61	D2
AC9	GND 14	GND 62	D4
U22	GND 140	GND 63	D7
V11	GND 141	GND 64	D10
V22	GND 142	GND 65	D13
W2	GND 143	GND 66	D16
W4	GND 144	GND 67	D19
W7	GND 145	GND 68	D22
W10	GND 146	GND 69	D25
W11	GND 147	GND 7	AB13
W22	GND 148	GND 70	D28
W25	GND 149	GND 71	D30
AD8	GND 15	GND 72	G2
W28	GND 150	GND 73	G4
W30	GND 151	GND 74	G7
Y13	GND 152	GND 75	G10
Y14	GND 153	GND 76	G13
Y15	GND 154	GND 77	G16
Y16	GND 155	GND 78	G19
Y17	GND 156	GND 79	G22
Y18	GND 157	GND 8	AB16
AK2	GND 158	GND 80	G24
AE8	GND 159	GND 81	G25
AB11	GND 160	GND 82	G28
AB14	GND 161	GND 83	G30
P24	GND 162	GND 84	H8
R24	GND 163	GND 85	H24
T31	GND 164	GND 86	J23
V27	GND 165	GND 87	K2
AE23	GND 166	GND 88	K4
L22	GND 167	GND 89	K7
AE2	GND 16	GND 9	AB19
AE4	GND 17	GND 90	K13
AE7	GND 18	GND 91	AE24
AE10	GND 19	GND 92	K19
A30	GND 2	GND 93	K22
AE13	GND 20	GND 94	AE25
K30	GND 96	GND 95	K28
L13	GND 97		
L14	GND 98		
L15	GND 99		

I 357

TITLE			
T124: GND			
DOC NUMBER	REV	PAGE	
602-7R375-0000-D00	4.00	12	

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D

C

B

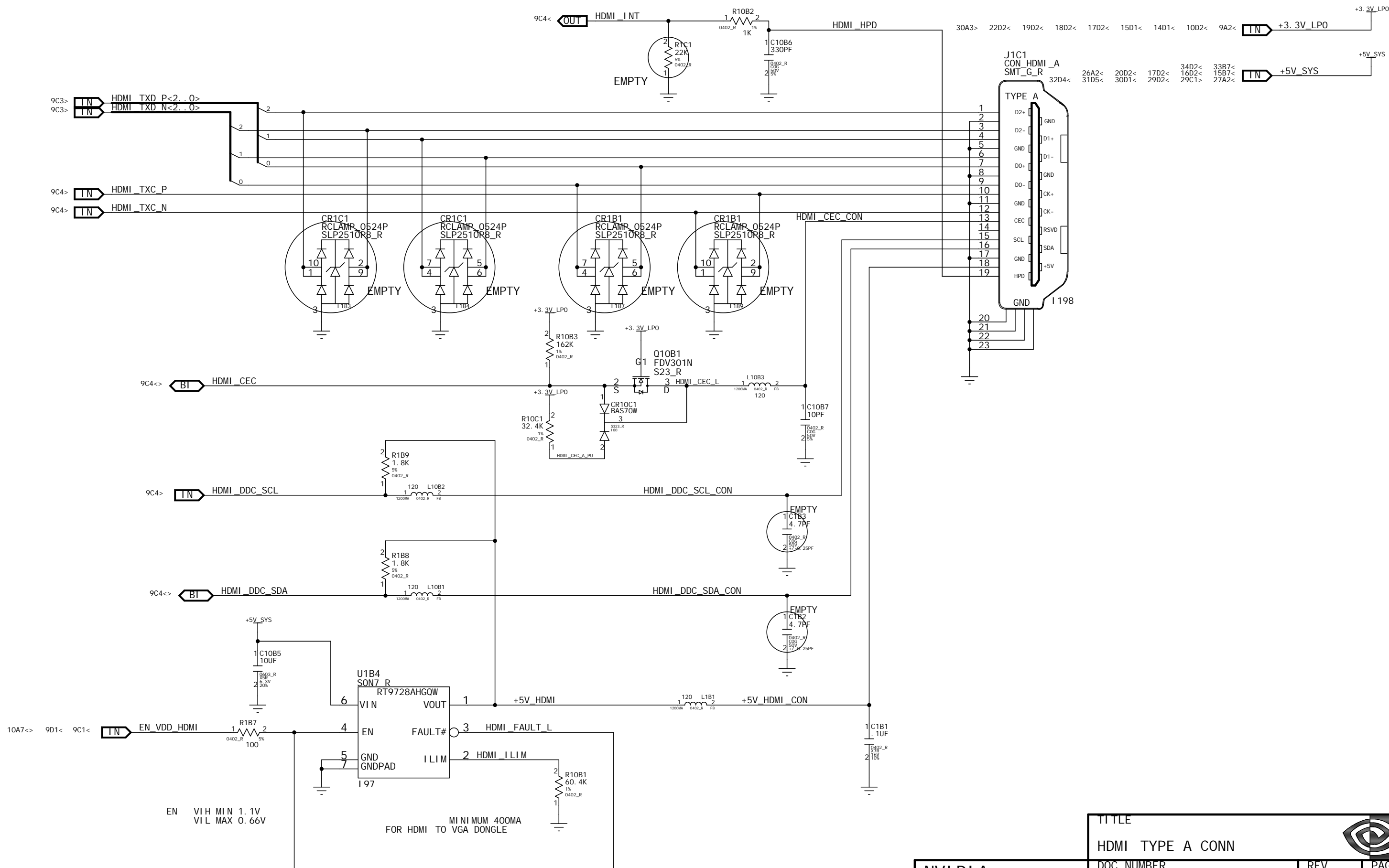
A

D

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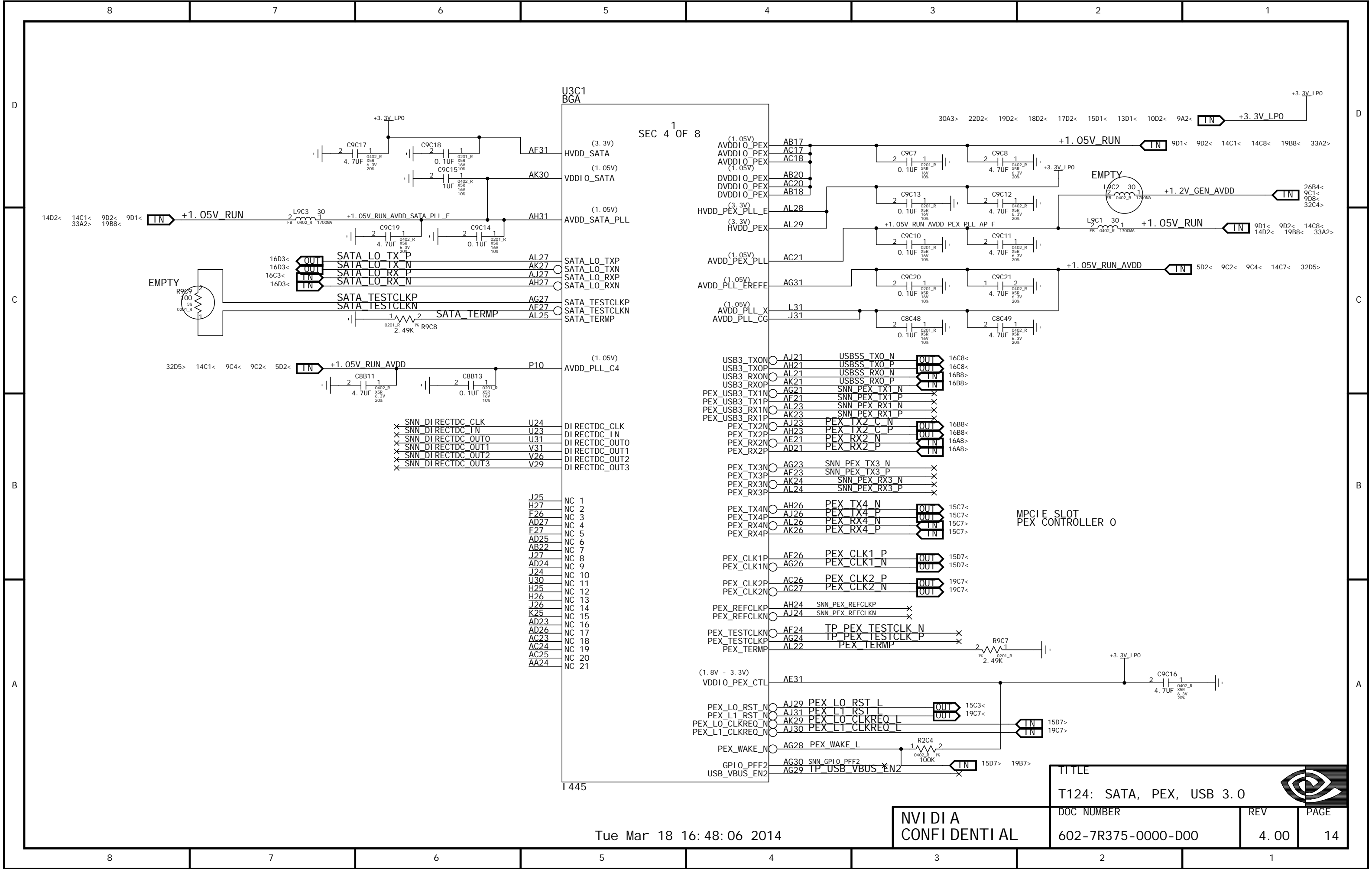
B

A



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Tue Mar 18 16:48:06 2014



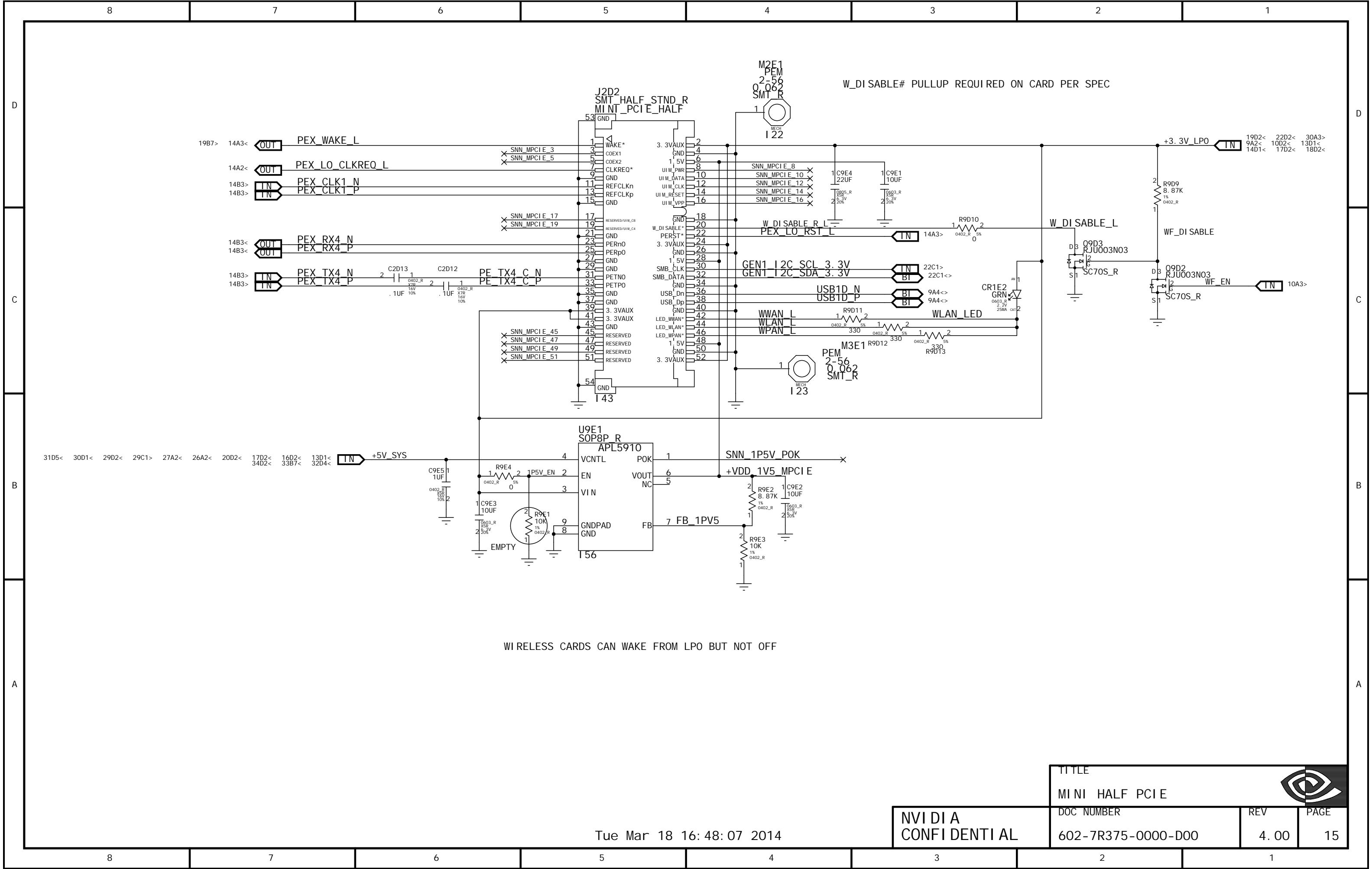
SEC 4 OF 8

1445

TITLE		
T124: SATA, PEX, USB 3.0		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.00	14


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Tue Mar 18 16:48:06 2014



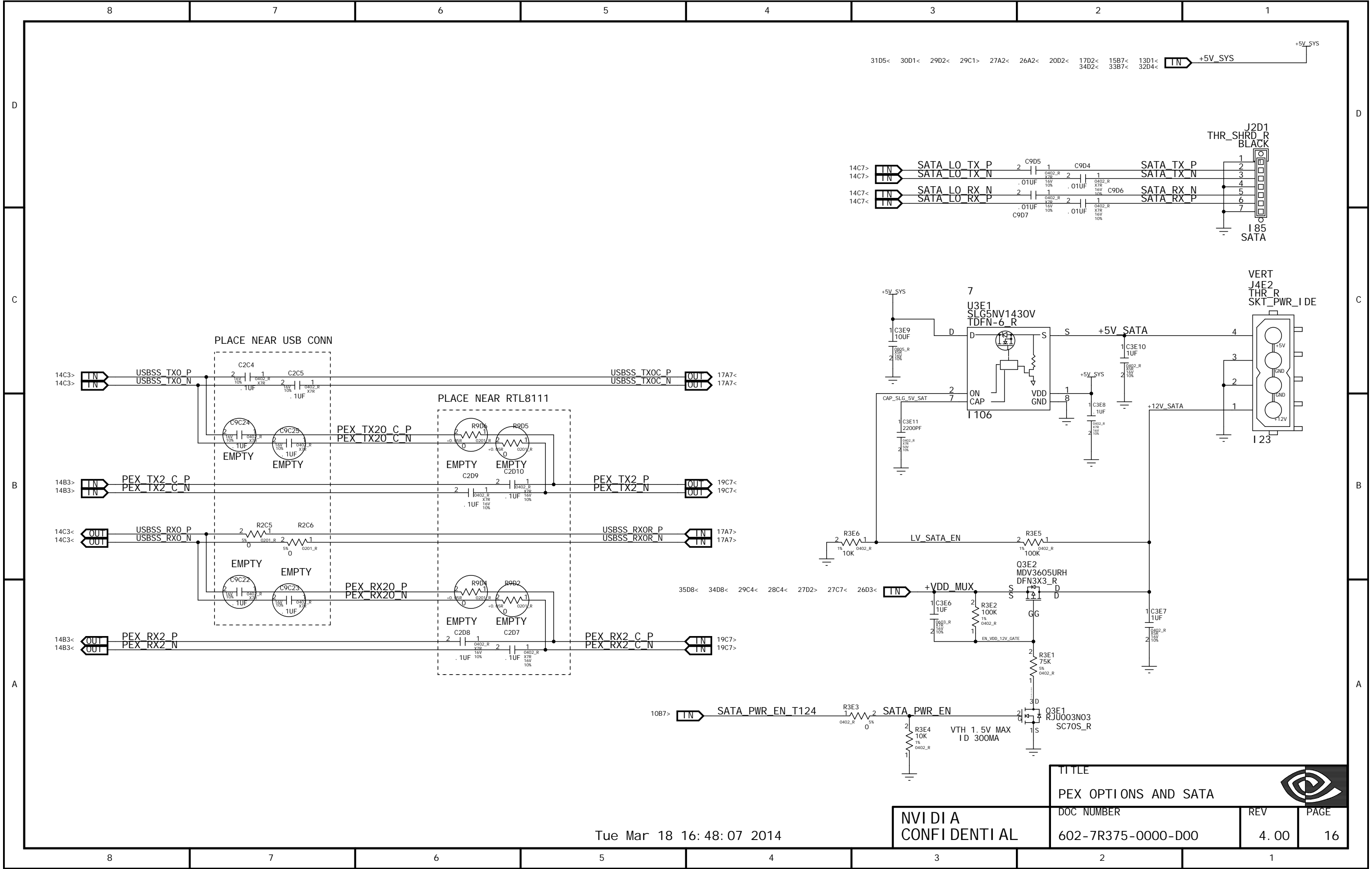
W_DISABLE# PULLUP REQUIRED ON CARD PER SPEC

WI RELESS CARDS CAN WAKE FROM LPO BUT NOT OFF

TITLE			
MINI HALF PCI E			
DOC NUMBER	REV	PAGE	
602-7R375-0000-D00	4.00	15	

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Tue Mar 18 16:48:07 2014

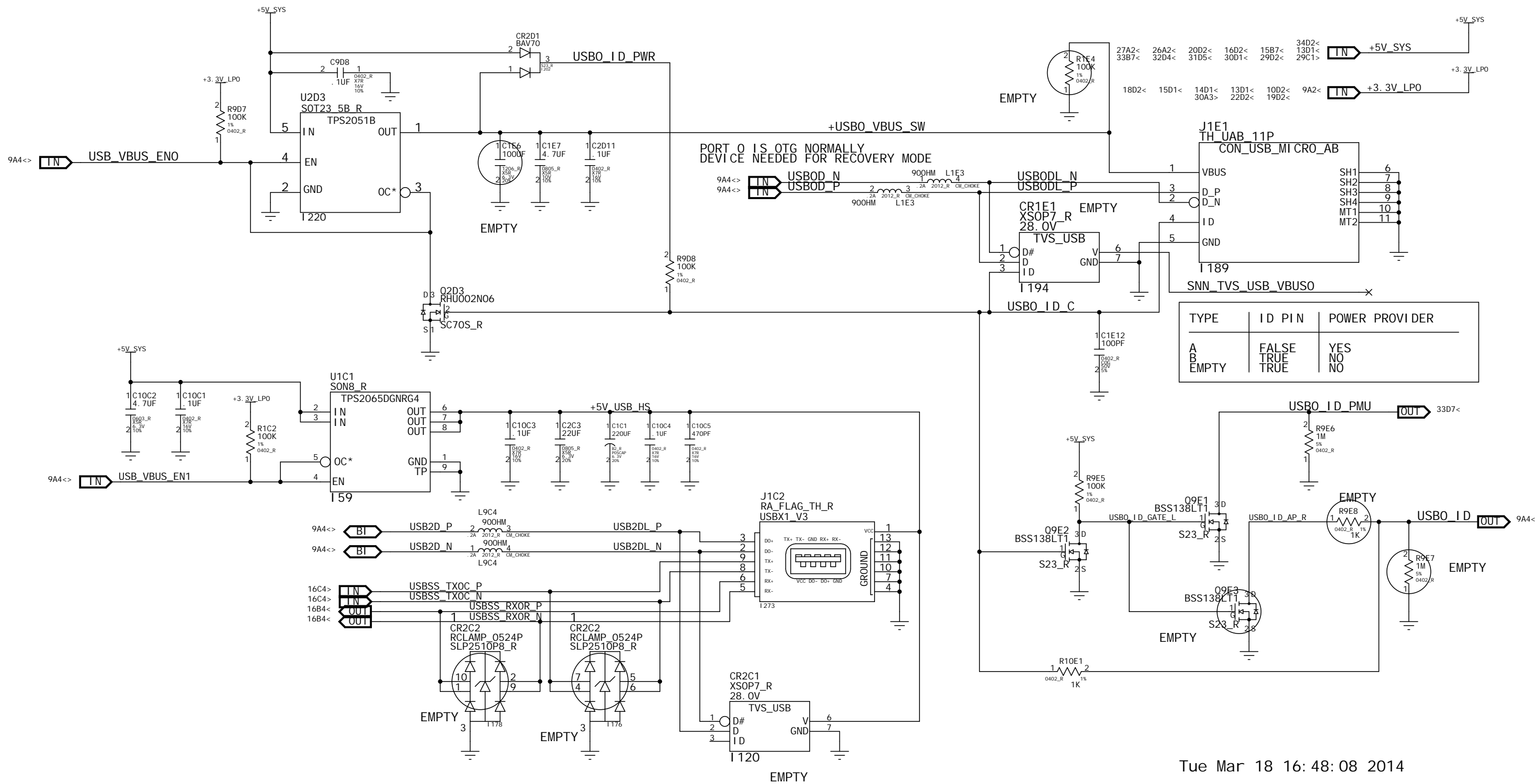


Tue Mar 18 16:48:07 2014

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TITLE		
PEX OPTIONS AND SATA		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.00	16



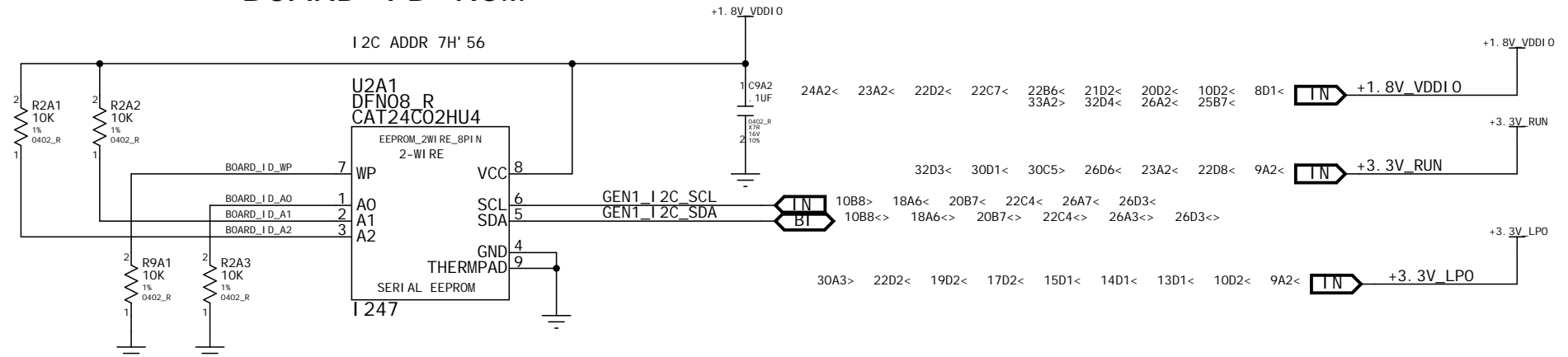


Tue Mar 18 16:48:08 2014

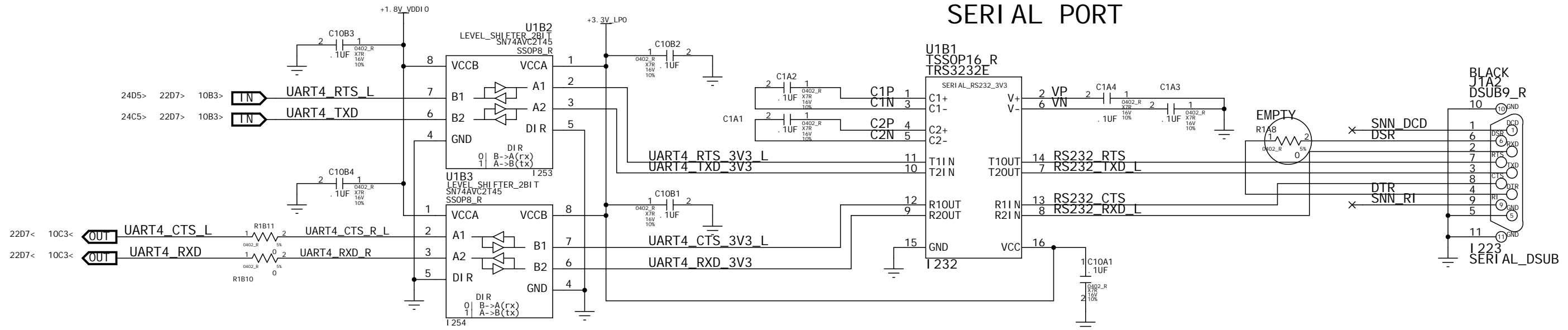
NVI DIA CONFIDENTIAL	TITLE USB PORTS		
	DOC NUMBER 602-7R375-0000-D00	REV 4.00	PAGE 17

BOARD I D ROM

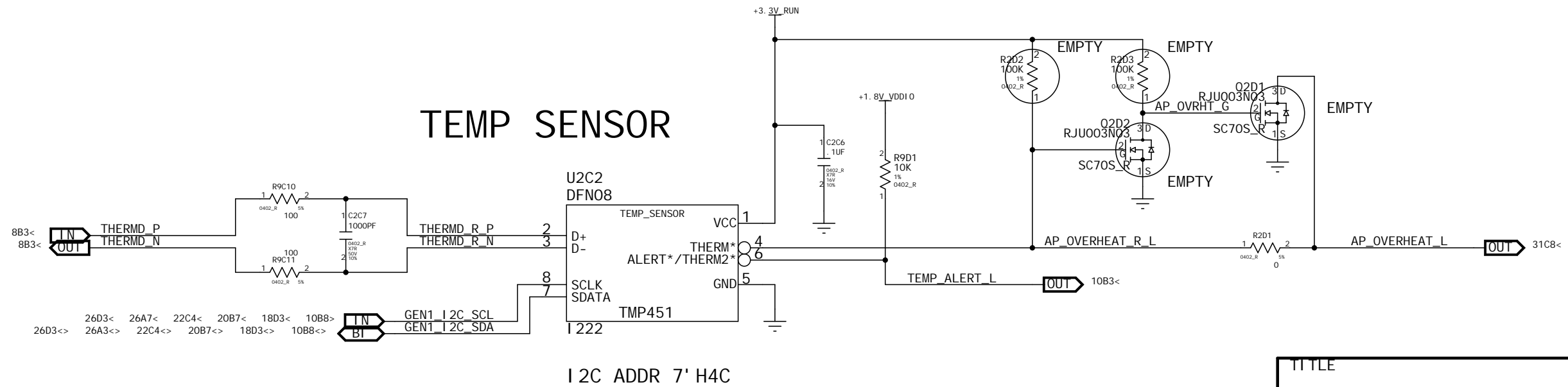
I2C ADDR 7H'56



SERIAL PORT



TEMP SENSOR



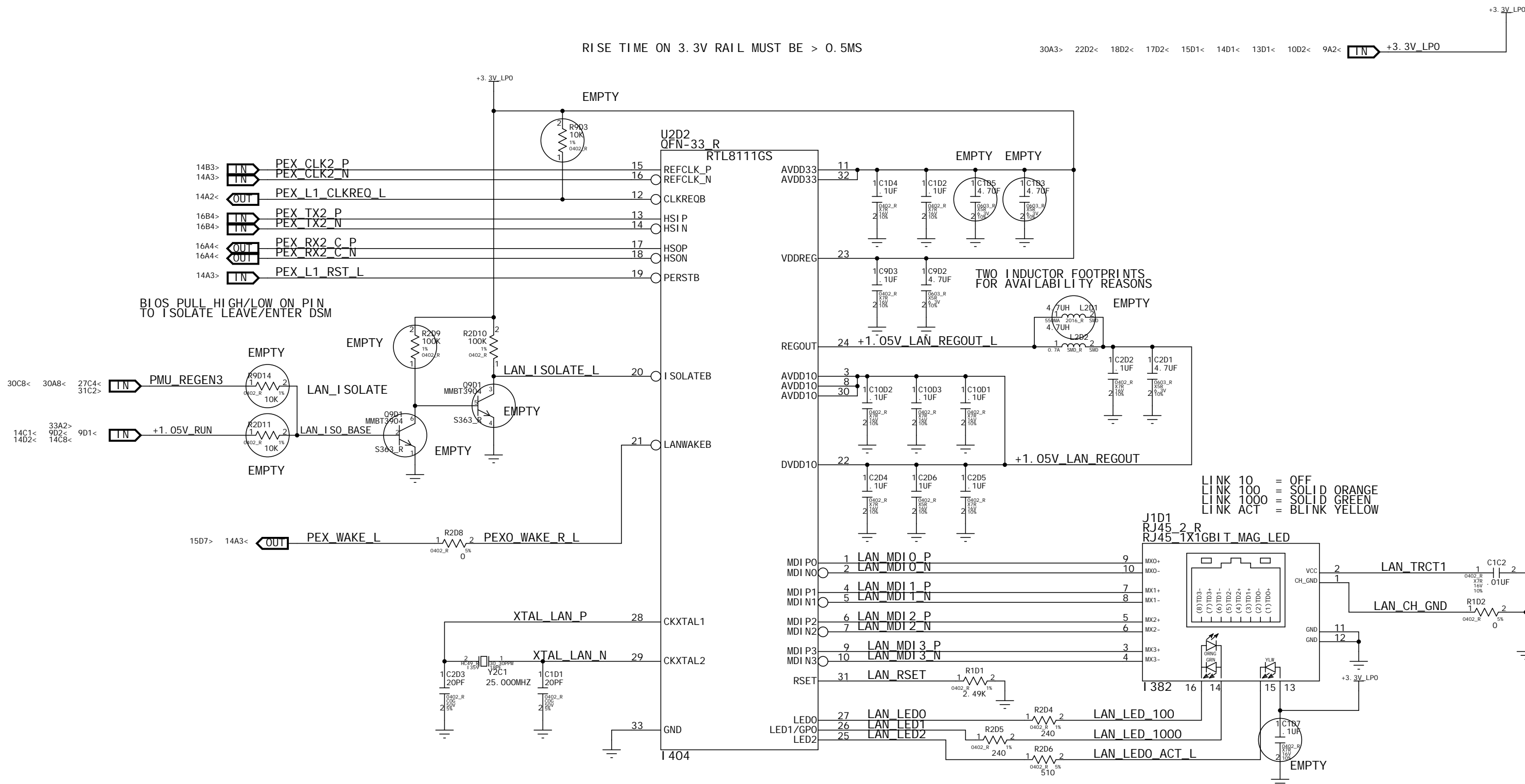
TITLE		
TEMP SENSOR, SERIAL, ID		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.00	18

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Tue Mar 18 16:48:09 2014

RISE TIME ON 3.3V RAIL MUST BE > 0.5MS

30A3> 22D2< 18D2< 17D2< 15D1< 14D1< 13D1< 10D2< 9A2< +3.3V_LPO

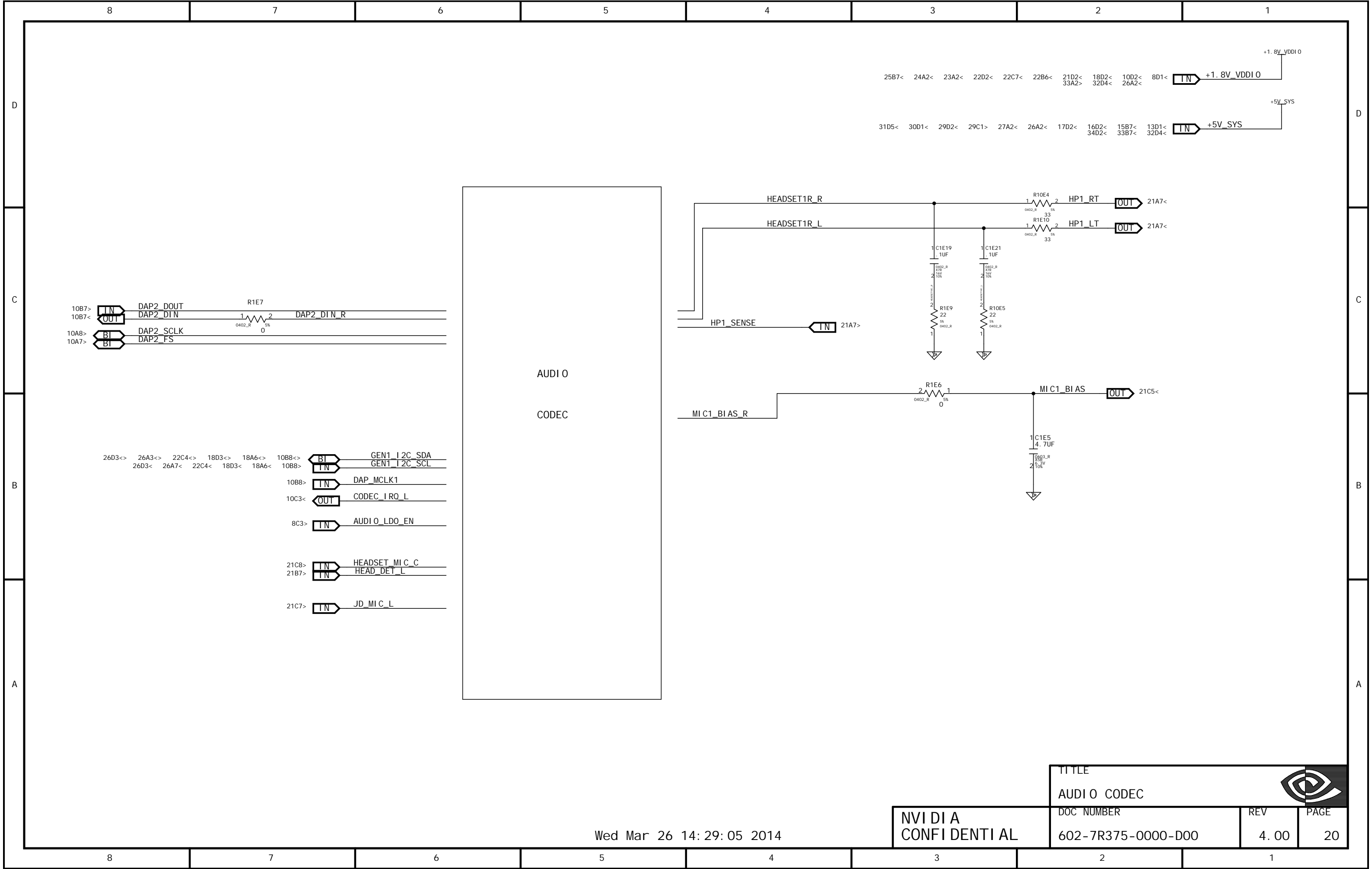


LINK 10 = OFF
 LINK 100 = SOLID ORANGE
 LINK 1000 = SOLID GREEN
 LINK ACT = BLINK YELLOW

TITLE		PEX GIGE LAN/PHY	
DOC NUMBER	REV	PAGE	
602-7R375-0000-D00	4.00	19	


NV I D I A
 C O N F I D E N T I A L

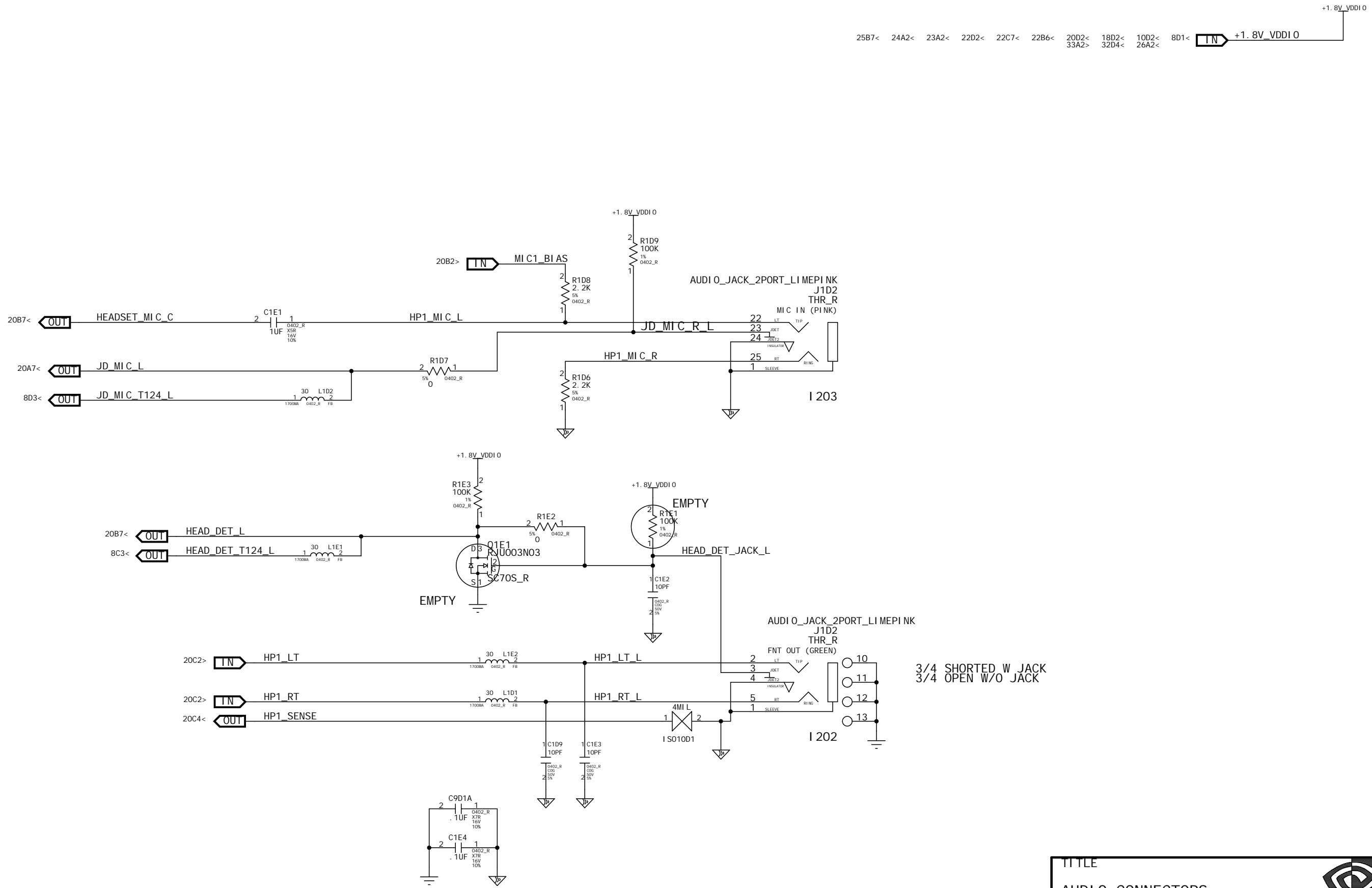
Tue Mar 18 16:48:09 2014



Wed Mar 26 14:29:05 2014

NVIDIA
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TITLE			
AUDIO CODEC			
DOC NUMBER	REV	PAGE	
602-7R375-0000-D00	4.00	20	



25B7< 24A2< 23A2< 22D2< 22C7< 22B6< 20D2< 18D2< 10D2< 8D1< +1.8V_VDDI0

3/4 SHORTED W JACK
3/4 OPEN W/O JACK

Tue Mar 18 16:48:10 2014

NV I D I A
C O N F I D E N T I A L

TITLE		
AUDIO CONNECTORS		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.00	21

D

C

B

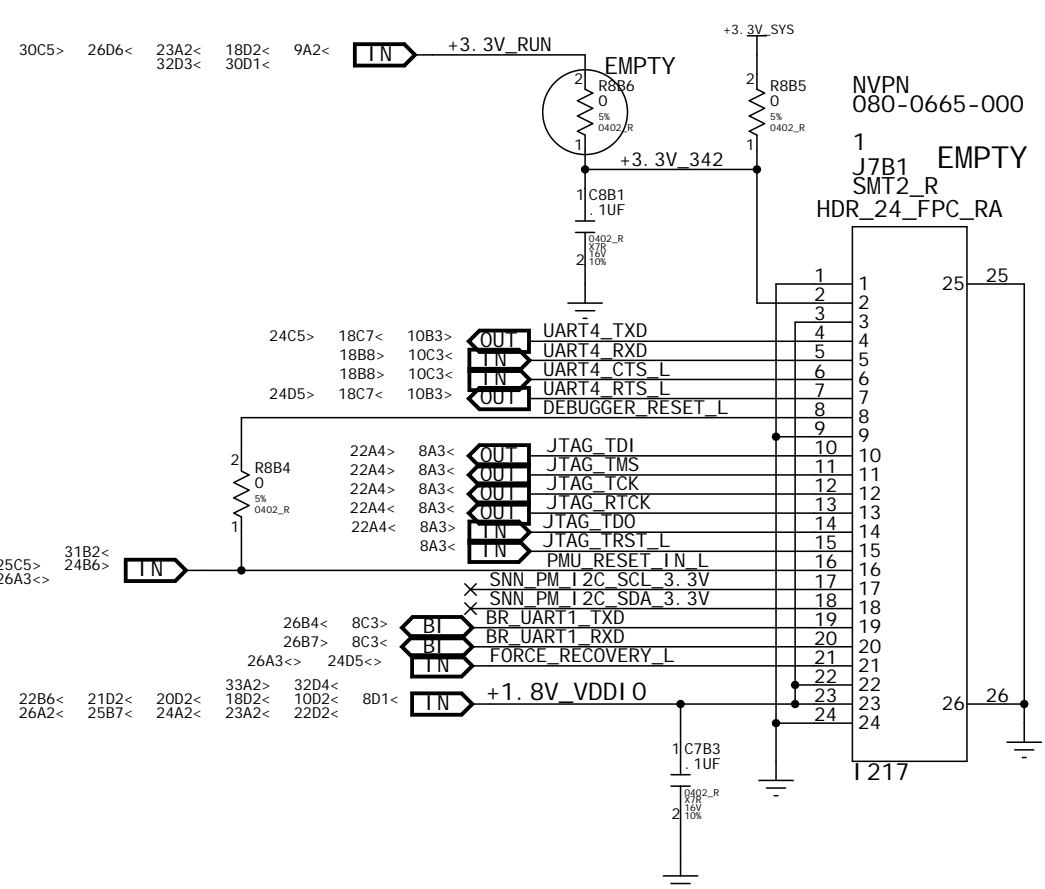
A

D

C

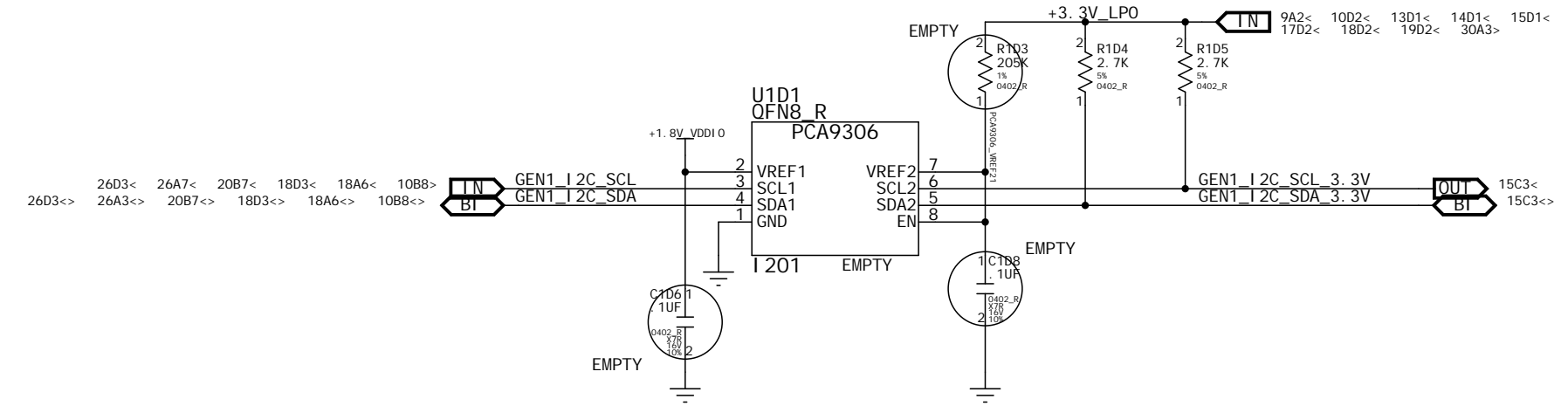
B

A

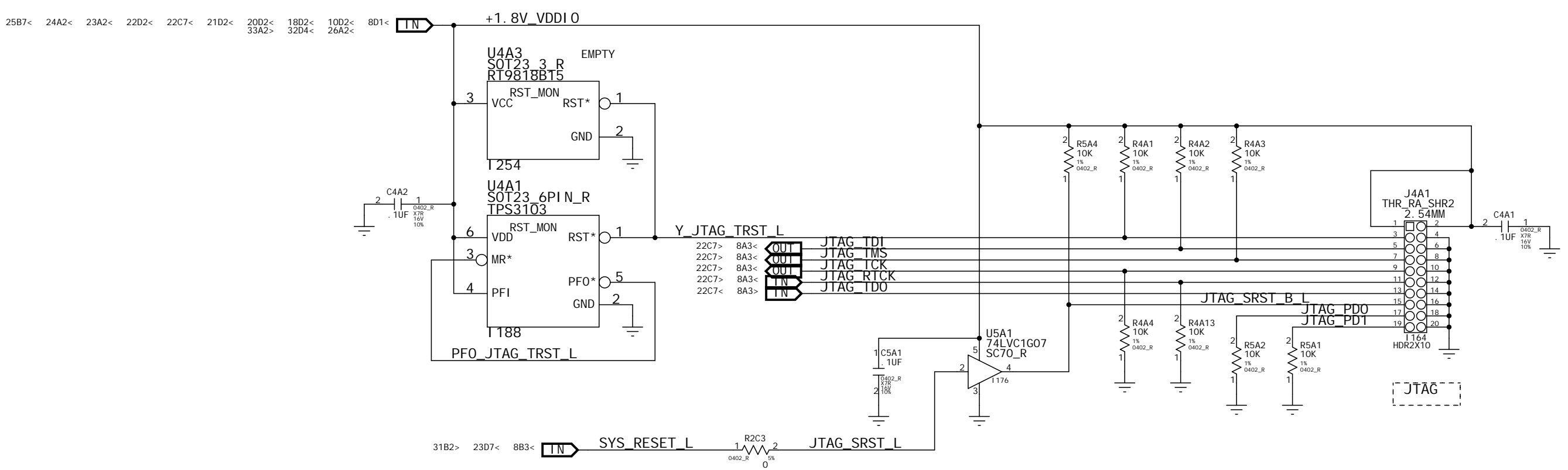



STUFF THIS DEBUG CONN
OR JTAG & DSUB, NOT BOTH

I2C LEVEL TRANSLATOR



RESET SUPERVISOR ALLOWS EXTERNAL ARM JTAG DEBUGGER TO DETECT POWER CYCLE
DEPOPULATE SUPERVISOR FOR PRODUCTION VERSIONS?

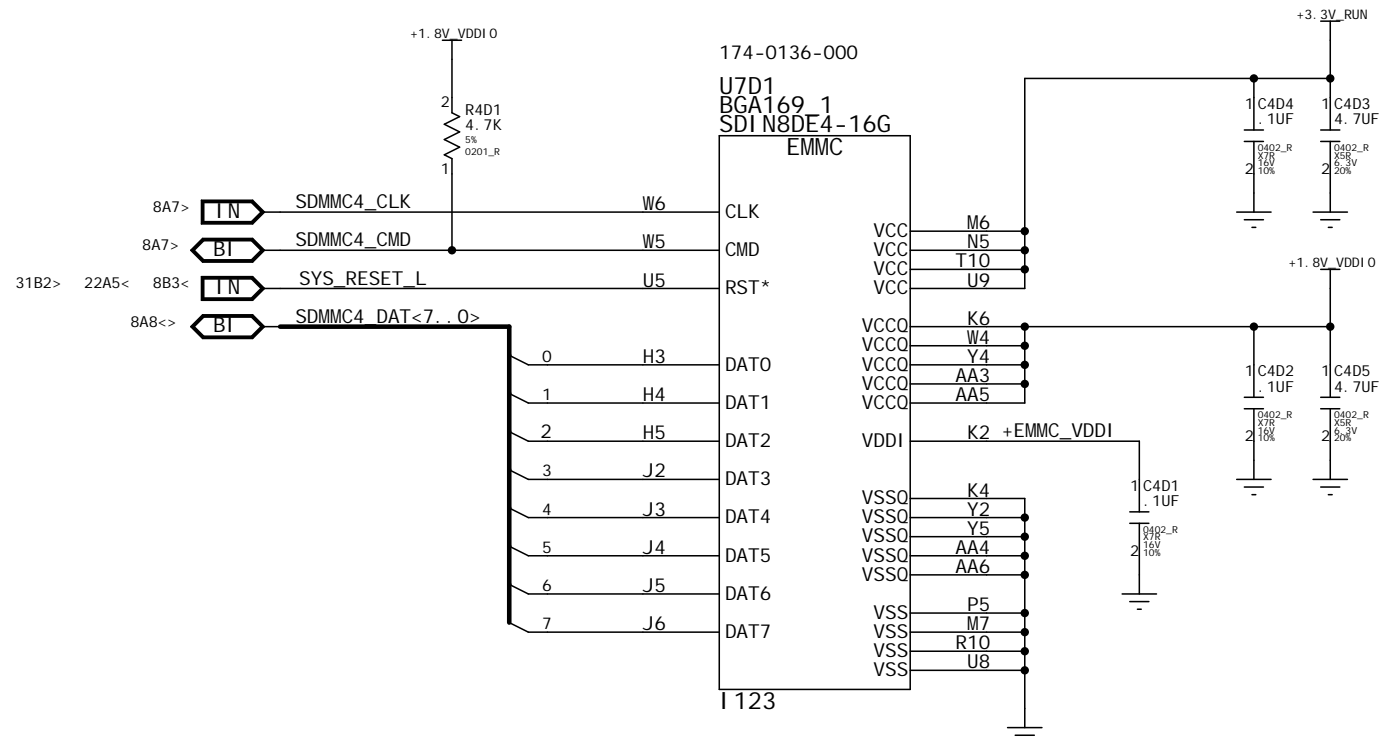


TITLE			
JTAG CONN; I2C TRANSLATER			
DOC NUMBER	REV	PAGE	
602-7R375-0000-D00	4.00	22	

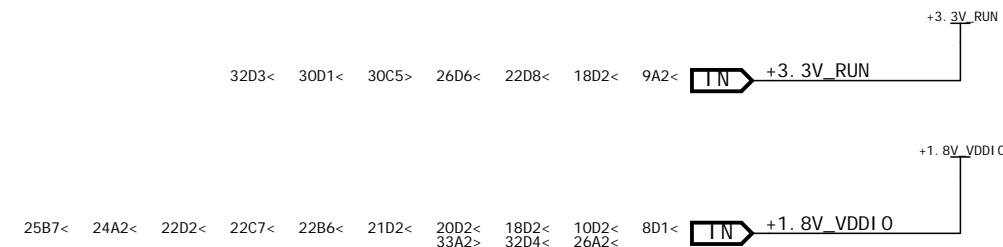
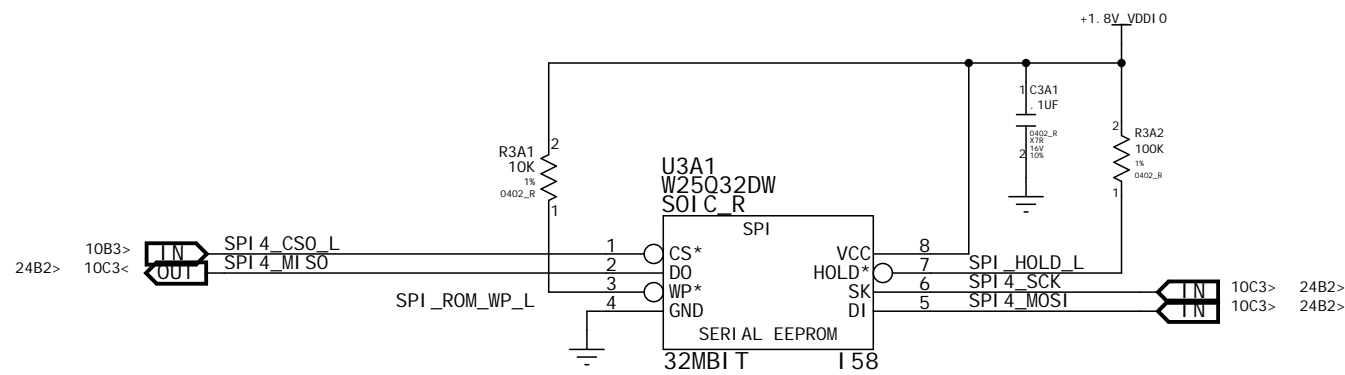
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Tue Mar 18 16:48:11 2014

EMMC 4.51



SPI BOOT ROM



TITLE			
EMMC, SPI ROM			
DOC NUMBER	REV	PAGE	
602-7R375-0000-D00	4.00	23	

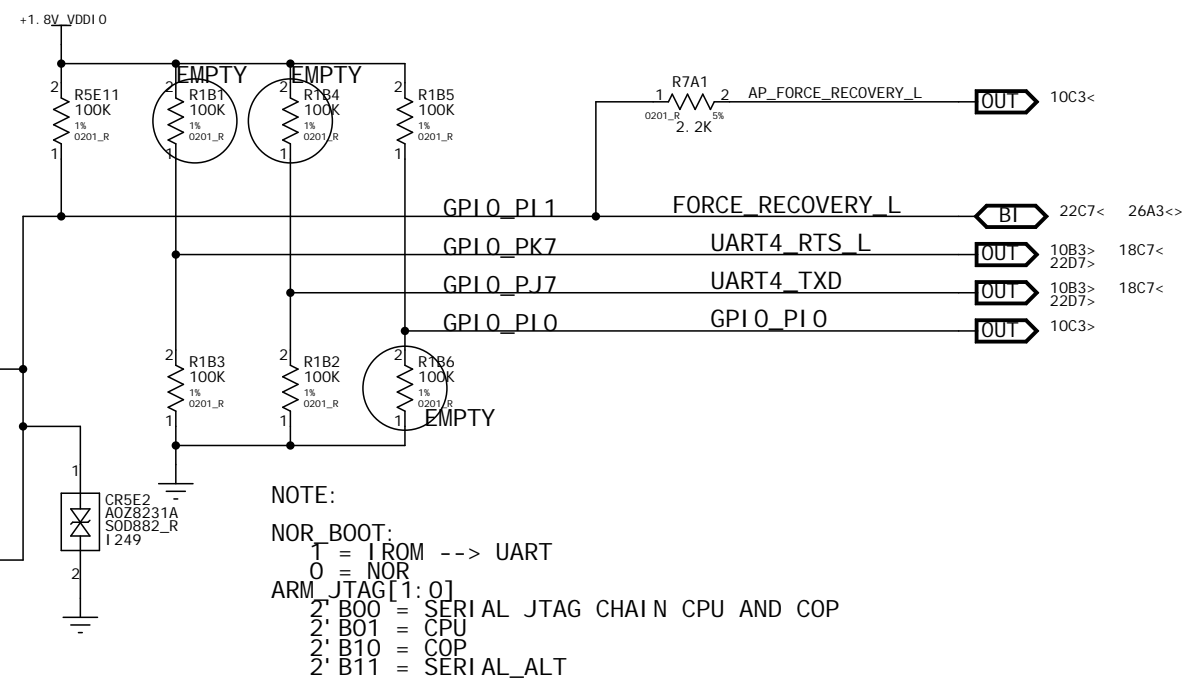
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Tue Mar 18 16:48:12 2014

FORCE_RECOVERY
BUTTON

SW5E2
THICK_UNI V
BUTTON_6P
J LEAD

PHI DGET
EMPTY
J5E1
THR
185



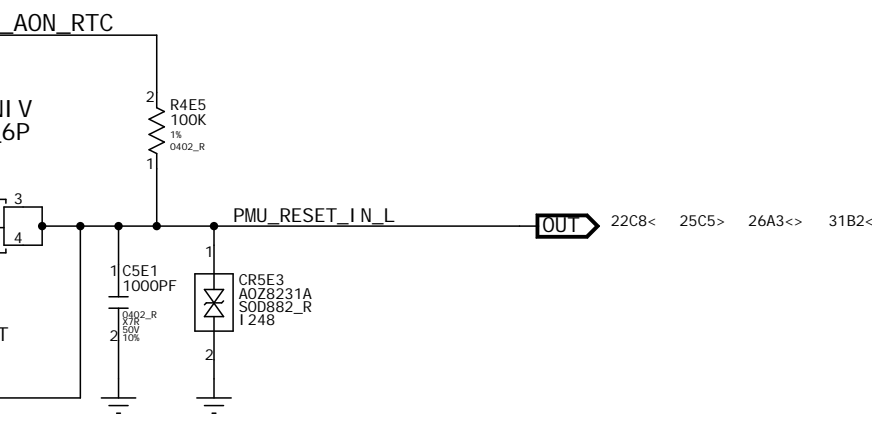
NOTE:
NOR_BOOT:
1 = IROM --> UART
0 = NOR
ARM_JTAG[1:0]:
2' B00 = SERIAL JTAG CHAIN CPU AND COP
2' B01 = CPU
2' B10 = COP
2' B11 = SERIAL_ALT

31C6< 31B7> 24A8<
31C8< +2.5V_AON_RTC

RESET
BUTTON

SW5E1
THICK_UNI V
BUTTON_6P
J LEAD

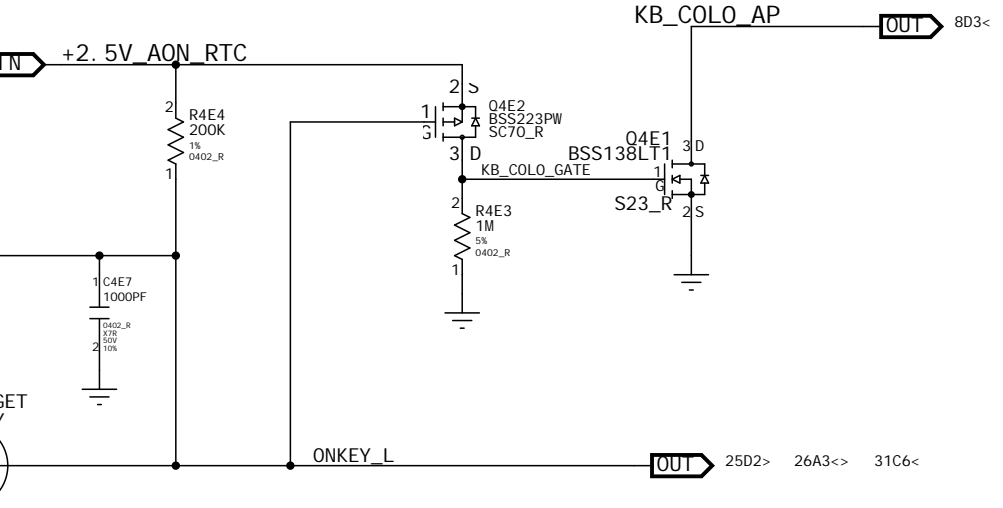
PHI DGET
EMPTY
J5E2
THR
181



POWER
BUTTON

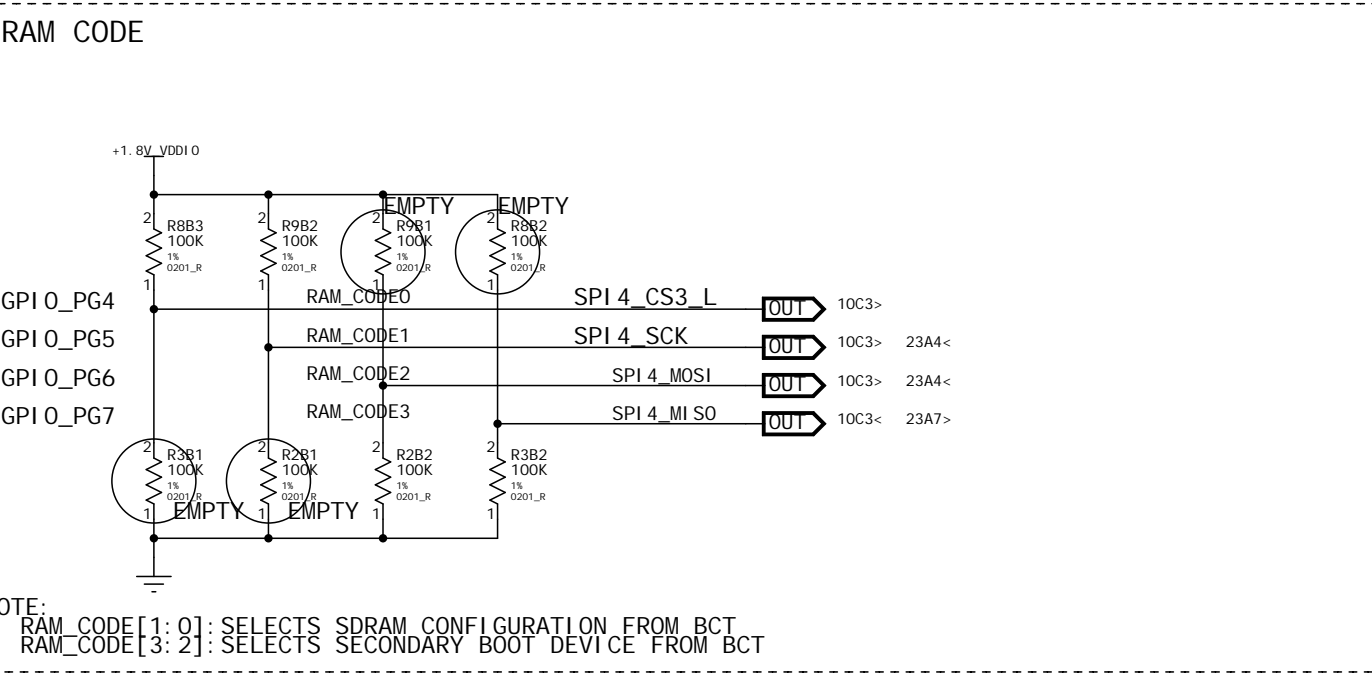
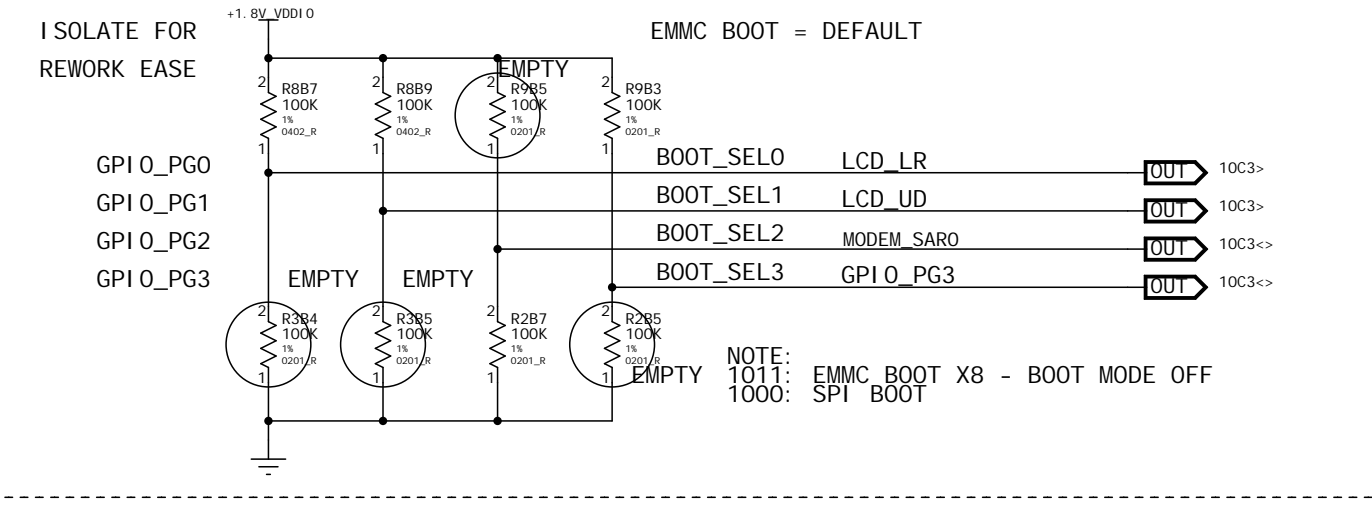
SW4E1
THICK_UNI V
BUTTON_6P
J LEAD

PHI DGET
EMPTY
J4E1
THR
1103

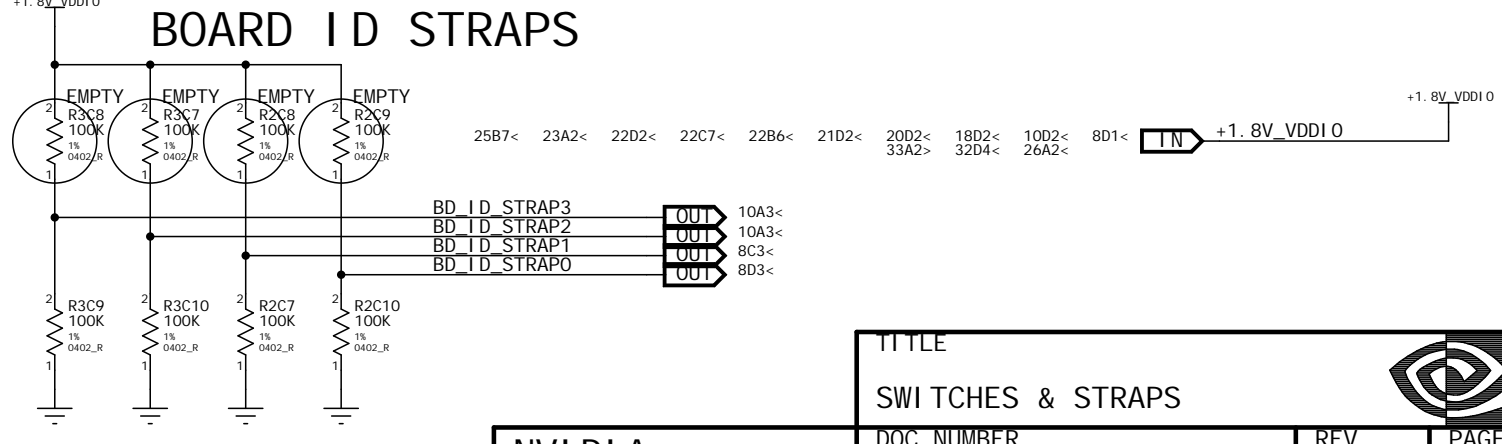


KB_COLO_AP (OUT) 8D3<

ONKEY_L (OUT) 25D2> 26A3<> 31C6<



NOTE:
RAM_CODE[1:0]: SELECTS SDRAM CONFIGURATION FROM BCT
RAM_CODE[3:2]: SELECTS SECONDARY BOOT DEVICE FROM BCT



BOARD ID STRAPS

TITLE		
SWITCHES & STRAPS		
DOC NUMBER	REV	PAGE
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NVIDIA
CONFIDENTIAL

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D

C

B

A

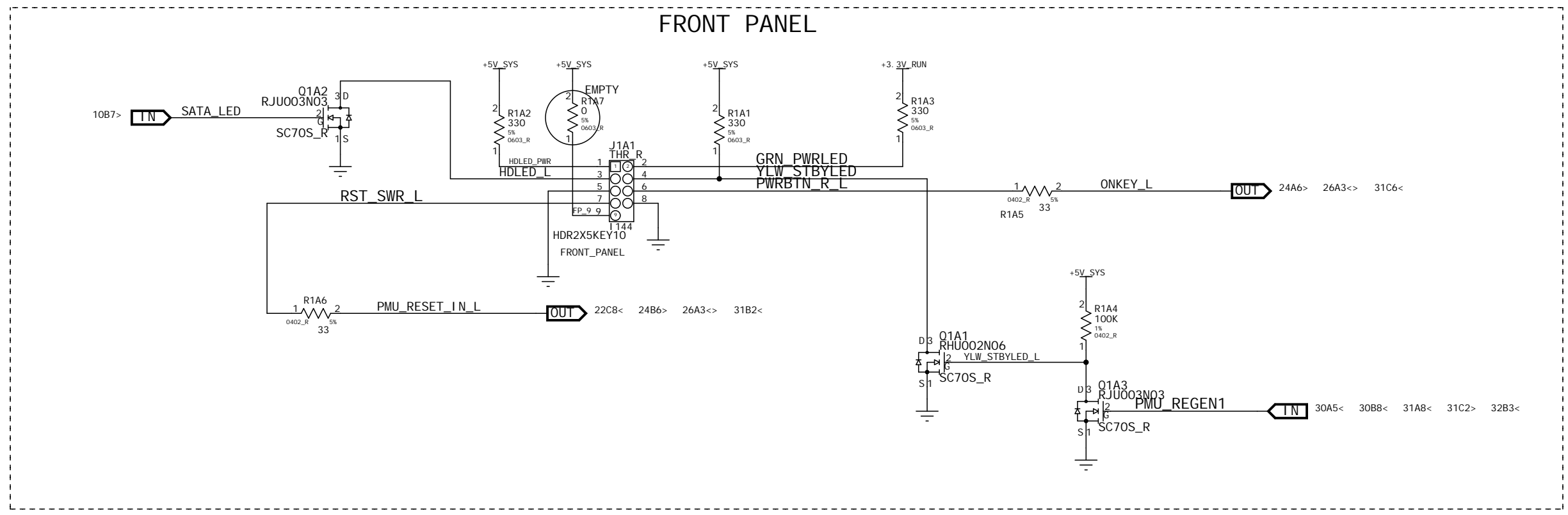
D

C

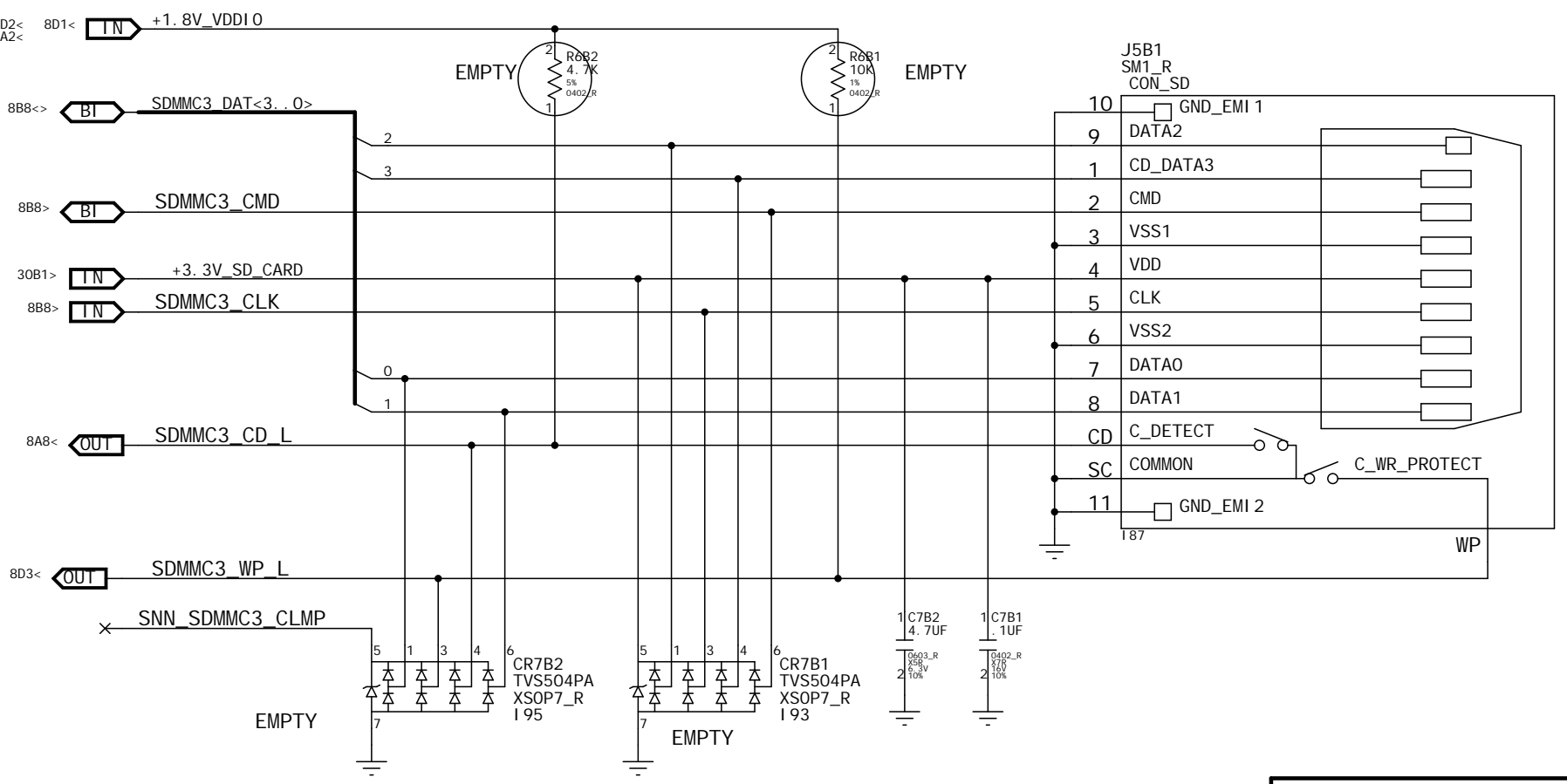
B

A

FRONT PANEL



23A2< 22D2< 22C7< 22B6< 21D2< 20D2< 18D2< 10D2< 8D1< 8B8<> 8B8> 30B1> 8B8> 8A8< 8D3< SNN_SDMMC3_CLMP



TITLE		
SD CONN & FRONT PANEL HDR		
DOC NUMBER	REV	PAGE
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NVI DIA
CONFIDENTIAL

Tue Mar 18 16:48:13 2014

D

C

B

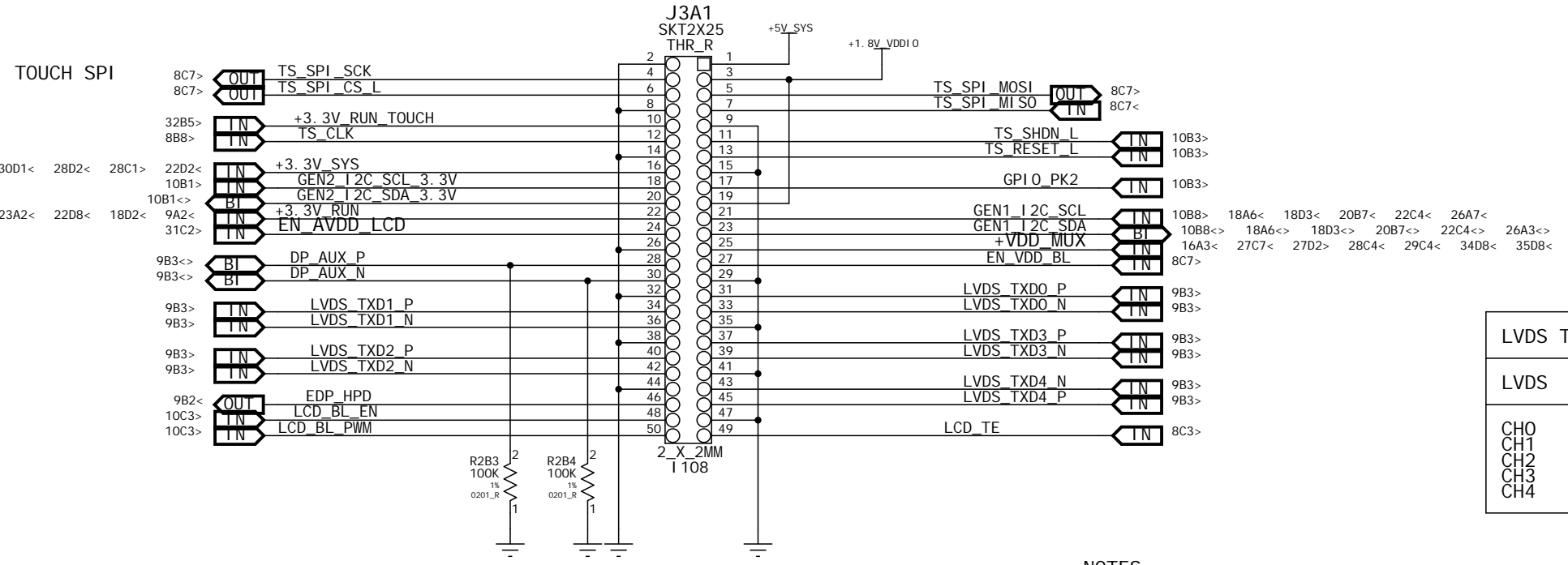
A

D

C

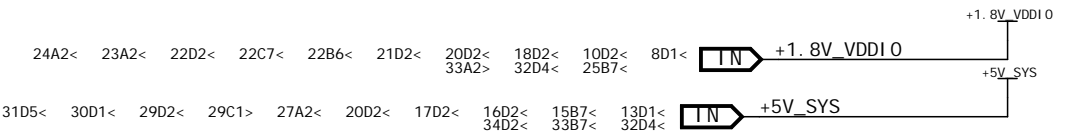
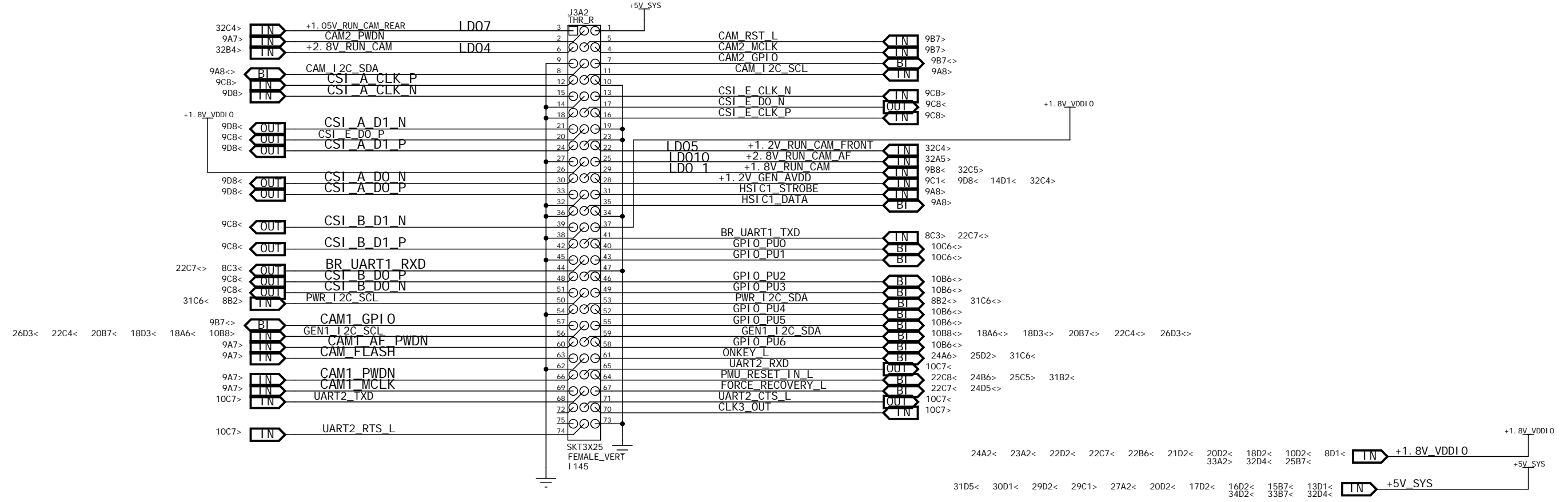
B


A



LVDS TO EDP MUX	
LVDS	EDP
CH0	CH2
CH1	CH1
CH2	CH0
CH3	---
CH4	CH3

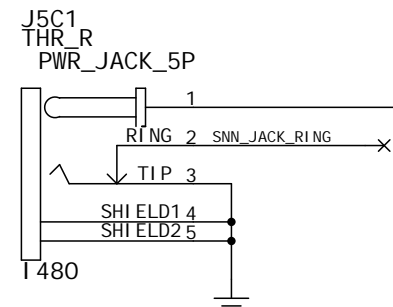
NOTES:
LVDS / EDP MODULES MAY USE +3.3V_RUN
OR +3.3V_RUN GATED BY EN_AVDD_LCD (PMI C GPI04)



TITLE			
EXP: TOUCH/DI SP & GENERAL			
DOC NUMBER	REV	PAGE	
602-7R375-0000-D00	4.00	26	

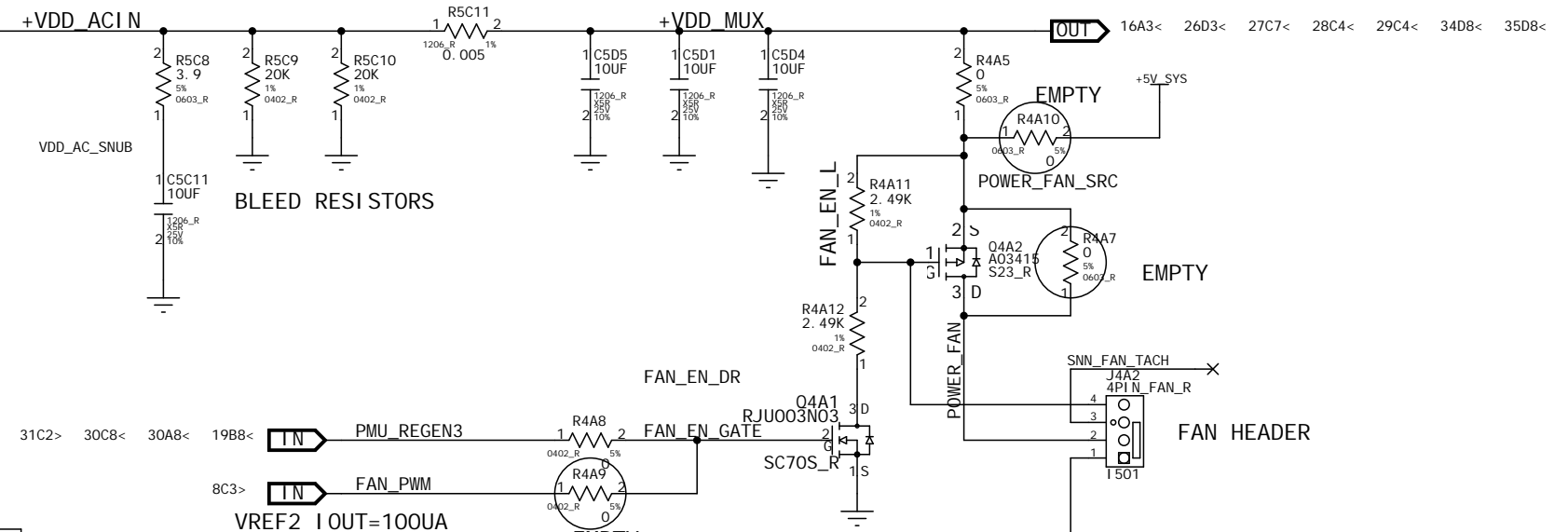
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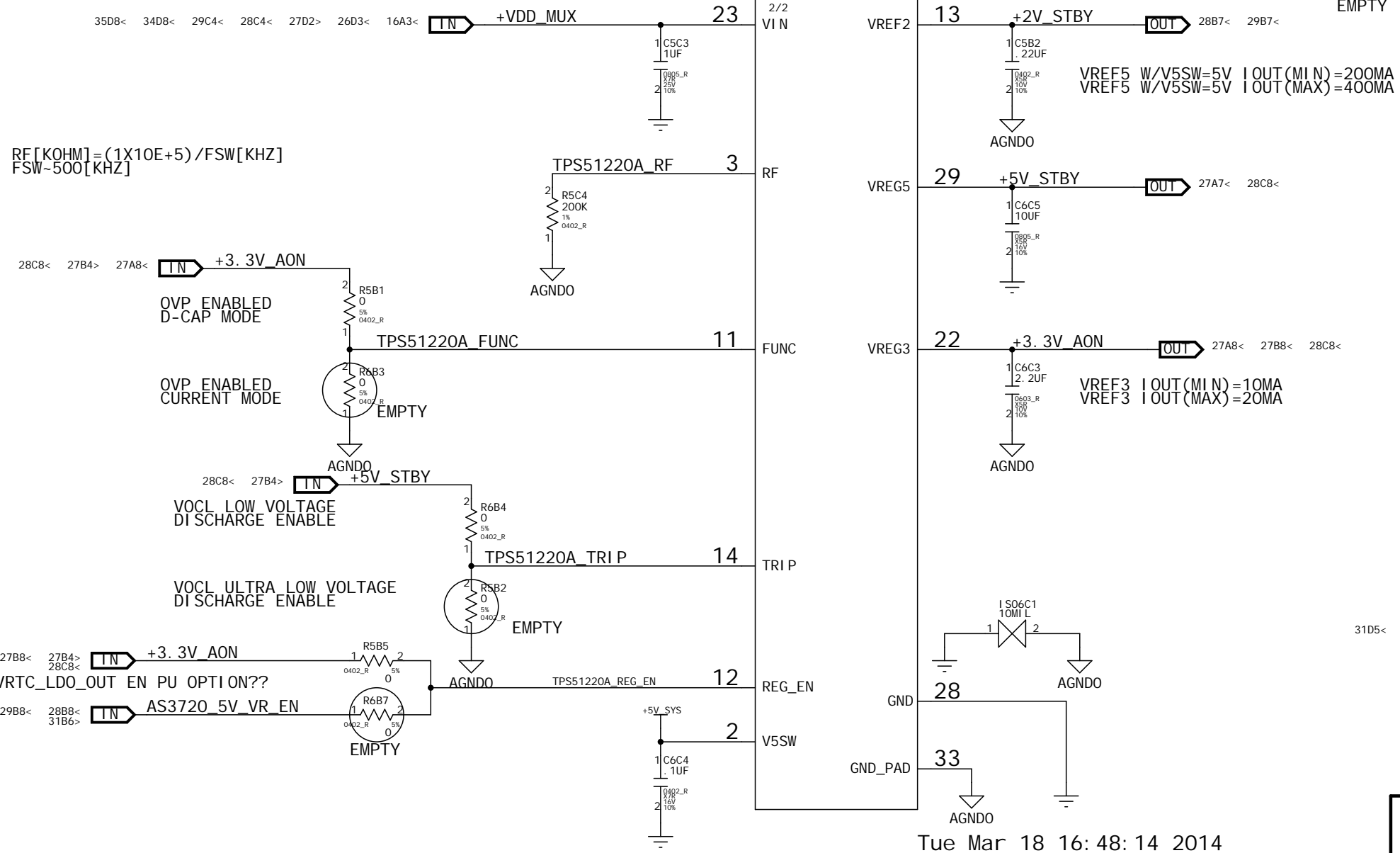
AC JACK

750-0147-000 FOR 12V BRICK
030-0364-000 FOR AC POWER CORD



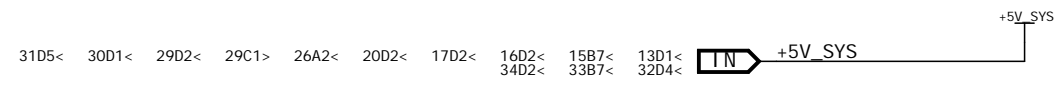
U5C1

U_SWREG_TPS51220
QFN32



$$RF[KOHM] = (1 \times 10^5) / FSW[KHZ]$$

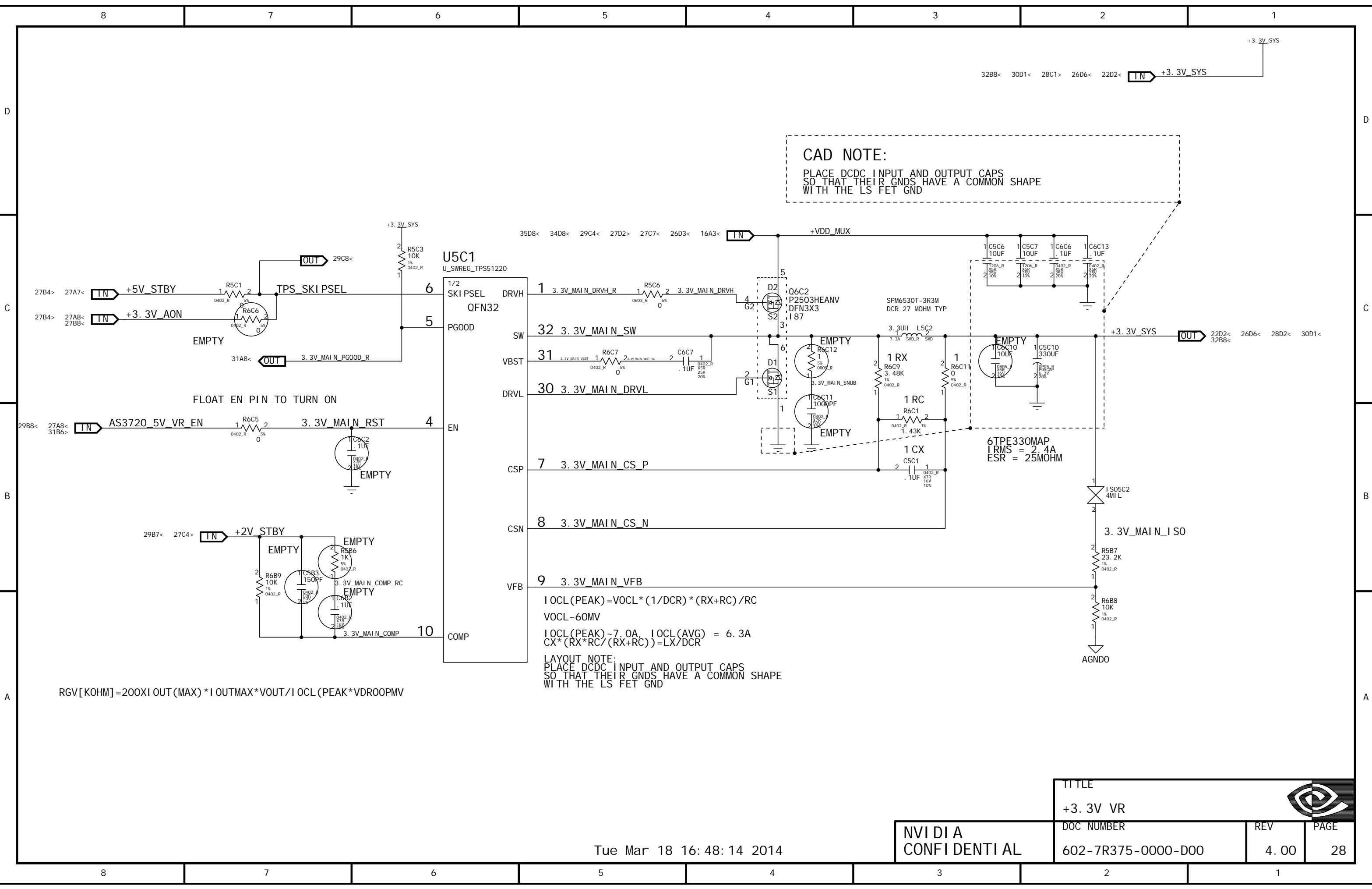
FSW=500[KHZ]



TITLE			
DC IN			
DOC NUMBER	REV	PAGE	
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CAD NOTE:
 PLACE DCDC INPUT AND OUTPUT CAPS
 SO THAT THEIR GNDS HAVE A COMMON SHAPE
 WITH THE LS FET GND

35D8< 34D8< 29C4< 27D2> 27C7< 26D3< 16A3< TN

U5C1
 U_SWREG_TPS51220

1/2 SKI PSEL DRVH 1 3.3V_MAIN_DRVH_R R5C6 2 3.3V_MAIN_DRVH 4 G2 S2 Q6C2 P2503HEANV DFN3X3 1.87

PGOOD 5 31A8< OUT 3.3V_MAIN_PGOOD_R

SW 32 3.3V_MAIN_SW

VBST 31 3.3V_MAIN_VBST R6C7 2 3.3V_MAIN_VBST_RC C6C7 1 0402_R 1.1UF X5R 25V 20%

DRVH 30 3.3V_MAIN_DRVH

EN 4 29B8< 27A8< 31B6> AS3720_5V_VR_EN R6C5 1 0402_R 5% 3.3V_MAIN_RST C6C2 1 0402_R 10UF

CSP 7 3.3V_MAIN_CS_P

CSN 8 3.3V_MAIN_CS_N


VFB 9 3.3V_MAIN_VFB

COMP 10

1 OCL (PEAK) = VOCL * (1/DCR) * (RX+RC) / RC
 VOCL ~ 60MV
 I OCL (PEAK) ~ 7.0A, I OCL (AVG) = 6.3A
 CX * (RX*RC / (RX+RC)) = LX / DCR

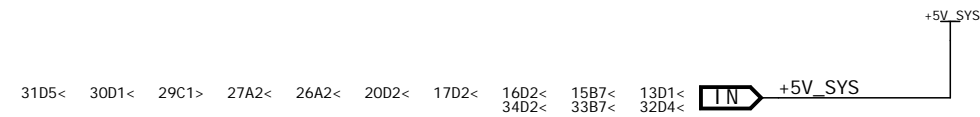
LAYOUT NOTE:
 PLACE DCDC INPUT AND OUTPUT CAPS
 SO THAT THEIR GNDS HAVE A COMMON SHAPE
 WITH THE LS FET GND

$RGV [KOHM] = 200 \times I_{OUT(MAX)} \times V_{OUT} / I_{OCL(PEAK \times V_{DROOPMV})}$

TITLE			
+3.3V VR			
DOC NUMBER	REV	PAGE	
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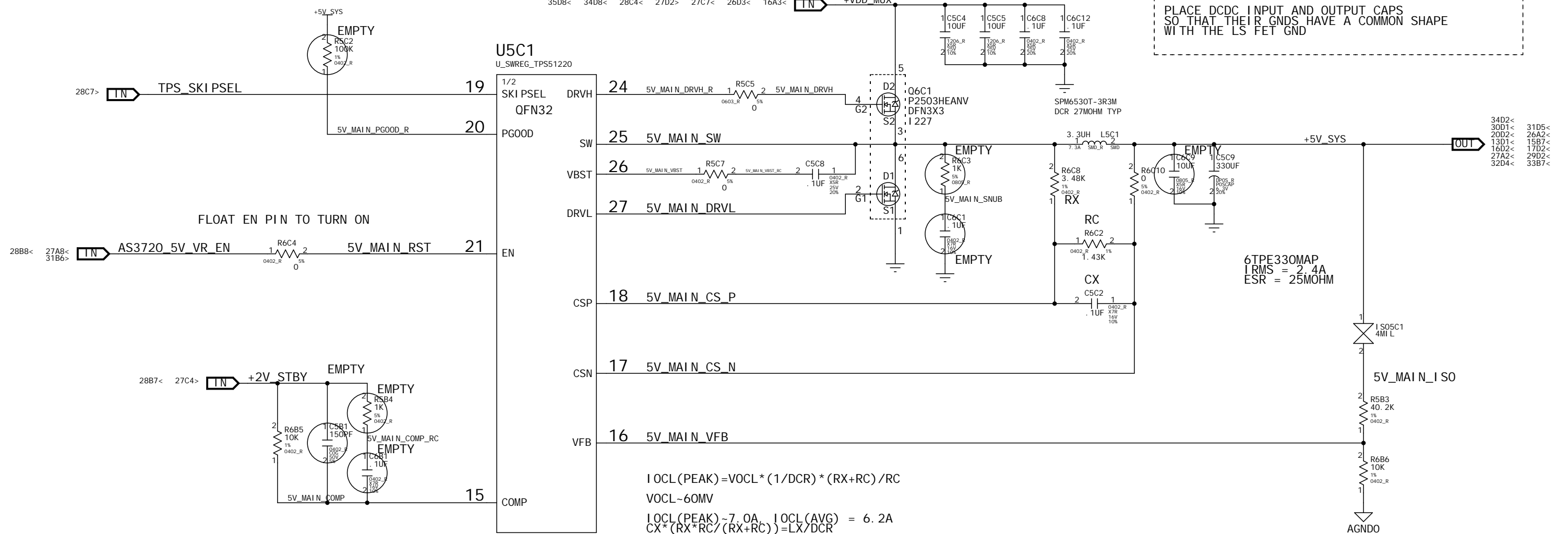
Tue Mar 18 16:48:14 2014



$I_{OCL(PEAK)} = VO_{CL} * (1/DCR) * (RX+RC) / RC$
 $VO_{CL} \sim 60MV$
 $I_{OCL(PEAK)} \sim 9.8A$
 $CX * (RX * RC / (RX + RC)) = LX / DCR$

LAYOUT NOTE:
PLACE DCDC INPUT AND OUTPUT CAPS
SO THAT THEIR GNDS HAVE A COMMON SHAPE
WITH THE LS FET GND

CAD NOTE:
PLACE DCDC INPUT AND OUTPUT CAPS
SO THAT THEIR GNDS HAVE A COMMON SHAPE
WITH THE LS FET GND



FLOAT EN PIN TO TURN ON

$RGV[KOHM] = 200XI_{OUT(MAX)} * I_{OUTMAX} * V_{OUT} / I_{OCL(PEAK * VDROOPMV)}$

$I_{OCL(PEAK)} = VO_{CL} * (1/DCR) * (RX+RC) / RC$
 $VO_{CL} \sim 60MV$
 $I_{OCL(PEAK)} \sim 7.0A$, $I_{OCL(AVG)} = 6.2A$
 $CX * (RX * RC / (RX + RC)) = LX / DCR$

LAYOUT NOTE:
PLACE DCDC INPUT AND OUTPUT CAPS
SO THAT THEIR GNDS HAVE A COMMON SHAPE
WITH THE LS FET GND

TITLE			
+5V VR			
DOC NUMBER	REV	PAGE	
602-7R375-0000-D00	4.00	29	

NVI DIA
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D

C

B

A

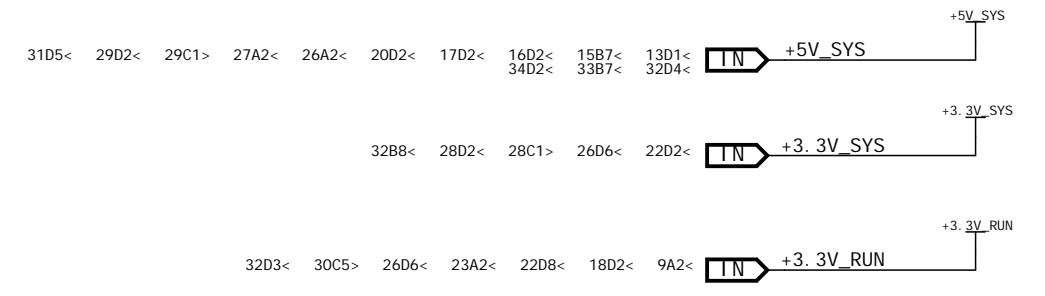
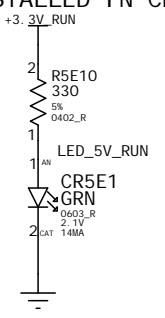
D

C

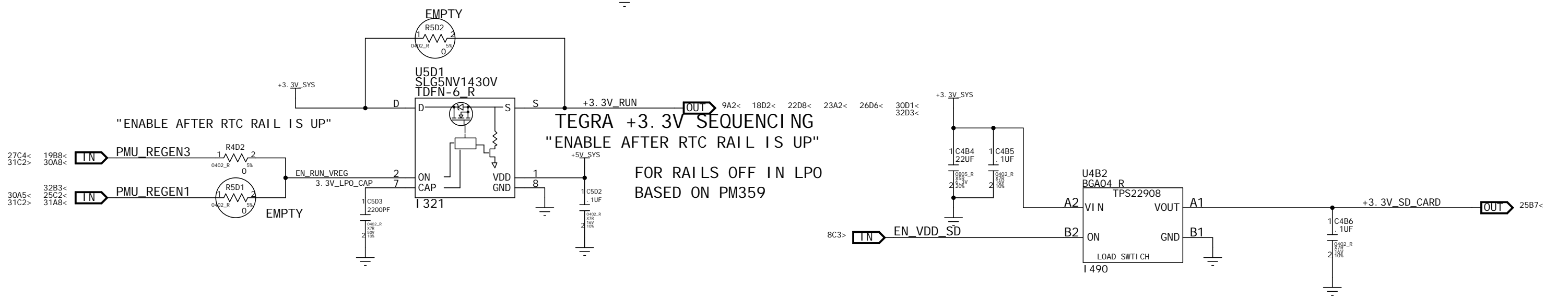
B

A

DE-POP WHEN INSTALLED IN CHASSIS



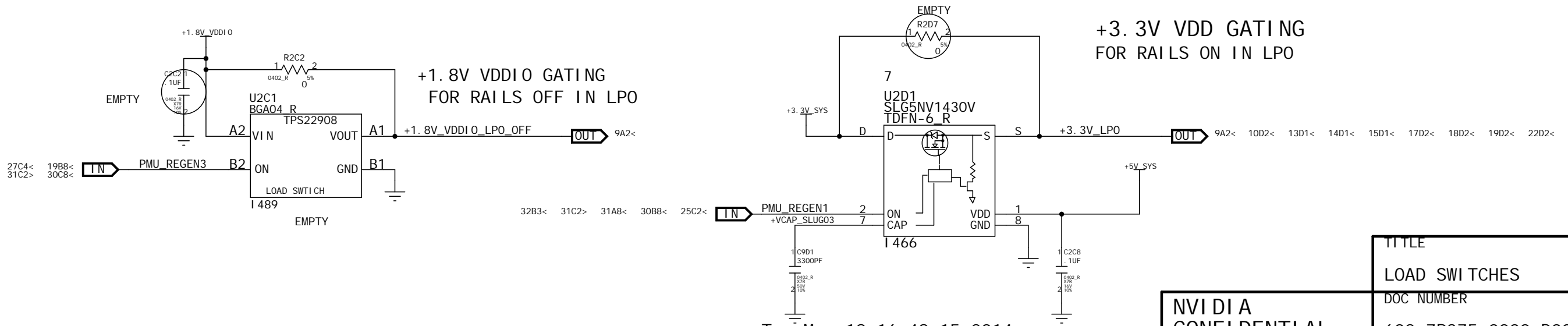
"ENABLE AFTER RTC RAIL IS UP"
 "TEGRA +3.3V SEQUENCING"
 "ENABLE AFTER RTC RAIL IS UP"



TEGRA +1.8V VDDIO SEQUENCING


+1.8V VDDIO GATING FOR RAILS OFF IN LPO

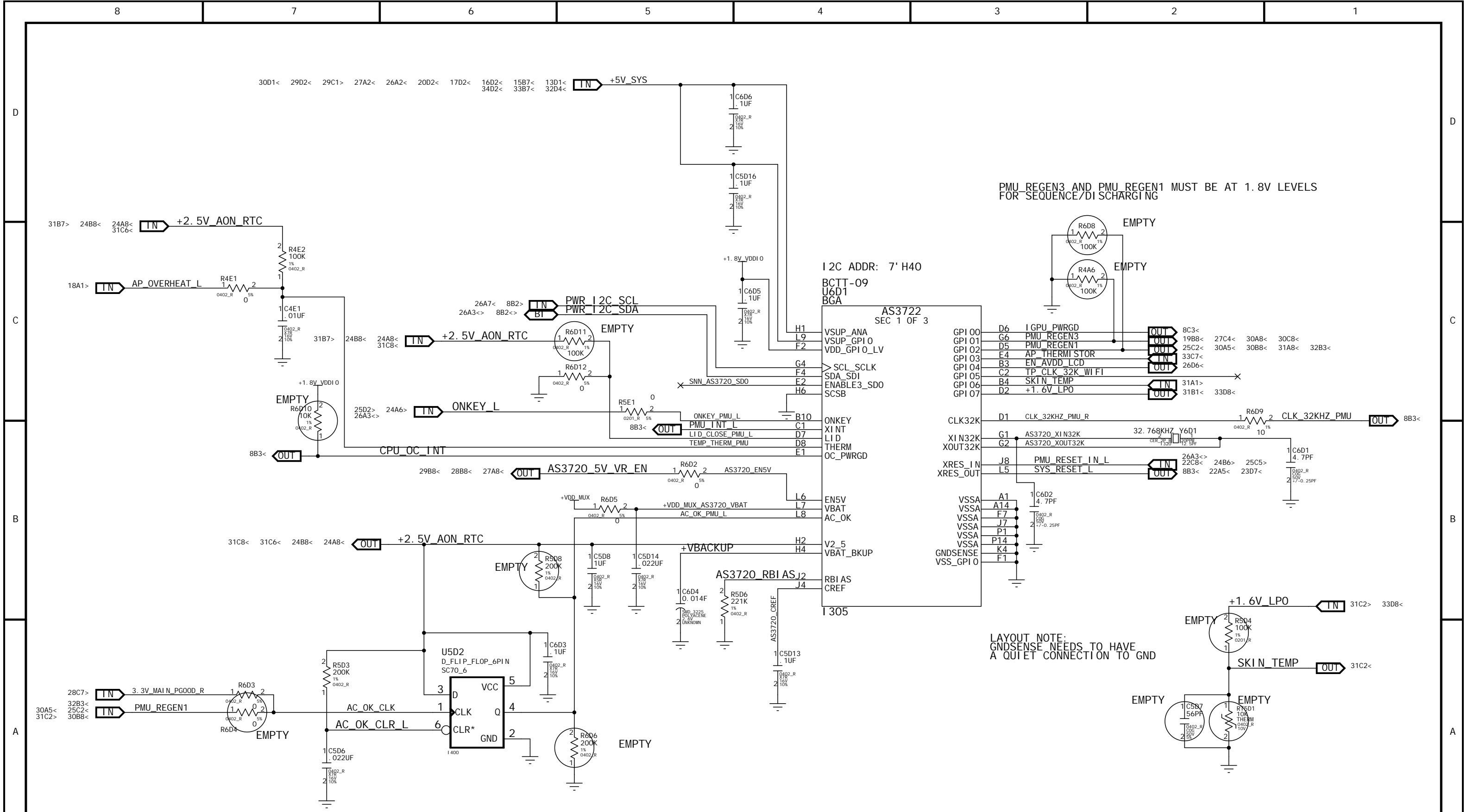
+3.3V VDD GATING FOR RAILS ON IN LPO



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TITLE			
LOAD SWITCHES			
DOC NUMBER	REV	PAGE	
602-7R375-0000-D00	4.00	30	



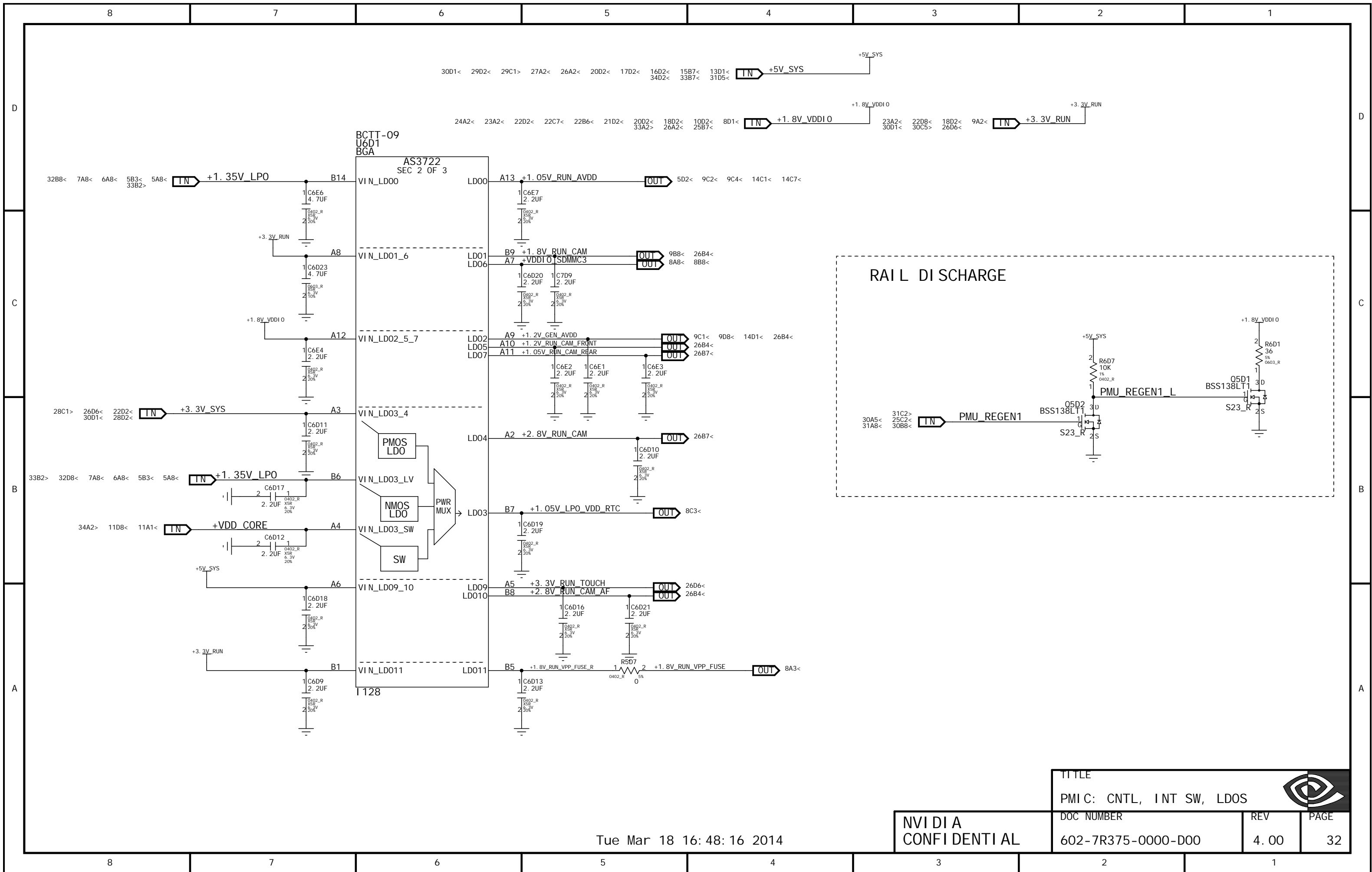
PMU_REGEN3 AND PMU_REGEN1 MUST BE AT 1.8V LEVELS FOR SEQUENCE/DI SCHARGING

LAYOUT NOTE: GNDSENSE NEEDS TO HAVE A QUIET CONNECTION TO GND

TITLE			
PMIC: LOGIC AND GPIOs			
DOC NUMBER	REV	PAGE	
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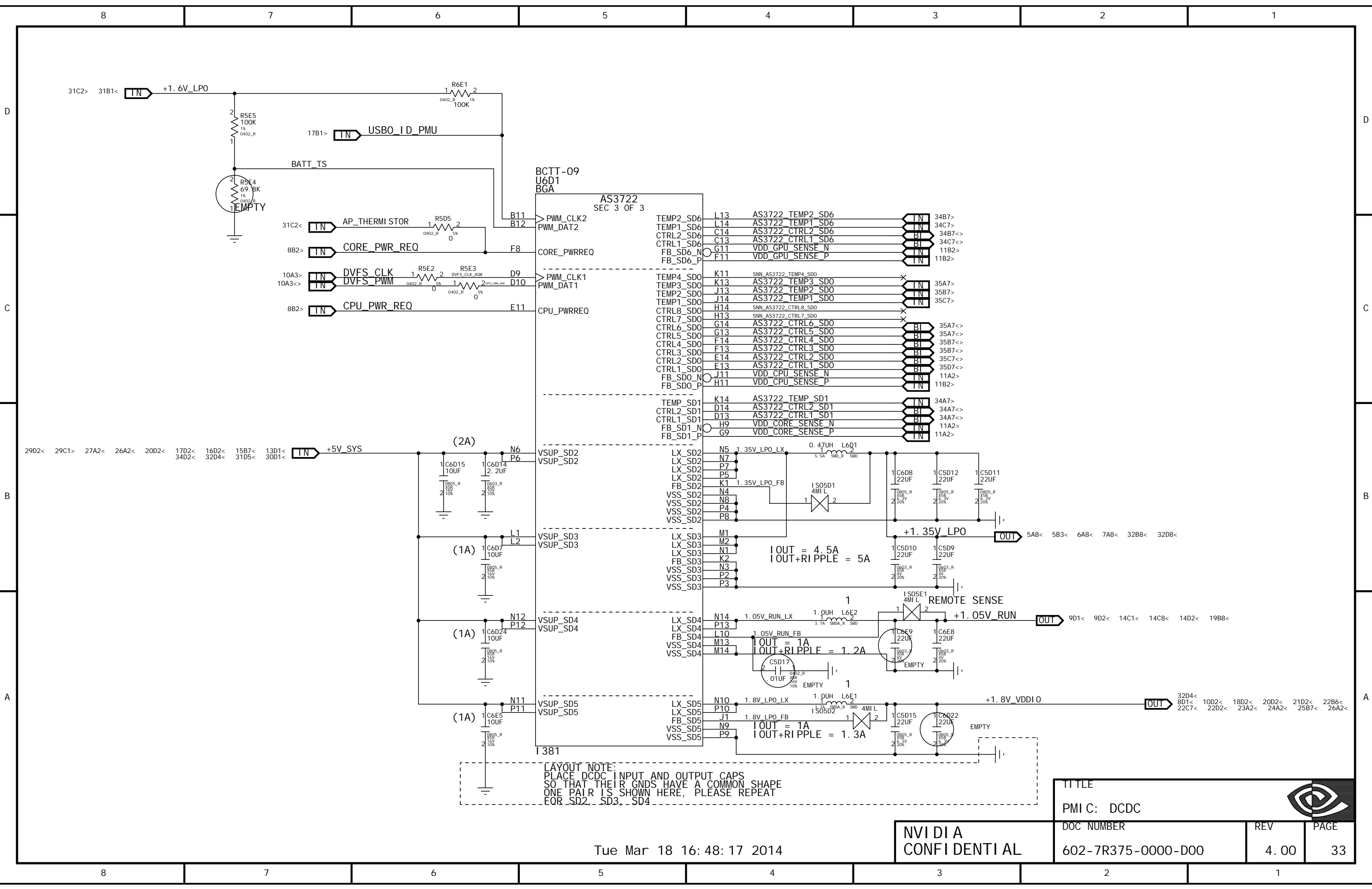
Tue Mar 18 16:48:16 2014



TITLE		
PMI C: CNTL, INT SW, LDOS		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.00	32

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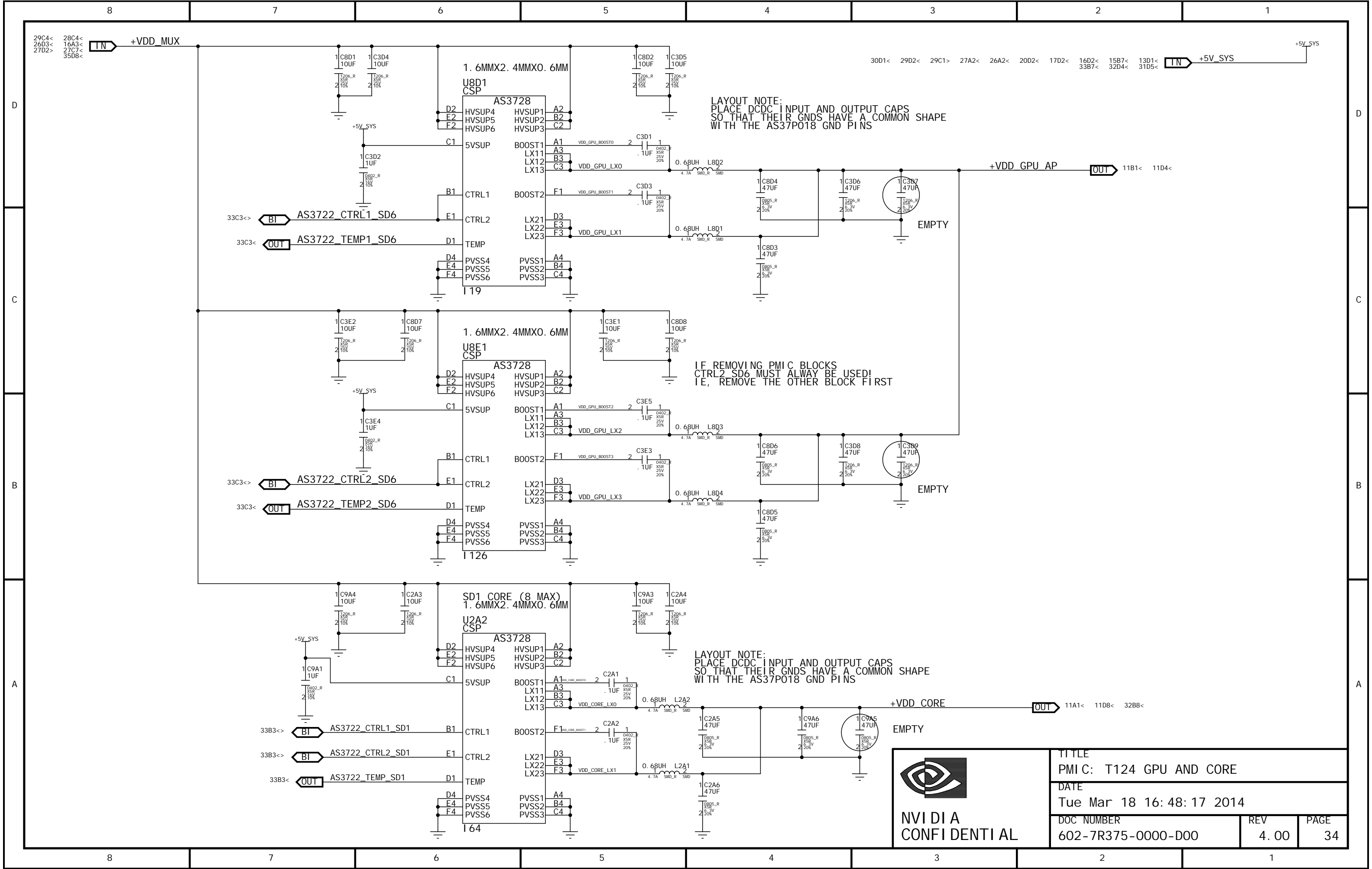


LAYOUT NOTE:
 PLACE DCDC INPUT AND OUTPUT CAPS
 SO THAT THEIR GNDS HAVE A COMMON SHAPE
 ONE PAIR IS SHOWN HERE, PLEASE REPEAT
 FOR SD2, SD3, SD4

TITLE		
PMI C: DCDC		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.00	33

NV I D I A
 C O N F I D E N T I A L

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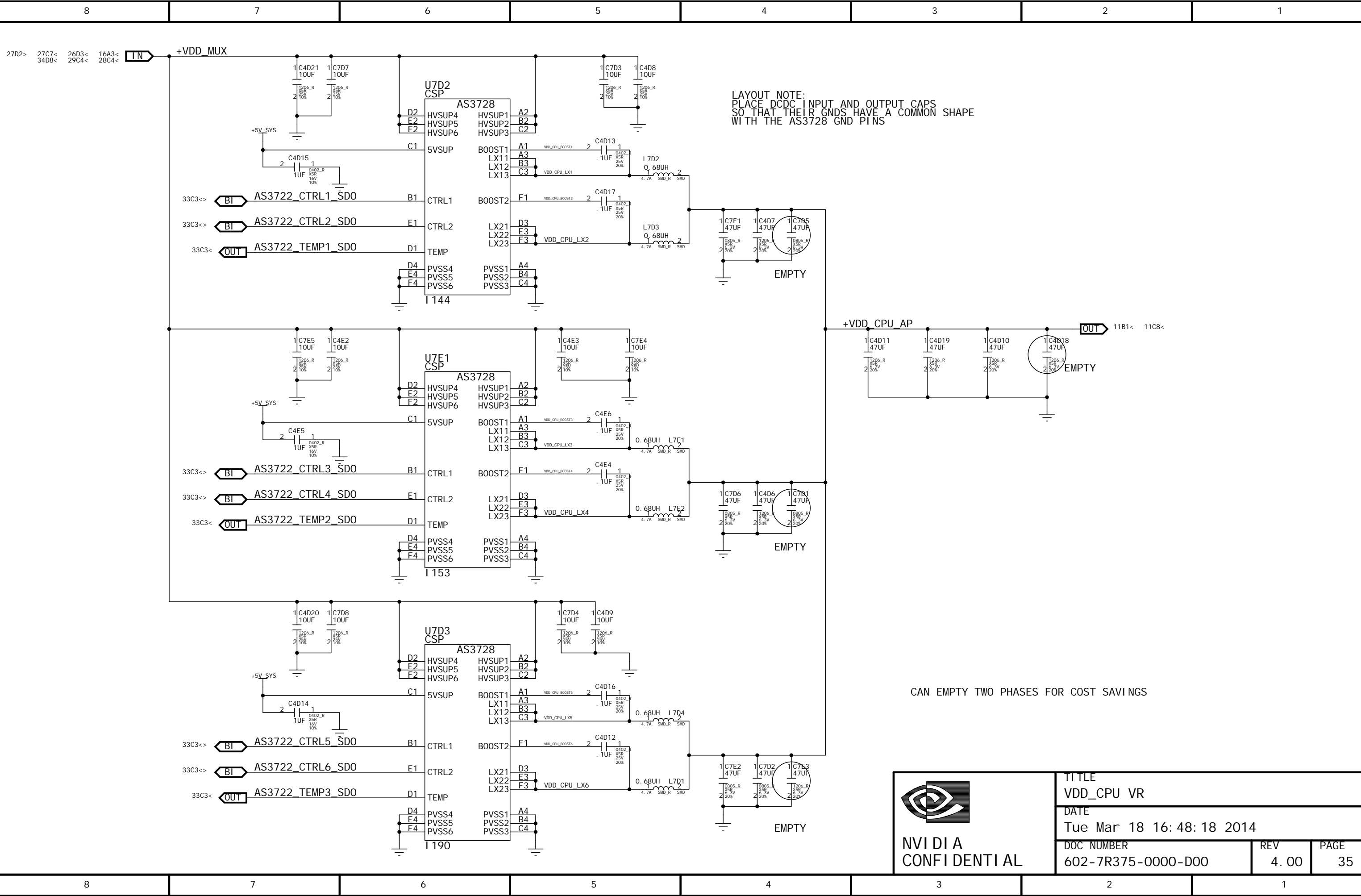
LAYOUT NOTE:
 PLACE DCDC INPUT AND OUTPUT CAPS
 SO THAT THEIR GNDS HAVE A COMMON SHAPE
 WITH THE AS37P018 GND PINS

IF REMOVING PMIC BLOCKS
 CTRL2 SD6 MUST ALWAYS BE USED!
 IE, REMOVE THE OTHER BLOCK FIRST

LAYOUT NOTE:
 PLACE DCDC INPUT AND OUTPUT CAPS
 SO THAT THEIR GNDS HAVE A COMMON SHAPE
 WITH THE AS37P018 GND PINS



TITLE		
PMIC: T124 GPU AND CORE		
DATE		
Tue Mar 18 16: 48: 17 2014		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.00	34



LAYOUT NOTE:
PLACE DCDC INPUT AND OUTPUT CAPS
SO THAT THEIR GNDS HAVE A COMMON SHAPE
WITH THE AS3728 GND PINS

CAN EMPTY TWO PHASES FOR COST SAVINGS



TITLE VDD_CPU VR		
DATE Tue Mar 18 16:48:18 2014		
DOC NUMBER 602-7R375-0000-D00	REV 4.00	PAGE 35

REVISION HISTORY

REVISION 1.00

BOM REVISION D

- RELEASED FAB A

REVISION 1.01

BOM REVISION E

- RELEASED FAB A
- UPDATE I2C MAP (P3)
- STUFF USB_VBUS_EN(0;1) PULLUPS (P17)
- STUFF USB0_VBUS RESISTOR TO 3.3V (P9)
- UPDATE EOL_HDMI_CONN (P13)
- CHANGE R5C10 TO 5 MOHM FOR COST SAVINGS (P27)
- CHANGE R3E5 -> 100K OHM; SATA POWER DIVIDER (P16)
- CHANGE DFF CLEAR (P31)
- CHANGE PMIC TO OTP TYPE 9 (P31-33)
- EMPTY C4B2 EXCESS BYPASS FOR 3.3V SD CARD (P30)
- CHANGE SLEW RATE CAP C9D1 TO 3.3NF (P30)
- EMPTY 3.3V RESISTORS ON GEN2_I2C STUFF 1.8V (P10)
- EMPTY R2D6 & R2D8, ADD R2D7 FOR LAN ISOLATEB (P19)
- BYPASS & EMPTY LOAD SWITCH U2C1 (P30)

REVISION 2.00

BOM REVISION B

- CHANGE RC ON DFF W/ CLOCK OPTIONS (P28,31)
- WIRE GPIO_PK2 TO EXPANSION HDR (P10, P26)
- WIRE +5V_SYS TO R2A5 (P25)
- RESIZE 0_OHM BYPASS RESISTORS TO 0402 (P30)
- CHANGE GEN2_I2C PULLUPS TO +3.3V_LPO (P10)
- RESIZE FAN RESISTORS (P27)
- REWIRE ISOLATEB ON LAN (P19)
- DIRECT WIRE VDD_GPIO_LV TO +1.8V_VDDIO (P31)
- REPLACE POWER FETS ON 3.3V SWITCHER (P28)
- REPLACE SD CARD SWITCH (P30)
- EMPTY USB ESD PROTECTION (P17)
- EMPTY SD ESD PROTECTION (P25)
- ADD BLEED RESISTORS ON DC INPUT (P27)
- SIMPLIFY FEEDBACK, DROP BLEED RESISTORS (P11)
- TUNE +5V_SYS & +3V3_SYS FOR 3.3UH INDUCTORS (P27-29)
- ADD DEBUG CONNECTOR (P22)
- ADD TEMP SENSOR BUFFERING OPTIONS (P18)
- RELEASED FAB B

REVISION 3.00

BOM REVISION A


- MODIFY EXPANSION HEADER (P11, P26)
- STUFF FRONT PANEL HEADER (P25)
- CHANGE AUDIO HEADER TO LIME/PINK (P21)
- RELEASED FAB C

REVISION 4.00

- REWIRE ONKEY TO KB_COLO FET (P24)
- REMOVE LED DIODE (P25)
- UART4 INPUTS STUFFING OPTIONS (P24)
- ADD EMI_CAP (P21)
- ADD EMI_CAP ON VDD_MUX (P29)
- REPLACE EOL_SNUBBERS (P24)
- ADD PMU_REGEN3_OPTION FOR LAN (P21)
- RELEASED FAB D

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TITLE			
REVISION HISTORY			
DOC NUMBER	REV	PAGE	
602-7R375-0000-D00	4.00	36	

Title: Basenet Report
Design: beaver_t124_fabd
Date: Mar 18 17:18:52 2014

Base nets and synonyms for
beaver_t124_lib.BEAVER_T124_FABD(@beaver_t124_lib.beaver
_t124_fabd(sch_1))

Base Signal Location([Zone][dir])

+1. 2V_GEN_AVDD 9C1< 9D8< 14D1< 26B4< 32C4>
+1. 2V_RUN_CAM_FRONT 26B4< 32C4>
+1. 05V_LAN_REGOUT 19B3
+1. 05V_LAN_REGOUT_L 19C4
+1. 05V_LPO_VDD_RTC 8C3< 32B5>
+1. 05V_RUN 9D1< 9D2< 14C1< 14C8< 14D2< 19B8<
33A2>
+1. 05V_RUN_AVDD 5D2< 9C2< 9C4< 14C1< 14C7< 32D5>
+1. 05V_RUN_AVDD_HDMI 9C3
_PLL_AP
+1. 05V_RUN_AVDD_HDMI 9D5
_PLL_AP_GATE
+1. 05V_RUN_AVDD_PEX_ 14C3
PLL_AP_F
+1. 05V_RUN_AVDD_SATA 14C7
_PLL_F
+1. 05V_RUN_CAM_REAR 26B7< 32C4>
+1. 6V_LPO 31B1< 31C2> 33D8<
+1. 8V_LPO_AVDD_OSC_A 8A4
P_F
+1. 8V_RUN_AVDD_PLL_U 9A5
TMI P_AP_F
+1. 8V_RUN_CAM 9B8< 26B4< 32C5>
+1. 8V_RUN_VPP_FUSE 8A3< 32A4>
+1. 8V_RUN_VPP_FUSE_R 32A5
+1. 8V_VDDI O 8D1< 10D2< 18D2< 20D2< 21D2< 22B6<
22C7< 22D2< 23A2< 24A2< 25B7< 26A2<
32D4< 33A2>
+1. 8V_VDDI O_LPO_OFF 9A2< 30A6>
+1. 35V_LPO 5A8< 5B3< 6A8< 7A8< 32B8< 32D8<
33B2>
+1. 35V_LPO_VDDI O_DDR 5B3
_MCLK_AP
+2. 5V_AON_RTC 24A8< 24B8< 31B7> 31C6< 31C8<
+2. 8V_RUN_CAM 26B7< 32B4>
+2. 8V_RUN_CAM_AF 26B4< 32A5>
+2V_STBY 27C4> 28B7< 29B7<
+3. 3V_342 22D7
+3. 3V_AON 27A8< 27B4> 27B8< 28C8<
+3. 3V_AVDD_HDMI_AP_G 9D5
ATED
+3. 3V_LPO 9A2< 10D2< 13D1< 14D1< 15D1< 17D2<
18D2< 19D2< 22D2< 30A3>
+3. 3V_RUN 9B3 9D2 18B4 23D4 25D4 30D5 32A7
32C7 9A2< 18D2< 22D8< 23A2< 26D6<
30C5> 30D1< 32D3<
9B3 9D2 18B4 23D4 25D4 30D5 32A7
32C7 9A2< 18D2< 22D8< 23A2< 26D6<

30C5> 30D1< 32D3<
+3. 3V_RUN 9B3 9D2 18B4 23D4 25D4 30D5 32A7
32C7 9A2< 18D2< 22D8< 23A2< 26D6<
30C5> 30D1< 32D3<
9B3 9D2 18B4 23D4 25D4 30D5 32A7
32C7 9A2< 18D2< 22D8< 23A2< 26D6<
30C5> 30D1< 32D3<
+3. 3V_RUN_TOUCH 26D6< 32B5>
+3. 3V_SD_CARD 25B7< 30B1>
+3. 3V_SYS 22D2< 26D6< 28C1> 28D2< 30D1< 32B8<
+5V_HDMI 13A5
+5V_HDMI_CON 13A4
+5V_SATA 16C2
+5V_STBY 27A7< 27B4> 28C8<
+5V_SYS 13D1< 15B7< 16D2< 17D2< 20D2< 26A2<
27A2< 29C1> 29D2< 30D1< 31D5< 32D4<
33B7< 34D2<
+5V_USB_HS 17B5
+12V_SATA 16B2
+AVDD_LVDSO_PLL_AP_F 9B4
+EMMC_VDDI 23C4
+USBO_VBUS_SW 17C4
+VBACKUP 31B5
+VCAP_SLUGO3 30A5
+VDDI O_SDMMC3 8A8< 8B8< 32C5>
+VDD_1V5_MPCI E 15B4
+VDD_ACI N 27D5
+VDD_CORE 11A1< 11D8< 32B8< 34A2>
+VDD_CPU_AP 11B1< 11C8< 35C2>
+VDD_GPU_AP 11B1< 11D4< 34D2>
+VDD_MI C 20B4
+VDD_MUX 16A3< 26D3< 27C7< 27D2> 28C4< 29C4<
34D8< 35D8<
+VDD_MUX_AS3720_VBAT 31B5
1. 05V_RUN_AVDD_HDMI _ 9C3
PLL_AP_EN_L
1. 05V_RUN_FB 33A4
1. 05V_RUN_LX 33A4
1. 8V_LPO_FB 33A4
1. 8V_LPO_LX 33A4
1. 35V_LPO_FB 33B4
1. 35V_LPO_LX 33B4
1P5V_EN 15B5
3. 3V_LPO_CAP 30B7
3. 3V_MAIN_COMP 28A7
3. 3V_MAIN_COMP_RC 28B7
3. 3V_MAIN_CS_N 28B5
3. 3V_MAIN_CS_P 28B5
3. 3V_MAIN_DRVH 28C5
3. 3V_MAIN_DRVH_R 28C5
3. 3V_MAIN_DRVL 28C5
3. 3V_MAIN_I SO 28B2
3. 3V_MAIN_PGOOD_R 28C7> 31A8<
3. 3V_MAIN_RST 28B7
3. 3V_MAIN_SNUB 28C4
3. 3V_MAIN_SW 28C5
3. 3V_MAIN_VBST 28C5

3. 3V_MAIN_VBST_RC 28C5
3. 3V_MAIN_VFB 28B5
3. 3V_RUN_AVDD_HDMI_A 9D3
P_EN_L
5V_MAIN_COMP 29A7
5V_MAIN_COMP_RC 29A7
5V_MAIN_CS_N 29B5
5V_MAIN_CS_P 29B5
5V_MAIN_DRVH 29C5
5V_MAIN_DRVH_R 29C5
5V_MAIN_DRVL 29B5
5V_MAIN_I SO 29B2
5V_MAIN_PGOOD_R 29C7
5V_MAIN_RST 29B7
5V_MAIN_SNUB 29B4
5V_MAIN_SW 29C5
5V_MAIN_VBST 29B5
5V_MAIN_VBST_RC 29B5
5V_MAIN_VFB 29A5
AC_OK_AP_L 10B4
AC_OK_CLK 31A7
AC_OK_CLR_L 31A7
AC_OK_PMU_L 31B5
AP_FORCE_RECOVERY_L 10C3< 24D5>
AP_OVERHEAT_L 18A1> 31C8<
AP_OVERHEAT_R_L 18A3
AP_OVRHT_G 18A3
AP_THERMI STOR 31C2< 33C7<
AS3720_5V_VR_EN 27A8< 28B8< 29B8< 31B6>
AS3720_CREF 31A4
AS3720_EN5V 31B5
AS3720_RB I AS 31B5
AS3720_XI N32K 31B3
AS3720_XOUT32K 31B3
AS3722_CTRL1_SDO 33C3<> 35D7<>
AS3722_CTRL1_SD1 33B3<> 34A7<>
AS3722_CTRL1_SD6 33C3<> 34C7<>
AS3722_CTRL2_SDO 33C3<> 35C7<>
AS3722_CTRL2_SD1 33B3<> 34A7<>
AS3722_CTRL2_SD6 33C3<> 34B7<>
AS3722_CTRL3_SDO 33C3<> 35B7<>
AS3722_CTRL4_SDO 33C3<> 35B7<>
AS3722_CTRL5_SDO 33C3<> 35A7<>
AS3722_CTRL6_SDO 33C3<> 35A7<>
AS3722_TEMP1_SDO 33C3< 35C7>
AS3722_TEMP1_SD6 33C3< 34C7>
AS3722_TEMP2_SDO 33C3< 35B7>
AS3722_TEMP2_SD6 33C3< 34B7>
AS3722_TEMP3_SDO 33C3< 35A7>
AS3722_TEMP_SD1 33B3< 34A7>
AUD1_VREF1 20B4
AUD1_VREF2 20B4
AUDIO_AVDD 20B4
AUDIO_DACREF 20B4
AUDIO_GND 20A1
20A3
20C3

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TITLE	20A1 20A2 20A2 20A3 20A3 20A3
DOC NUMBER	20A6 20B2 20B2 20B2 20B3 20B3
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 8B7 8B7 8B7 8C4 8C6 8C7 8D3 8D4
 8D4 8D6 8D6 8D8 9A3 9A3 9A4 9A4 9A4
 9A4 9A4 9A7 9A7 9A7 9B4 9B4 9B4 9B4
 9B7 9B7 9B8 9C2 9C3 9C3 9C3 9C4 9D3
 9D3 9D4 9D4 9D4 9D7 9D7 10B2 10B3
 10B6 10B7 10D3 10D3 10D3 10D3 10D6
 10D7 11A4 11A4 11A8 11A8 11B4 11B8
 11B8 11C4 11C4 11C8 11D8 12A3 12A4
 12A6 12A6 12A6 12A7 12B6 12B6 12B6
 12B7 13A4 13A4 13A5 13A7 13A7 13B4
 13B4 13C3 13C4 13C5 13C6 13C7 13D4
 13D5 14A1 14A2 14C2 14C2 14C2 14C2
 14C3 14C3 14C3 14C3 14C6 14C6 14C6
 14C6 14C7 14D2 14D3 14D6 14D6 14D7
 15B4 15B4 15B4 15B5 15B5 15B5 15B6
 15B6 15C2 15C2 15C3 15C4 16A2 16A2
 16A3 16B1 16B2 16B2 16B2 16B3 16B4
 16C1 16C3 17A1 17A2 17A4 17A4 17A5
 17A6 17B2 17B2 17B3 17B3 17B5 17B5
 17B5 17B5 17B6 17B6 17B7 17B8 17C1
 17C3 17C5 17C6 17C6 17C6 17C7 17D3
 17D6 18A2 18A3 18A4 18A4 18B2 18B3
 18B4 18B5 18B6 18B6 18B7 18C3 18C4
 18C5 18C5 18C5 18C7 18D3 19A1 19A2
 19A2 19A3 19A5 19A6 19A6 19B3 19B3
 19B4 19B4 19B4 19B4 19B4 19B4 19B6
 19B6 19C3 19C4 19C4 19C4 19C4 19C4
 20A4 20A4 20A4 20A4 20A4 20A4 20A5
 20A6 20B7 20B7 20B7 21A3 21A6 21B5
 22A1 22A1 22A2 22A2 22A2 22A3 22A3
 22A4 22A5 22B5 22B6 22B7 22C2 22C3
 22C3 22C6 22C6 22D7 23A5 23B4 23C4
 23C4 23C4 23C4 23D4 23D4 24A4 24A4
 24A4 24A4 24A6 24A6 24A7 24A8 24A8
 24B4 24B7 24B7 24B8 24C4 24C7 24C7
 24C8 25A4 25A4 25A4 25A5 25A6 25C3
 25C4 25C5 25D5 25D6 26A5 26A5 26C5
 26C5 26C5 26C5 27A4 27A5 27A6 27B5
 27C2 27C3 27C5 27C6 27D3 27D3 27D3
 27D4 27D4 27D6 28B4 28B4 28B7 28C2
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C3D6	CAP_1206_R	[34D4]
C3D7	CAP_1206_R	[34D3]
C3D8	CAP_1206_R	[34B4]
C3D9	CAP_1206_R	[34B3]
C3E1	CAP_1206_R	[34C5]
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C3E3	CAP_0402_R	[34B5]
C3E4	CAP_0402_R	[34B6]
C3E5	CAP_0402_R	[34B5]
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C3E7	CAP_0402_R	[16A2]
C3E8	CAP_0402_R	[16B2]
C3E9	CAP_0805_R	[16C3]
C3E10	CAP_0402_R	[16C2]
C3E11	CAP_0402_R	[16B3]
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C4B1	CAP_0201_R	[6A7]
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C4B3	CAP_0402_R	[6A8]
C4B4	CAP_0805_R	[30C4]
C4B5	CAP_0402_R	[30C3]
C4B6	CAP_0402_R	[30B2]
C4C1	CAP_0402_R	[7A7]
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C4C4	CAP_0201_R	[7A6]
C4C5	CAP_0201_R	[7B4]
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C4D3	CAP_0402_R	[23D4]
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C5D5	CAP_1206_R	[27D3]
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C5D10	CAP_0603_R	[33B3]
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?	[31B5]
?	[33A3]



	8	7	6	5	4	3	2	1		
D	L5C2	INDUCTOR_SMD_R	[28C3]	Q9E3	MOSFETNSOT23_S23_R	[17A2]	R2B4	RES_0201_R	[26C5]	
	L6D1	INDUCTOR_SMD_R	[33B4]	Q10B1	MOSFETNSOT23_S23_R	[13C5]	R2B5	RES_0201_R	[24D2]	
	L6E1	PWR_INDUTOR_SMDA_R	[33A4]	R1A1	RES_0603_R	[25D4]	R2B6	RES_0201_R	[10B2]	
	L6E2	PWR_INDUTOR_SMDA_R	[33A4]	R1A2	RES_0603_R	[25D5]	R2B7	RES_0201_R	[24D3]	
	L7D1	INDUCTOR_SMD_R	[35A5]	R1A3	RES_0603_R	[25D4]	R2B8	RES_0201_R	[10B2]	
	L7D2	INDUCTOR_SMD_R	[35D5]	R1A4	RES_0402_R	[25C3]	R2B9	RES_0402_R	[8C7]	
	L7D3	INDUCTOR_SMD_R	[35C5]	R1A5	RES_0402_R	[25D3]	R2C1	RES_0402_R	[8C8]	
	L7D4	INDUCTOR_SMD_R	[35A5]	R1A6	RES_0402_R	[25C6]	R2C2	RES_0402_R	[30A7]	
	L7E1	INDUCTOR_SMD_R	[35B5]	R1A7	RES_0603_R	[25D5]	R2C3	RES_0402_R	[22A4]	
	L7E2	INDUCTOR_SMD_R	[35B5]	R1A8	RES_0402_R	[18C2]	R2C4	RES_0402_R	[14A3]	
C	L8B1	INDUCTOR_0402_R	[8A3]	R1B1	RES_0201_R	[24D7]	R2C5	RES_0201_R	[16B7]	
	L8D1	INDUCTOR_SMD_R	[34C4]	R1B2	RES_0201_R	[24C7]	R2C6	RES_0201_R	[16B7]	
	L8D2	INDUCTOR_SMD_R	[34D4]	R1B3	RES_0201_R	[24C7]	R2C7	RES_0402_R	[24A4]	
	L8D3	INDUCTOR_SMD_R	[34B4]	R1B4	RES_0201_R	[24D7]	R2C8	RES_0402_R	[24A4]	
	L8D4	INDUCTOR_SMD_R	[34B4]	R1B5	RES_0201_R	[24D6]	R2C9	RES_0402_R	[24A4]	
	L9B1	INDUCTOR_0402_R	[9B4]	R1B6	RES_0201_R	[24C6]	R2C10	RES_0402_R	[24A4]	
	L9B2	INDUCTOR_0402_R	[9A4]	R1B7	RES_0402_R	[13A7]	R2D1	RES_0402_R	[18A2]	
	L9C1	INDUCTOR_0402_R	[14C2]	R1B8	RES_0402_R	[13B6]	R2D2	RES_0402_R	[18B3]	
	L9C2	INDUCTOR_0402_R	[14D2]	R1B9	RES_0402_R	[13B6]	R2D3	RES_0402_R	[18B3]	
	L9C3	INDUCTOR_0402_R	[14C7]	R1B10	RES_0402_R	[18B7]	R2D4	RES_0402_R	[19A3]	
B	L9C4	CHOKE_2012_R	[17B6 17B6]	R1B11	RES_0402_R	[18B7]	R2D5	RES_0402_R	[19A3]	
	L10B1	INDUCTOR_0402_R	[13B6]	R1C1	RES_0402_R	[13D4]	R2D6	RES_0402_R	[19A3]	
	L10B2	INDUCTOR_0402_R	[13B6]	R1C2	RES_0402_R	[17B7]	R2D7	RES_0402_R	[30A4]	
	L10B3	INDUCTOR_0402_R	[13C4]	R1D1	RES_0402_R	[19A4]	R2D8	RES_0402_R	[19B6]	
	L10E1	INDUCTOR_0402_R	[20A6]	R1D2	RES_0402_R	[19A1]	R2D9	RES_0402_R	[19C6]	
	M1A1	BRD_MOUNT_BRDMNT2	[12B7]	R1D3	RES_0402_R	[22D2]	R2D10	RES_0402_R	[19C6]	
	M1E1	BRD_MOUNT_BRDMNT2	[12A7]	R1D4	RES_0402_R	[22D2]	R2D11	RES_0402_R	[19B7]	
	M2E1	PEM_SMT_R	[15D4]	R1D5	RES_0402_R	[22D2]	R3A1	RES_0402_R	[23B6]	
	M3E1	PEM_SMT_R	[15C4]	R1D6	RES_0402_R	[21C5]	R3A2	RES_0402_R	[23B4]	
	M5A1	BRD_MOUNT_BRDMNT2	[12A6]	R1D7	RES_0402_R	[21C5]	R3B1	RES_0201_R	[24B4]	
A	M5E1	BRD_MOUNT_BRDMNT2	[12B6]	R1D8	RES_0402_R	[21C5]	R3B2	RES_0201_R	[24B3]	
	Q1A1	MOSFETN_SC70S_SC70S_R	[25C4]	R1D9	RES_0402_R	[21C4]	R3B3	RES_0402_R	[10B2]	
	Q1A2	MOSFETN_SC70S_SC70S_R	[25D6]	R1E1	RES_0402_R	[21B4]	R3B4	RES_0201_R	[24D3]	
	Q1A3	MOSFETN_SC70S_SC70S_R	[25C3]	R1E2	RES_0402_R	[21B5]	R3B5	RES_0201_R	[24D3]	
	Q1E1	MOSFETN_SC70S_SC70S_R	[21B5]	R1E3	RES_0402_R	[21B5]	R3B6	RES_0201_R	[8C3]	
	Q2D1	MOSFETN_SC70S_SC70S_R	[18A2]	R1E4	RES_0402_R	[17D3]	R3B7	RES_0201_R	[8C3]	
	Q2D2	MOSFETN_SC70S_SC70S_R	[18A3]	R1E5	RES_0402_R	[20B1]	R3C1	RES_0201_R	[5A6]	
	Q2D3	MOSFETN_SC70S_SC70S_R	[17C6]	R1E6	RES_0402_R	[20B3]	R3C2	RES_0201_R	[5A6]	
	Q3E1	MOSFETN_SC70S_SC70S_R	[16A2]	R1E7	RES_0402_R	[20C7]	R3C3	RES_0201_R	[8C3]	
	Q3E2	MOSFETP_DFN3X3_DFN3X3_R	[16A2]	R1E8	RES_0402_R	[20B7]	R3C4	RES_0201_R	[10A6]	
Q4A1	MOSFETN_SC70S_SC70S_R	[27C3]	R1E9	RES_0402_R	[20C3]	R3C5	RES_0201_R	[8C2]		
Q4A2	MOSFETPSOT23_S23_R	[27D2]	R1E10	RES_0402_R	[20C2]	R3C6	RES_0201_R	[10B6]		
Q4E1	MOSFETNSOT23_S23_R	[24A6]	R2A1	RES_0402_R	[18D6]	R3C7	RES_0402_R	[24A4]		
Q4E2	MOSFETP_SC70_SC70_R	[24A6]	R2A2	RES_0402_R	[18D5]	R3C8	RES_0402_R	[24A4]		
Q5D1	MOSFETNSOT23_S23_R	[32B1]	R2A3	RES_0402_R	[18D5]	R3C9	RES_0402_R	[24A4]		
Q5D2	MOSFETNSOT23_S23_R	[32B2]	R2A4	RES_0402_R	[9D3]	R3C10	RES_0402_R	[24A4]		
Q6C1	MOSFETN_DFN_DUAL_DFN3X3	[29C4]	R2A5	RES_0402_R	[9C3]	R3E1	RES_0402_R	[16A2]		
Q6C2	MOSFETN_DFN_DUAL_DFN3X3	[28C4]	R2A6	RES_0402_R	[9D2]	R3E2	RES_0402_R	[16A3]		
Q9A1	MOSFETPSOT23_S23_R	[9C3]	R2A7	RES_0402_R	[9C2]	R3E3	RES_0402_R	[16A3]		
Q9A2	MOSFETPSOT23_S23_R	[9D3]	R2A8	RES_0402_R	[9D3]	R3E4	RES_0402_R	[16A3]		
Q9A3	MOSFETNSOT23_S23_R	[9C3]	R2A9	RES_0402_R	[9D2]	R3E5	RES_0402_R	[16B2]		
Q9A4	MOSFETNSOT23_S23_R	[9D3]	R2A10	RES_0402_R	[9D2]	R3E6	RES_0402_R	[16B4]		
Q9D1	NPN_S363_R	[19B6 19B6]	R2A11	RES_0402_R	[9C2]	R4A1	RES_0402_R	[22B2]		
Q9D2	MOSFETN_SC70S_SC70S_R	[15C2]	R2A12	RES_0402_R	[9C2]	R4A2	RES_0402_R	[22B2]		
Q9D3	MOSFETN_SC70S_SC70S_R	[15C2]	R2B1	RES_0201_R	[24B3]	R4A3	RES_0402_R	[22B2]		
Q9E1	MOSFETNSOT23_S23_R	[17B2]	R2B2	RES_0201_R	[24B3]	R4A4	RES_0402_R	[22A2]		
Q9E2	MOSFETNSOT23_S23_R	[17B3]	R2B3	RES_0201_R	[26C6]					
←→										
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	8	7	6	5	4	3	2	1	
D	R4A6	RES_0402_R	[31C3]	R5E9	RES_0402_R	[11A4]	R8B11	RES_0201_R	[10B7]
	R4A7	RES_0603_R	[27D2]	R5E10	RES_0402_R	[30D5]	R8B12	RES_0201_R	[10C6]
	R4A8	RES_0402_R	[27C3]	R5E11	RES_0201_R	[24D7]	R8B13	RES_0201_R	[8A7]
	R4A9	RES_0402_R	[27C3]	R6B1	RES_0402_R	[25B4]	R8B14	RES_0201_R	[8A3]
	R4A10	RES_0603_R	[27D2]	R6B2	RES_0402_R	[25B5]	R8B15	RES_0201_R	[8A6]
	R4A11	RES_0402_R	[27D3]	R6B3	RES_0402_R	[27B7]	R8B16	RES_0201_R	[10B3]
	R4A12	RES_0402_R	[27C3]	R6B4	RES_0402_R	[27A7]	R8B17	RES_0201_R	[10B3]
	R4A13	RES_0402_R	[22A2]	R6B5	RES_0402_R	[29A7]	R8B18	RES_0201_R	[8B7]
	R4B1	RES_0201_R	[6B3]	R6B6	RES_0402_R	[29A1]	R8B19	RES_0201_R	[4C2]
	R4B2	RES_0201_R	[6B4]	R6B7	RES_0402_R	[27A7]	R8B20	RES_0201_R	[8A4]
C	R4B3	RES_0402_R	[6B5]	R6B8	RES_0402_R	[28A2]	R8B21	RES_0201_R	[4C3]
	R4B4	RES_0402_R	[6B5]	R6B9	RES_0402_R	[28B7]	R8B22	RES_0201_R	[8B7]
	R4C1	RES_0402_R	[7B5]	R6C1	RES_0402_R	[28B3]	R8B23	RES_0201_R	[8A4]
	R4D1	RES_0201_R	[23D6]	R6C2	RES_0402_R	[29B3]	R8C1	RES_0201_R	[4C2]
	R4D2	RES_0402_R	[30C7]	R6C3	RES_0805_R	[29B4]	R8C2	RES_0201_R	[4C2]
	R4E1	RES_0402_R	[31C7]	R6C4	RES_0402_R	[29B7]	R8C3	RES_0201_R	[8B3]
	R4E2	RES_0402_R	[31C7]	R6C5	RES_0402_R	[28B7]	R8C4	RES_0201_R	[8A7]
	R4E3	RES_0402_R	[24A6]	R6C6	RES_0402_R	[28C7]	R8C5	RES_0201_R	[11B4]
	R4E4	RES_0402_R	[24A7]	R6C7	RES_0402_R	[28C5]	R8C6	RES_0201_R	[8A7]
	R4E5	RES_0402_R	[24B7]	R6C8	RES_0402_R	[29B3]	R8C7	RES_0201_R	[11A4]
B	R5A1	RES_0402_R	[22A2]	R6C9	RES_0402_R	[28C3]	R8C8	RES_0201_R	[11A4]
	R5A2	RES_0402_R	[22A2]	R6C10	RES_0402_R	[29B3]	R9A1	RES_0402_R	[18D5]
	R5A4	RES_0402_R	[22B3]	R6C11	RES_0402_R	[28C3]	R9B1	RES_0201_R	[24B3]
	R5B1	RES_0402_R	[27B7]	R6C12	RES_0805_R	[28C4]	R9B2	RES_0201_R	[24B3]
	R5B2	RES_0402_R	[27A7]	R6D1	RES_0603_R	[32C1]	R9B3	RES_0201_R	[24D2]
	R5B3	RES_0402_R	[29A1]	R6D2	RES_0402_R	[31B5]	R9B4	RES_0201_R	[10B2]
	R5B4	RES_0402_R	[29A6]	R6D3	RES_0402_R	[31A7]	R9B5	RES_0201_R	[24D3]
	R5B5	RES_0402_R	[27A7]	R6D4	RES_0402_R	[31A7]	R9B6	RES_0201_R	[10B1]
	R5B6	RES_0402_R	[28B6]	R6D5	RES_0402_R	[31B5]	R9B7	RES_0201_R	[9B4]
	R5B7	RES_0402_R	[28B2]	R6D6	RES_0402_R	[31A5]	R9B8	RES_0201_R	[9C4]
A	R5C1	RES_0402_R	[28C7]	R6D7	RES_0402_R	[32C2]	R9B9	RES_0201_R	[9B8]
	R5C2	RES_0402_R	[29C7]	R6D8	RES_0402_R	[31C3]	R9B10	RES_0201_R	[9B8]
	R5C3	RES_0402_R	[28C6]	R6D9	RES_0402_R	[31B2]	R9B11	RES_0201_R	[9B7]
	R5C4	RES_0402_R	[27B6]	R6D10	RES_0402_R	[31B7]	R9B12	RES_0402_R	[8D8]
	R5C5	RES_0603_R	[29C5]	R6D11	RES_0402_R	[31C5]	R9B13	RES_0201_R	[9B7]
	R5C6	RES_0603_R	[28C5]	R6D12	RES_0402_R	[31C5]	R9C1	RES_0402_R	[8D8]
	R5C7	RES_0402_R	[29B5]	R6E1	RES_0402_R	[33D6]	R9C2	RES_0201_R	[9A7]
	R5C8	RES_0603_R	[27D4]	R6E2	RES_0402_R	[11A4]	R9C3	RES_0201_R	[9A7]
	R5C9	RES_0402_R	[27D4]	R6E3	RES_0402_R	[11A2]	R9C4	RES_0201_R	[9A4]
	R5C10	RES_0402_R	[27D4]	R7A1	RES_0201_R	[24D6]	R9C5	RES_0201_R	[9A7]
R5C11	RES_1206_R	[27D4]	R7B1	RES_0201_R	[6B7]	R9C6	RES_0402_R	[9A3]	
A	R5D1	RES_0402_R	[30B7]	R7B2	RES_0201_R	[6B8]	R9C7	RES_0201_R	[14A3]
	R5D2	RES_0402_R	[30C6]	R7C1	RES_0201_R	[7B7]	R9C8	RES_0201_R	[14C6]
	R5D3	RES_0402_R	[31A7]	R7C2	RES_0201_R	[7B7]	R9C9	RES_0201_R	[14C8]
	R5D4	RES_0201_R	[31A2]	R7C3	RES_0201_R	[7B3]	R9C10	RES_0402_R	[18A6]
	R5D5	RES_0402_R	[33C6]	R7C4	RES_0201_R	[7B3]	R9C11	RES_0402_R	[18A6]
	R5D6	RES_0402_R	[31B4]	R7C5	RES_0402_R	[7B5]	R9D1	RES_0402_R	[18A4]
	R5D7	RES_0402_R	[32A5]	R8B1	RES_0201_R	[8A3]	R9D2	RES_0201_R	[16A6]
	R5D8	RES_0402_R	[31B5]	R8B2	RES_0201_R	[24B3]	R9D3	RES_0402_R	[19C5]
	R5E1	RES_0201_R	[31C5]	R8B3	RES_0201_R	[24B4]	R9D4	RES_0201_R	[16A6]
	R5E2	RES_0402_R	[33C6]	R8B4	RES_0402_R	[22C8]	R9D5	RES_0201_R	[16B6]
R5E3	RES_0402_R	[33C6]	R8B5	RES_0402_R	[22D6]	R9D6	RES_0201_R	[16B6]	
R5E4	RES_0402_R	[33D7]	R8B6	RES_0402_R	[22D7]	R9D7	RES_0402_R	[17C7]	
R5E5	RES_0402_R	[33D7]	R8B7	RES_0402_R	[24D3]	R9D8	RES_0402_R	[17C5]	
R5E6	RES_0402_R	[11B4]	R8B8	RES_0201_R	[8A4]	R9D9	RES_0402_R	[15D2]	
R5E7	RES_0402_R	[11B2]	R8B9	RES_0402_R	[24D3]	R9D10	RES_0402_R	[15C3]	
R5E8	RES_0402_R	[11B2]	R8B10	RES_0201_R	[10B8]				
							TITLE	[17C5]	
							?	[15D2]	
							?	[15C3]	
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T4C27	TEE_TEE	[7D7]
T4C28	TEE_TEE	[7D7]
T4C29	TEE_TEE	[7C7]
T4C30	TEE_TEE	[6C7]
T4C31	TEE_TEE	[4C5]
T4C32	TEE_TEE	[7D7]
T4C33	TEE_TEE	[7B7]
T4C34	TEE_TEE	[6C7]
T4C35	TEE_TEE	[7C7]
T4C36	TEE_TEE	[6C7]
T4C37	TEE_TEE	[7B7]
T4C38	TEE_TEE	[6D7]
T4C39	TEE_TEE	[7D7]
T4C40	TEE_TEE	[7D7]
T4C41	TEE_TEE	[6D7]
T4C42	TEE_TEE	[7C7]
T4C43	TEE_TEE	[4C5]
T4C44	TEE_TEE	[6C7]
T4C45	TEE_TEE	[7D7]
T4C46	TEE_TEE	[7B7]
T4C47	TEE_TEE	[7B7]
T4C48	TEE_TEE	[7D7]
T4C49	TEE_TEE	[7B7]
U1B1	SERIAL_RS232_3V3_TSSOP16_R	[18C4]
U1B2	LEVEL_SHIFTER_2BIT_SSOP8_R	[18C6]
U1B3	LEVEL_SHIFTER_2BIT_SSOP8_R	[18B6]
U1B4	POWER_SW_SON7_R	[13A6]
U1C1	POWER_SW_SON8_R	[17B6]
U1D1	PCA9306_QFN8_R	[22C3]
U1E1	ALC5639_QFN48	[20B5]
U2A1	EEPROM_2WIRE_8PIN_DFN08_R	[18D4]
U2A2	AS3728_CSP	[34A6]
U2C1	POWER_SW_BGA04_R	[30A7]
U2C2	TEMP_SENSOR_DFN08	[18A5]
U2D1	SLG5NV1430V_TDFN-6_R	[30A4]
U2D2	RTL8111GS_QFN-33_R	[19B5]
U2D3	POWER_SW_SOT23_5B_R	[17C7]
U3A1	EEPROM_SPI_8PIN_SOIC_R	[23A5]
U3C1	T124MI D_BGA	[4C6]
U3C1	T124MI D_BGA	[5B5]
U3C1	T124MI D_BGA	[8C5]
U3C1	T124MI D_BGA	[9C5]
U3C1	T124MI D_BGA	[10B5]
U3C1	T124MI D_BGA	[11C6]
U3C1	T124MI D_BGA	[12B3]
U3C1	T124MI D_BGA	[14C5]
U3E1	SLG5NV1430V_TDFN-6_R	[16B2]
U4A1	RST_MON_SOT23_6PIN_R	[22A5]
U4A3	RST_MON_SOT23_3_R	[22B5]
U4B1	DDR3_X16_BGA100_2	[6C2]
U4B2	POWER_SW_BGA04_R	[30B3]
U4C1	DDR3_X16_BGA100_2	[7C6]
U5A1	BUFFER_5PIN_SC70_R	[22A3]
U5C1	U_SWREG_TPS51220_QFN32	[27B5]

U5C1	U_SWREG_TPS51220_QFN32	[28B6]
U5C1	U_SWREG_TPS51220_QFN32	[29B6]
U5D1	SLG5NV1430V_TDFN-6_R	[30C6]
U5D2	D_FLIP_FLOP_6PIN_SC70_6	[31A6]
U6D1	AS3722_BGA	[31B4]
U6D1	AS3722_BGA	[32C6]
U6D1	AS3722_BGA	[33B5]
U7B1	DDR3_X16_BGA100_2	[6C6]
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U7D2	AS3728_CSP	[35D6]
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U8D1	AS3728_CSP	[34D6]
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U9E1	APL5910_SOP8P_R	[15B5]
Y2C1	XTAL_HC49_R	[19A6]
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