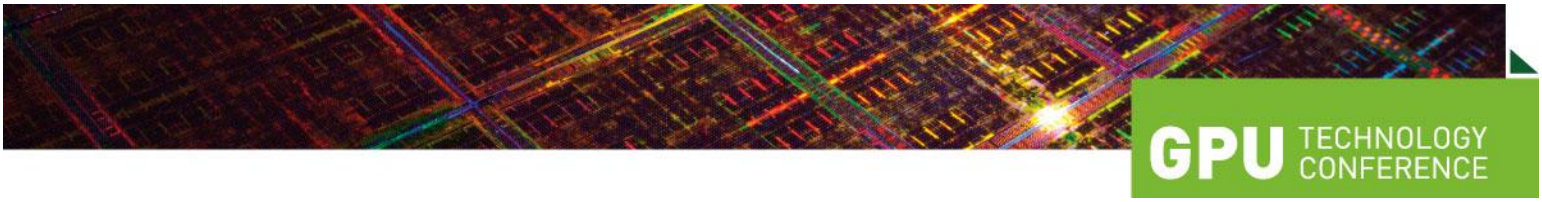


GPU Technology Conference, May 14-17, 2012
McEnery Convention Center, San Jose, California
www.gputechconf.com

Sessions on Electrical Design & Analysis (subject to change)

IMPORTANT: Visit http://www.gputechconf.com/page/sessions.html for the most up-to-date schedule.

S0317 - Compiling a Parallel Domain Specific Language to GPUs
Ramesh Narayanaswamy (Synopsys Inc.)
Day: Tuesday, 05/15 | **Time:** 9:30 am - 9:55 am
Topic Areas: Electrical Design and Analysis; Application Design & Porting Techniques
Session Level: Intermediate

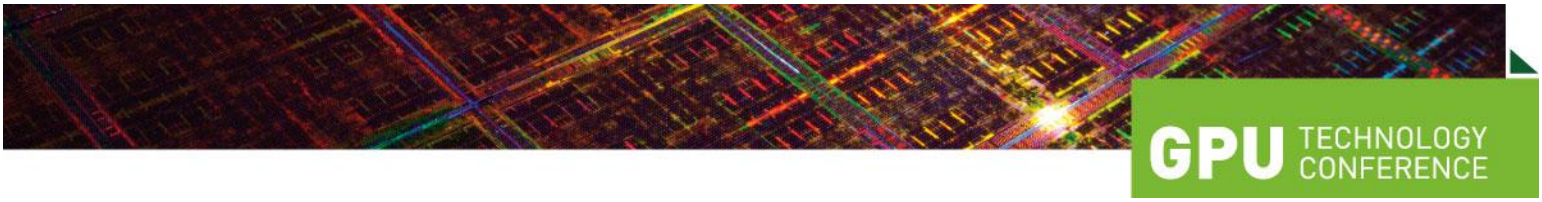
Discuss techniques for compiling Parallel DSLs to GPUs. Verilog is a Domain Specific Language for Hardware Description. Verilog users express parallelism with guarded processes similar to Occam's guarded commands. Review Verilog semantics, and different approaches to compiling Verilog to parallel architectures and to GPUs. Discuss challenges with (a) Verilog description's runtime behavior (b) managing process dependency. Discuss approaches and challenges in compiling a parallel DSL to CUDA C.

S0329 - Using GPUs to Speedup Computational Lithography
Constantin Chuyeshov (Cadence Design Systems)
Day: Tuesday, 05/15 | **Time:** 10:00 am - 10:25 am
Topic Areas: Electrical Design and Analysis
Session Level: Intermediate

In this paper we show how GPUs can be used to significantly speedup computational lithography, which is heavily used in the Electronic Design Automation (EDA) industry. In particular, we demonstrate a noticeable performance increase in several basic optical lithography algorithms as well as the speedup of the full-chip verification software, crucial parts of which were ported to NVIDIA's GPUs. We summarize the advantages, disadvantages and challenges of using GPUs and compare it to more traditional multithreading and distributed computing alternatives for the same applications.

S0520 - Using GPUs to Speedup Chip Verification
Tomer Ben-David (Rocketick)
Day: Tuesday, 05/15 | **Time:** 10:30 am - 11:20 am
Topic Areas: Electrical Design and Analysis
Session Level: Beginner

As VLSI designs become more complex, the process of verifying them becomes increasingly expensive and time consuming. Verification of such designs has become quite taxing as they take simulators to the edge in terms of both runtime demands and host memory requirements. In order to reduce verification time, different verification methodologies have been adopted including the use of emulators. However, emulators' price point is high and so is the engineering time to set them up. Rocketick develops a Verilog co-simulator that uses GPUs as an acceleration platform. Rocketick's product, RocketSim® is now part of NVIDIA's design flow and it is being used to accelerate simulations by 10X-30X compared to the standard simulator and to reduce the memory footprint by 5X. In this session RocketSim® will be presented using some real-world examples of verification flows.



S0069 - GPU Computing Advances in 3D Electromagnetic Simulation
Fabrizio Zanella (CST of America), Andreas Buhr (CST AG)
Day: Tuesday, 05/15 | **Time:** 2:00 pm - 2:25 pm
Topic Areas: Electrical Design and Analysis
Session Level: Intermediate

Learn about the latest developments in GPU acceleration for 3D Full Wave Electromagnetic simulation. The latest version of CST Studio Suite supports the full range of Tesla products on both Windows and Linux operating systems. Using GPU, multi-GPU and MPI-GPU Computing drastically reduces the simulation times for CST customers. We will provide a status of current and future GPU developments at CST and share detailed simulation results.